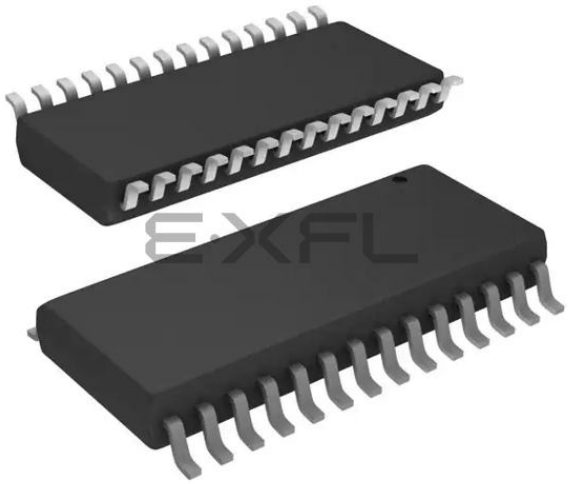

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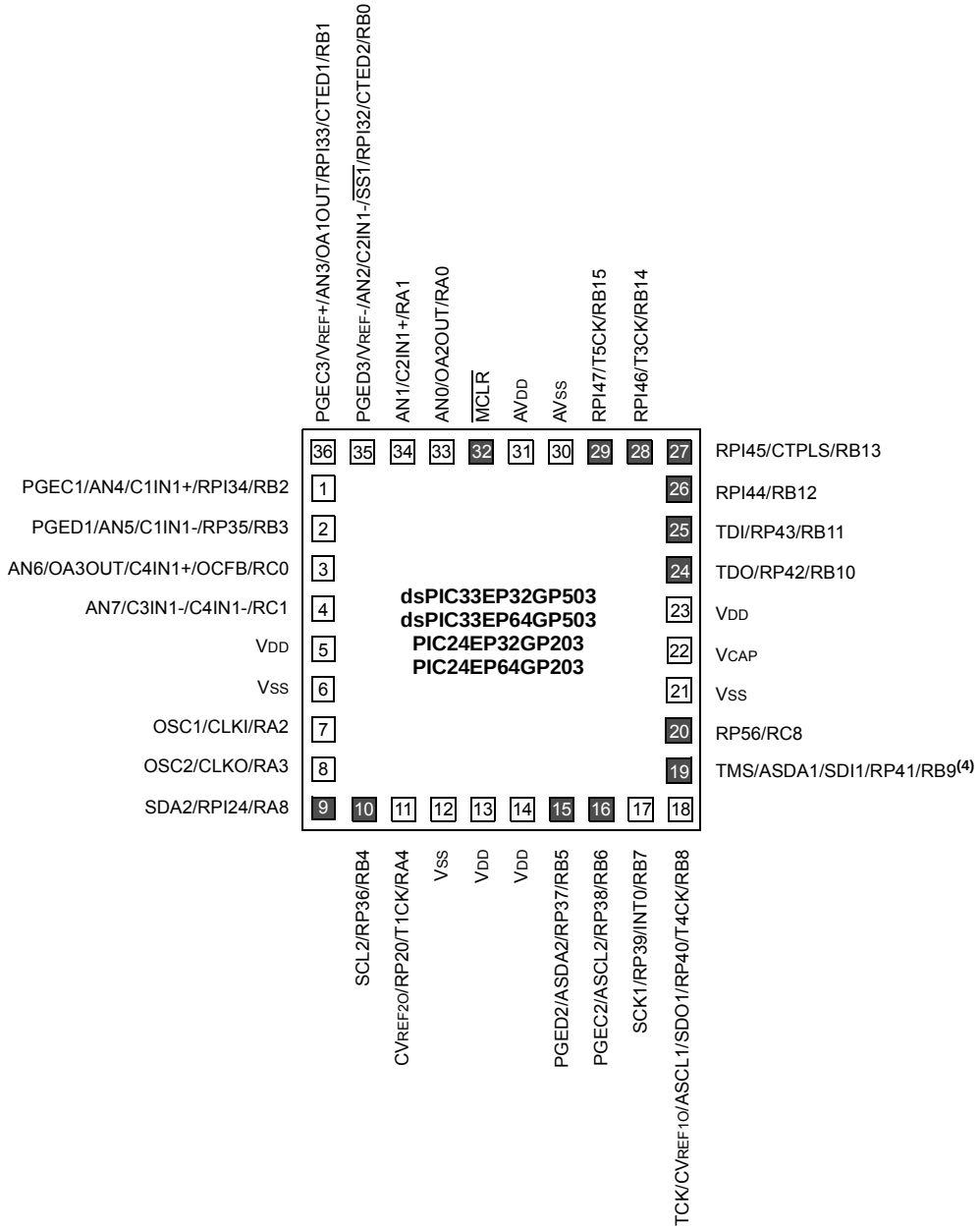
Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	PIC
Core Size	16-Bit
Speed	70 MIPs
Connectivity	I²C, IrDA, LINbus, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, DMA, POR, PWM, WDT
Number of I/O	21
Program Memory Size	128KB (43K x 24)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	8K x 16
Voltage - Supply (Vcc/Vdd)	3V ~ 3.6V
Data Converters	A/D 6x10b/12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	28-SOIC (0.295", 7.50mm Width)
Supplier Device Package	28-SOIC
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/pic24ep128gp202t-i-so

Pin Diagrams (Continued)

36-Pin VTLA(1,2,3)

■ = Pins are up to 5V tolerant



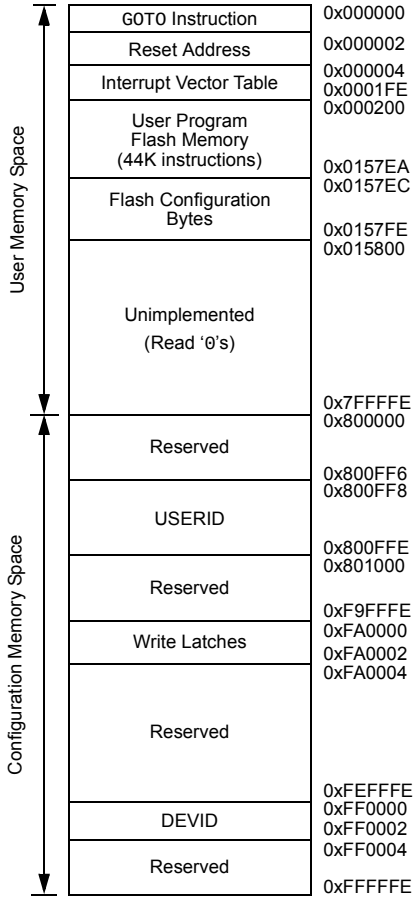
Note 1: The RPn/RPIn pins can be used by any remappable peripheral with some limitation. See **Section 11.4 "Peripheral Pin Select (PPS)"** for available peripherals and for information on limitations.

2: Every I/O port pin (RAx-RGx) can be used as a Change Notification pin (CNAx-CNGx). See **Section 11.0 "I/O Ports"** for more information.

3: The metal pad at the bottom of the device is not connected to any pins and is recommended to be connected to VSS externally.

4: There is an internal pull-up resistor connected to the TMS pin when the JTAG interface is active. See the JTAGEN bit field in Table 27-2.

FIGURE 4-3: PROGRAM MEMORY MAP FOR dsPIC33EP128GP50X, dsPIC33EP128MC20X/50X AND PIC24EP128GP/MC20X DEVICES



Note: Memory areas are not shown to scale.

REGISTER 8-3: DMAxSTAH: DMA CHANNEL x START ADDRESS REGISTER A (HIGH)

U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
—	—	—	—	—	—	—	—
bit 15							bit 8

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
STA<23:16>							
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 15-8 **Unimplemented:** Read as ‘0’

bit 7-0 **STA<23:16>:** Primary Start Address bits (source or destination)

REGISTER 8-4: DMAxSTAL: DMA CHANNEL x START ADDRESS REGISTER A (LOW)

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
STA<15:8>							
bit 15							bit 8

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
STA<7:0>							
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 15-0 **STA<15:0>:** Primary Start Address bits (source or destination)

11.1.1 OPEN-DRAIN CONFIGURATION

In addition to the PORTx, LATx and TRISx registers for data control, port pins can also be individually configured for either digital or open-drain output. This is controlled by the Open-Drain Control register, ODCx, associated with each port. Setting any of the bits configures the corresponding pin to act as an open-drain output.

The open-drain feature allows the generation of outputs other than VDD by using external pull-up resistors. The maximum open-drain voltage allowed on any pin is the same as the maximum VIH specification for that particular pin.

See the **"Pin Diagrams"** section for the available 5V tolerant pins and Table 30-11 for the maximum VIH specification for each pin.

11.2 Configuring Analog and Digital Port Pins

The ANSELx register controls the operation of the analog port pins. The port pins that are to function as analog inputs or outputs must have their corresponding ANSELx and TRISx bits set. In order to use port pins for I/O functionality with digital modules, such as Timers, UARTs, etc., the corresponding ANSELx bit must be cleared.

The ANSELx register has a default value of 0xFFFF; therefore, all pins that share analog functions are analog (not digital) by default.

Pins with analog functions affected by the ANSELx registers are listed with a buffer type of analog in the Pinout I/O Descriptions (see Table 1-1).

If the TRISx bit is cleared (output) while the ANSELx bit is set, the digital output level (VOH or VOL) is converted by an analog peripheral, such as the ADC module or comparator module.

When the PORTx register is read, all pins configured as analog input channels are read as cleared (a low level).

Pins configured as digital inputs do not convert an analog input. Analog levels on any pin defined as a digital input (including the ANx pins) can cause the input buffer to consume current that exceeds the device specifications.

11.2.1 I/O PORT WRITE/READ TIMING

One instruction cycle is required between a port direction change or port write operation and a read operation of the same port. Typically this instruction would be a NOP, as shown in Example 11-1.

11.3 Input Change Notification (ICN)

The Input Change Notification function of the I/O ports allows devices to generate interrupt requests to the processor in response to a Change-of-State (COS) on selected input pins. This feature can detect input Change-of-States even in Sleep mode, when the clocks are disabled. Every I/O port pin can be selected (enabled) for generating an interrupt request on a Change-of-State.

Three control registers are associated with the Change Notification (CN) functionality of each I/O port. The CNENx registers contain the CN interrupt enable control bits for each of the input pins. Setting any of these bits enables a CN interrupt for the corresponding pins.

Each I/O pin also has a weak pull-up and a weak pull-down connected to it. The pull-ups and pull-downs act as a current source or sink source connected to the pin and eliminate the need for external resistors when push button, or keypad devices are connected. The pull-ups and pull-downs are enabled separately, using the CNPUx and the CNPDx registers, which contain the control bits for each of the pins. Setting any of the control bits enables the weak pull-ups and/or pull-downs for the corresponding pins.

Note:	Pull-ups and pull-downs on Change Notification pins should always be disabled when the port pin is configured as a digital output.

EXAMPLE 11-1: PORT WRITE/READ EXAMPLE

```
MOV   0xFF00, W0   ; Configure PORTB<15:8>
                   ; as inputs
MOV   W0, TRISB    ; and PORTB<7:0>
                   ; as outputs
NOP                ; Delay 1 cycle
BTSS  PORTB, #13   ; Next Instruction
```

TABLE 11-2: INPUT PIN SELECTION FOR SELECTABLE INPUT SOURCES

Peripheral Pin Select Input Register Value	Input/ Output	Pin Assignment	Peripheral Pin Select Input Register Value	Input/ Output	Pin Assignment
000 0000	I	Vss	010 1101	I	RPI45
000 0001	I	C1OUT(1)	010 1110	I	RPI46
000 0010	I	C2OUT(1)	010 1111	I	RPI47
000 0011	I	C3OUT(1)	011 0000	—	—
000 0100	I	C4OUT(1)	011 0001	—	—
000 0101	—	—	011 0010	—	—
000 0110	I	PTGO30(1)	011 0011	I	RPI51
000 0111	I	PTGO31(1)	011 0100	I	RPI52
000 1000	I	FINDX1(1,2)	011 0101	I	RPI53
000 1001	I	FHOME1(1,2)	011 0110	I/O	RP54
000 1010	—	—	011 0111	I/O	RP55
000 1011	—	—	011 1000	I/O	RP56
000 1100	—	—	011 1001	I/O	RP57
000 1101	—	—	011 1010	I	RPI58
000 1110	—	—	011 1011	—	—
000 1111	—	—	011 1100	—	—
001 0000	—	—	011 1101	—	—
001 0001	—	—	011 1110	—	—
001 0010	—	—	011 1111	—	—
001 0011	—	—	100 0000	—	—
001 0100	I/O	RP20	100 0001	—	—
001 0101	—	—	100 0010	—	—
001 0110	—	—	100 0011	—	—
001 0111	—	—	100 0100	—	—
001 1000	I	RPI24	100 0101	—	—
001 1001	I	RPI25	100 0110	—	—
001 1010	—	—	100 0111	—	—
001 1011	I	RPI27	100 1000	—	—
001 1100	I	RPI28	100 1001	—	—
001 1101	—	—	100 1010	—	—
001 1110	—	—	100 1011	—	—
001 1111	—	—	100 1100	—	—
010 0000	I	RPI32	100 1101	—	—
010 0001	I	RPI33	100 1110	—	—
010 0010	I	RPI34	100 1111	—	—
010 0011	I/O	RP35	101 0000	—	—
010 0100	I/O	RP36	101 0001	—	—
010 0101	I/O	RP37	101 0010	—	—
010 0110	I/O	RP38	101 0011	—	—
010 0111	I/O	RP39	101 0100	—	—

Legend: Shaded rows indicate PPS Input register values that are unimplemented.

Note 1: See **Section 11.4.4.1 “Virtual Connections”** for more information on selecting this pin assignment.

2: These inputs are available on dsPIC33EPXXXGP/MC50X devices only.

REGISTER 11-13: RPINR23: PERIPHERAL PIN SELECT INPUT REGISTER 23

U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
—	—	—	—	—	—	—	—
bit 15							bit 8

U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
—	SS2R<6:0>						
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 15-7 **Unimplemented:** Read as ‘0’

bit 6-0 **SS2R<6:0>:** Assign SPI2 Slave Select ($\overline{SS2}$) to the Corresponding RPn Pin bits (see Table 11-2 for input pin selection numbers)

1111001 = Input tied to RPI121
.
.
.
0000001 = Input tied to CMP1
0000000 = Input tied to Vss

REGISTER 11-14: RPINR26: PERIPHERAL PIN SELECT INPUT REGISTER 26 (dsPIC33EPXXXGP/MC50X DEVICES ONLY)

U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
—	—	—	—	—	—	—	—
bit 15							bit 8

U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
—	C1RXR<6:0>						
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 15-7 **Unimplemented:** Read as ‘0’

bit 6-0 **C1RXR<6:0>:** Assign CAN1 RX Input (CRX1) to the Corresponding RPn Pin bits (see Table 11-2 for input pin selection numbers)

1111001 = Input tied to RPI121
.
.
.
0000001 = Input tied to CMP1
0000000 = Input tied to Vss

REGISTER 11-20: RPOR2: PERIPHERAL PIN SELECT OUTPUT REGISTER 2

U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
—	—	RP39R<5:0>					
bit 15							bit 8

U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
—	—	RP38R<5:0>					
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15-14 **Unimplemented:** Read as '0'

bit 13-8 **RP39R<5:0>:** Peripheral Output Function is Assigned to RP39 Output Pin bits (see Table 11-3 for peripheral function numbers)

bit 7-6 **Unimplemented:** Read as '0'

bit 5-0 **RP38R<5:0>:** Peripheral Output Function is Assigned to RP38 Output Pin bits (see Table 11-3 for peripheral function numbers)

REGISTER 11-21: RPOR3: PERIPHERAL PIN SELECT OUTPUT REGISTER 3

U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
—	—	RP41R<5:0>					
bit 15							bit 8

U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
—	—	RP40R<5:0>					
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15-14 **Unimplemented:** Read as '0'

bit 13-8 **RP41R<5:0>:** Peripheral Output Function is Assigned to RP41 Output Pin bits (see Table 11-3 for peripheral function numbers)

bit 7-6 **Unimplemented:** Read as '0'

bit 5-0 **RP40R<5:0>:** Peripheral Output Function is Assigned to RP40 Output Pin bits (see Table 11-3 for peripheral function numbers)

REGISTER 13-2: TyCON: (TIMER3 AND TIMER5) CONTROL REGISTER

R/W-0	U-0	R/W-0	U-0	U-0	U-0	U-0	U-0
TON(1)	—	TSIDL(2)	—	—	—	—	—
bit 15							bit 8

U-0	R/W-0	R/W-0	R/W-0	U-0	U-0	R/W-0	U-0
—	TGATE(1)	TCKPS1(1)	TCKPS0(1)	—	—	TCS(1,3)	—
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15 **TON:** Timery On bit(1)
1 = Starts 16-bit Timery
0 = Stops 16-bit Timery

bit 14 **Unimplemented:** Read as '0'

bit 13 **TSIDL:** Timery Stop in Idle Mode bit(2)
1 = Discontinues module operation when device enters Idle mode
0 = Continues module operation in Idle mode

bit 12-7 **Unimplemented:** Read as '0'

bit 6 **TGATE:** Timery Gated Time Accumulation Enable bit(1)
When TCS = 1:
This bit is ignored.
When TCS = 0:
1 = Gated time accumulation is enabled
0 = Gated time accumulation is disabled

bit 5-4 **TCKPS<1:0>:** Timery Input Clock Prescale Select bits(1)
11 = 1:256
10 = 1:64
01 = 1:8
00 = 1:1

bit 3-2 **Unimplemented:** Read as '0'

bit 1 **TCS:** Timery Clock Source Select bit(1,3)
1 = External clock is from pin, TyCK (on the rising edge)
0 = Internal clock (FP)

bit 0 **Unimplemented:** Read as '0'

Note 1: When 32-bit operation is enabled (T2CON<3> = 1), these bits have no effect on Timery operation; all timer functions are set through TxCON.

2: When 32-bit timer operation is enabled (T32 = 1) in the Timerx Control register (TxCON<3>), the TSIDL bit must be cleared to operate the 32-bit timer in Idle mode.

3: The TyCK pin is not available on all timers. See the **"Pin Diagrams"** section for the available pins.

14.1 Input Capture Resources

Many useful resources are provided on the main product page of the Microchip web site for the devices listed in this data sheet. This product page, which can be accessed using this link, contains the latest updates and additional information.

Note:	In the event you are not able to access the product page using the link above, enter this URL in your browser: http://www.microchip.com/wwwproducts/Devices.aspx?dDocName=en555464

14.1.1 KEY RESOURCES

- **"Input Capture"** (DS70352) in the *"dsPIC33/PIC24 Family Reference Manual"*
- Code Samples
- Application Notes
- Software Libraries
- Webinars
- All Related *"dsPIC33/PIC24 Family Reference Manual"* Sections
- Development Tools

17.0 QUADRATURE ENCODER INTERFACE (QEI) MODULE (dsPIC33EPXXXMC20X/50X and PIC24EPXXXMC20X DEVICES ONLY)

Note 1: This data sheet summarizes the features of the dsPIC33EPXXXGP50X, dsPIC33EPXXXMC20X/50X and PIC24EPXXXGP/MC20X families of devices. It is not intended to be a comprehensive reference source. To complement the information in this data sheet, refer to **"Quadrature Encoder Interface (QEI)"** (DS70601) in the "*dsPIC33/PIC24 Family Reference Manual*", which is available from the Microchip web site (www.microchip.com).

2: Some registers and associated bits described in this section may not be available on all devices. Refer to **Section 4.0 "Memory Organization"** in this data sheet for device-specific register and bit information.

This chapter describes the Quadrature Encoder Interface (QEI) module and associated operational modes. The QEI module provides the interface to incremental encoders for obtaining mechanical position data.

The operational features of the QEI module include:

- 32-Bit Position Counter
- 32-Bit Index Pulse Counter
- 32-Bit Interval Timer
- 16-Bit Velocity Counter
- 32-Bit Position Initialization/Capture/Compare High register
- 32-Bit Position Compare Low register
- x4 Quadrature Count mode
- External Up/Down Count mode
- External Gated Count mode
- External Gated Timer mode
- Internal Timer mode

Figure 17-1 illustrates the QEI block diagram.

REGISTER 21-26: CxTRmnCON: ECANx TX/RX BUFFER mn CONTROL REGISTER (m = 0,2,4,6; n = 1,3,5,7)

R/W-0	R-0	R-0	R-0	R/W-0	R/W-0	R/W-0	R/W-0
TXENn	TXABTn	TXLARBn	TXERRn	TXREQn	RTRENn	TXnPRI1	TXnPRI0
bit 15							bit 8

R/W-0	R-0	R-0	R-0	R/W-0	R/W-0	R/W-0	R/W-0
TXENm	TXABTm(1)	TXLARBm(1)	TXERRm(1)	TXREQm	RTRENm	TXmPRI1	TXmPRI0
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15-8 See Definition for bits<7:0>, Controls Buffer n

bit 7 **TXENm:** TX/RX Buffer Selection bit
1 = Buffer TRBn is a transmit buffer
0 = Buffer TRBn is a receive buffer

bit 6 **TXABTm:** Message Aborted bit(1)
1 = Message was aborted
0 = Message completed transmission successfully

bit 5 **TXLARBm:** Message Lost Arbitration bit(1)
1 = Message lost arbitration while being sent
0 = Message did not lose arbitration while being sent

bit 4 **TXERRm:** Error Detected During Transmission bit(1)
1 = A bus error occurred while the message was being sent
0 = A bus error did not occur while the message was being sent

bit 3 **TXREQm:** Message Send Request bit
1 = Requests that a message be sent; the bit automatically clears when the message is successfully sent
0 = Clearing the bit to '0' while set requests a message abort

bit 2 **RTRENm:** Auto-Remote Transmit Enable bit
1 = When a remote transmit is received, TXREQ will be set
0 = When a remote transmit is received, TXREQ will be unaffected

bit 1-0 **TXmPRI<1:0>:** Message Transmission Priority bits
11 = Highest message priority
10 = High intermediate message priority
01 = Low intermediate message priority
00 = Lowest message priority

Note 1: This bit is cleared when TXREQ is set.

Note: The buffers, SID, EID, DLC, Data Field, and Receive Status registers are located in DMA RAM.

REGISTER 23-2: AD1CON2: ADC1 CONTROL REGISTER 2

R/W-0	R/W-0	R/W-0	U-0	U-0	R/W-0	R/W-0	R/W-0
VCFG2	VCFG1	VCFG0	—	—	CSCNA	CHPS1	CHPS0
bit 15							bit 8

R-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
BUFS	SMPI4	SMPI3	SMPI2	SMPI1	SMPI0	BUFM	ALTS
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15-13 **VCFG<2:0>:** Converter Voltage Reference Configuration bits

Value	VREFH	VREFL
000	AVDD	Avss
001	External VREF+	Avss
010	AVDD	External VREF-
011	External VREF+	External VREF-
1xx	AVDD	AVSS

bit 12-11 **Unimplemented:** Read as '0'

bit 10 **CSCNA:** Input Scan Select bit
1 = Scans inputs for CH0+ during Sample MUXA
0 = Does not scan inputs

bit 9-8 **CHPS<1:0>:** Channel Select bits
In 12-bit mode (AD21B = 1), the CHPS<1:0> bits are Unimplemented and are Read as '0':
1x = Converts CH0, CH1, CH2 and CH3
01 = Converts CH0 and CH1
00 = Converts CH0

bit 7 **BUFS:** Buffer Fill Status bit (only valid when BUFM = 1)
1 = ADC is currently filling the second half of the buffer; the user application should access data in the first half of the buffer
0 = ADC is currently filling the first half of the buffer; the user application should access data in the second half of the buffer

bit 6-2 **SMPI<4:0>:** Increment Rate bits
When ADDMAEN = 0:
x1111 = Generates interrupt after completion of every 16th sample/conversion operation
x1110 = Generates interrupt after completion of every 15th sample/conversion operation
•
•
•
x0001 = Generates interrupt after completion of every 2nd sample/conversion operation
x0000 = Generates interrupt after completion of every sample/conversion operation
When ADDMAEN = 1:
11111 = Increments the DMA address after completion of every 32nd sample/conversion operation
11110 = Increments the DMA address after completion of every 31st sample/conversion operation
•
•
•
00001 = Increments the DMA address after completion of every 2nd sample/conversion operation
00000 = Increments the DMA address after completion of every sample/conversion operation

REGISTER 23-6: AD1CHS0: ADC1 INPUT CHANNEL 0 SELECT REGISTER (CONTINUED)

bit 4-0 **CH0SA<4:0>:** Channel 0 Positive Input Select for Sample MUXA bits(1)

11111 = Open; use this selection with CTMU capacitive and time measurement
11110 = Channel 0 positive input is connected to the CTMU temperature measurement diode (CTMU TEMP)
11101 = Reserved
11100 = Reserved
11011 = Reserved
11010 = Channel 0 positive input is the output of OA3/AN6(2,3)
11001 = Channel 0 positive input is the output of OA2/AN0(2)
11000 = Channel 0 positive input is the output of OA1/AN3(2)
10110 = Reserved
•
•
•
10000 = Reserved
01111 = Channel 0 positive input is AN15(1,3)
01110 = Channel 0 positive input is AN14(1,3)
01101 = Channel 0 positive input is AN13(1,3)
•
•
•
00010 = Channel 0 positive input is AN2(1,3)
00001 = Channel 0 positive input is AN1(1,3)
00000 = Channel 0 positive input is AN0(1,3)

Note 1: AN0 through AN7 are repurposed when comparator and op amp functionality is enabled. See Figure 23-1 to determine how enabling a particular op amp or comparator affects selection choices for Channels 1, 2 and 3.

2: The OAx input is used if the corresponding op amp is selected (OPMODE (CMxCON<10>) = 1); otherwise, the ANx input is used.

3: See the **"Pin Diagrams"** section for the available analog channels for each device.

REGISTER 23-7: AD1CSSH: ADC1 INPUT SCAN SELECT REGISTER HIGH(1)

R/W-0	R/W-0	U-0	U-0	U-0	R/W-0	R/W-0	R/W-0
CSS31	CSS30	—	—	—	CSS26(2)	CSS25(2)	CSS24(2)
bit 15							bit 8

U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
—	—	—	—	—	—	—	—
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15 **CSS31:** ADC1 Input Scan Selection bit
1 = Selects CTMU capacitive and time measurement for input scan (Open)
0 = Skips CTMU capacitive and time measurement for input scan (Open)

bit 14 **CSS30:** ADC1 Input Scan Selection bit
1 = Selects CTMU on-chip temperature measurement for input scan (CTMU TEMP)
0 = Skips CTMU on-chip temperature measurement for input scan (CTMU TEMP)

bit 13-11 **Unimplemented:** Read as '0'

bit 10 **CSS26:** ADC1 Input Scan Selection bit(2)
1 = Selects OA3/AN6 for input scan
0 = Skips OA3/AN6 for input scan

bit 9 **CSS25:** ADC1 Input Scan Selection bit(2)
1 = Selects OA2/AN0 for input scan
0 = Skips OA2/AN0 for input scan

bit 8 **CSS24:** ADC1 Input Scan Selection bit(2)
1 = Selects OA1/AN3 for input scan
0 = Skips OA1/AN3 for input scan

bit 7-0 **Unimplemented:** Read as '0'

Note 1: All AD1CSSH bits can be selected by user software. However, inputs selected for scan, without a corresponding input on the device, convert VREFL.

2: The OAx input is used if the corresponding op amp is selected (OPMODE (CMxCON<10>) = 1); otherwise, the ANx input is used.

REGISTER 24-4: PTGT0LIM: PTG TIMER0 LIMIT REGISTER(1)

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
PTGT0LIM<15:8>							
bit 15							bit 8

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
PTGT0LIM<7:0>							
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15-0 **PTGT0LIM<15:0>:** PTG Timer0 Limit Register bits
General Purpose Timer0 Limit register (effective only with a PTGT0 Step command).

Note 1: This register is read-only when the PTG module is executing Step commands (PTGEN = 1 and PTGSTRT = 1).

REGISTER 24-5: PTGT1LIM: PTG TIMER1 LIMIT REGISTER(1)

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
PTGT1LIM<15:8>							
bit 15							bit 8

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
PTGT1LIM<7:0>							
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15-0 **PTGT1LIM<15:0>:** PTG Timer1 Limit Register bits
General Purpose Timer1 Limit register (effective only with a PTGT1 Step command).

Note 1: This register is read-only when the PTG module is executing Step commands (PTGEN = 1 and PTGSTRT = 1).

TABLE 31-4: DC CHARACTERISTICS: POWER-DOWN CURRENT (I_{PD})

DC CHARACTERISTICS			Standard Operating Conditions: 3.0V to 3.6V (unless otherwise stated) Operating temperature -40°C ≤ TA ≤ +150°C			
Parameter No.	Typical	Max	Units	Conditions		
Power-Down Current (I_{PD})						
HDC60e	1400	2500	μA	+150°C	3.3V	Base Power-Down Current **(Notes 1, 3)**
HDC61c	15	—	μA	+150°C	3.3V	Watchdog Timer Current: ΔI_{WDT} **(Notes 2, 4)**

Note 1: Base I_{PD} is measured with all peripherals and clocks shut down. All I/Os are configured as inputs and pulled to V_{SS}. WDT, etc., are all switched off and VREGS (RCON<8>) = 1.

2: The Δ current is the additional current consumed when the module is enabled. This current should be added to the base I_{PD} current.

3: These currents are measured on the device containing the most memory in this family.

4: These parameters are characterized, but are not tested in manufacturing.

TABLE 31-5: DC CHARACTERISTICS: IDLE CURRENT (I_{IDLE})

DC CHARACTERISTICS			Standard Operating Conditions: 3.0V to 3.6V (unless otherwise stated) Operating temperature -40°C ≤ TA ≤ +150°C			
Parameter No.	Typical	Max	Units	Conditions		
HDC44e	12	30	mA	+150°C	3.3V	40 MIPS

TABLE 31-6: DC CHARACTERISTICS: OPERATING CURRENT (I_{DD})

DC CHARACTERISTICS			Standard Operating Conditions: 3.0V to 3.6V (unless otherwise stated) Operating temperature -40°C ≤ TA ≤ +150°C			
Parameter No.	Typical	Max	Units	Conditions		
HDC20	9	15	mA	+150°C	3.3V	10 MIPS
HDC22	16	25	mA	+150°C	3.3V	20 MIPS
HDC23	30	50	mA	+150°C	3.3V	40 MIPS

TABLE 31-7: DC CHARACTERISTICS: DOZE CURRENT (I_{DOZE})

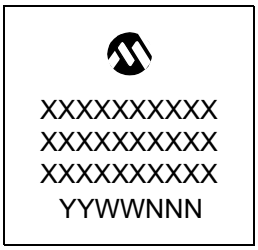
DC CHARACTERISTICS			Standard Operating Conditions: 3.0V to 3.6V (unless otherwise stated) Operating temperature -40°C ≤ TA ≤ +150°C				
Parameter No.	Typical	Max	Doze Ratio	Units	Conditions		
HDC72a	24	35	1:2	mA	+150°C	3.3V	40 MIPS
HDC72f(1)	14	—	1:64	mA			
HDC72g(1)	12	—	1:128	mA			

Note 1: Parameters with Doze ratios of 1:64 and 1:128 are characterized, but are not tested in manufacturing.

NOTES:

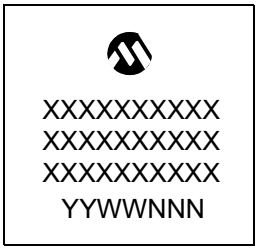
33.1 Package Marking Information (Continued)

36-Lead VTLA (TLA)



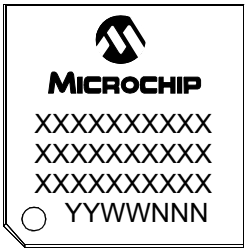
Example

44-Lead VTLA (TLA)



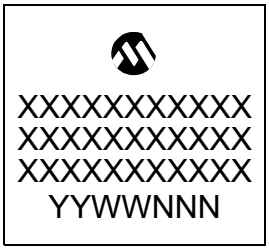
Example

44-Lead TQFP



Example

44-Lead QFN (8x8x0.9 mm)



Example

Revision F (November 2012)

Removed “Preliminary” from data sheet footer.

Revision G (March 2013)

This revision includes the following global changes:

- changes “$\overline{\text{FLTx}}$” pin function to “FLTx” on all occurrences
- adds **Section 31.0 “High-Temperature Electrical Characteristics”** for high-temperature (+150°C) data

This revision also includes minor typographical and formatting changes throughout the text.

Other major changes are referenced by their respective section in Table A-5.

TABLE A-5: MAJOR SECTION UPDATES

Section Name	Update Description
Cover Section	• Changes internal oscillator specification to 1.0% • Changes I/O sink/source values to 12 mA or 6 mA • Corrects 44-pin VTLA pin diagram (pin 32 now shows as 5V tolerant)
Section 4.0 “Memory Organization”	• Deletes references to Configuration Shadow registers • Corrects the spelling of the JTAGIP and PTGWDTIP bits throughout • Corrects the Reset value of all IOCON registers as C000h • Adds footnote to Table 4-42 to indicate the absence of Comparator 3 in 28-pin devices
Section 6.0 “Resets”	• Removes references to cold and warm Resets, and clarifies the initial configuration of the device clock source on all Resets
Section 7.0 “Interrupt Controller”	• Corrects the definition of GIE as “Global Interrupt Enable” (not “General”)
Section 9.0 “Oscillator Configuration”	• Clarifies the behavior of the CF bit when cleared in software • Removes POR behavior footnotes from all control registers • Corrects the tuning range of the TUN<5:0> bits in Register 9-4 to an overall range ±1.5%
Section 13.0 “Timer2/3 and Timer4/5”	• Clarifies the presence of the ADC Trigger in 16-bit Timer3 and Timer5, as well as the 32-bit timers
Section 15.0 “Output Compare”	• Corrects the first trigger source for SYNCSEL<4:0> (OCxCON2<4:0>) as OCxRS match
Section 16.0 “High-Speed PWM Module”	• Clarifies the source of the PWM interrupts in Figure 16-1 • Corrects the Reset states of IOCONx<15:14> in Register 16-13 as ‘11’
Section 17.0 “Quadrature Encoder Interface (QEI) Module”	• Clarifies the operation of the IMV<1:0> bits (QEICON<9:8>) with updated text and additional notes • Corrects the first prescaler value for QFVDIV<2:0> (QEI1OC<13:11>), now 1:128
Section 23.0 “10-Bit/12-Bit Analog-to-Digital Converter (ADC)”	• Adds note to Figure 23-1 that Op Amp 3 is not available in 28-pin devices • Changes “sample clock” to “sample trigger” in AD1CON1 (Register 23-1) • Clarifies footnotes on op amp usage in Registers 23-5 and 23-6
Section 25.0 “Op Amp/ Comparator Module”	• Adds Note text to indicate that Comparator 3 is unavailable in 28-pin devices • Splits Figure 25-1 into two figures for clearer presentation (Figure 25-1 for Op amp/ Comparators 1 through 3, Figure 25-2 for Comparator 4). Subsequent figures are renumbered accordingly. • Corrects reference description in xxxxx (now (AV_{DD} + AV_{SS})/2) • Changes CMSTAT<15> in Register 25-1 to “PSIDL”
Section 27.0 “Special Features”	• Corrects the addresses of all Configuration bytes for 512 Kbyte devices

NOTES: