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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "<u>Embedded -</u> <u>Microcontrollers</u>"

Details

Product Status	Active
Core Processor	PIC
Core Size	16-Bit
Speed	70 MIPs
Connectivity	I ² C, IrDA, LINbus, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, DMA, POR, PWM, WDT
Number of I/O	21
Program Memory Size	128KB (43K x 24)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	8K x 16
Voltage - Supply (Vcc/Vdd)	3V ~ 3.6V
Data Converters	A/D 6x10b/12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	28-SSOP (0.209", 5.30mm Width)
Supplier Device Package	28-SSOP
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/pic24ep128gp202t-i-ss

Email: info@E-XFL.COM

Address: Room A, 16/F, Full Win Commercial Centre, 573 Nathan Road, Mongkok, Hong Kong

3.8 Arithmetic Logic Unit (ALU)

The dsPIC33EPXXXGP50X, dsPIC33EPXXXMC20X/ 50X and PIC24EPXXXGP/MC20X ALU is 16 bits wide, and is capable of addition, subtraction, bit shifts and logic operations. Unless otherwise mentioned, arithmetic operations are two's complement in nature. Depending on the operation, the ALU can affect the values of the Carry (C), Zero (Z), Negative (N), Overflow (OV) and Digit Carry (DC) Status bits in the <u>SR register. The C and DC</u> Status bits operate as Borrow and Digit Borrow bits, respectively, for subtraction operations.

The ALU can perform 8-bit or 16-bit operations, depending on the mode of the instruction that is used. Data for the ALU operation can come from the W register array or data memory, depending on the addressing mode of the instruction. Likewise, output data from the ALU can be written to the W register array or a data memory location.

Refer to the *"16-bit MCU and DSC Programmer's Reference Manual"* (DS70157) for information on the SR bits affected by each instruction.

The core CPU incorporates hardware support for both multiplication and division. This includes a dedicated hardware multiplier and support hardware for 16-bit divisor division.

3.8.1 MULTIPLIER

Using the high-speed 17-bit x 17-bit multiplier, the ALU supports unsigned, signed, or mixed-sign operation in several MCU multiplication modes:

- 16-bit x 16-bit signed
- 16-bit x 16-bit unsigned
- 16-bit signed x 5-bit (literal) unsigned
- 16-bit signed x 16-bit unsigned
- 16-bit unsigned x 5-bit (literal) unsigned
- 16-bit unsigned x 16-bit signed
- 8-bit unsigned x 8-bit unsigned

3.8.2 DIVIDER

The divide block supports 32-bit/16-bit and 16-bit/16-bit signed and unsigned integer divide operations with the following data sizes:

- 32-bit signed/16-bit signed divide
- 32-bit unsigned/16-bit unsigned divide
- 16-bit signed/16-bit signed divide
- 16-bit unsigned/16-bit unsigned divide

The quotient for all divide instructions ends up in W0 and the remainder in W1. The 16-bit signed and unsigned DIV instructions can specify any W register for both the 16-bit divisor (Wn) and any W register (aligned) pair (W(m + 1):Wm) for the 32-bit dividend. The divide algorithm takes one cycle per bit of divisor, so both 32-bit/16-bit and 16-bit/16-bit instructions take the same number of cycles to execute.

3.9 DSP Engine (dsPIC33EPXXXMC20X/50X and dsPIC33EPXXXGP50X Devices Only)

The DSP engine consists of a high-speed 17-bit x 17-bit multiplier, a 40-bit barrel shifter and a 40-bit adder/subtracter (with two target accumulators, round and saturation logic).

The DSP engine can also perform inherent accumulatorto-accumulator operations that require no additional data. These instructions are ADD, SUB and NEG.

The DSP engine has options selected through bits in the CPU Core Control register (CORCON), as listed below:

- Fractional or integer DSP multiply (IF)
- · Signed, unsigned or mixed-sign DSP multiply (US)
- · Conventional or convergent rounding (RND)
- · Automatic saturation on/off for ACCA (SATA)
- Automatic saturation on/off for ACCB (SATB)
- Automatic saturation on/off for writes to data memory (SATDW)
- Accumulator Saturation mode selection (ACCSAT)

SOMMAN							
Instruction	Algebraic Operation	ACC Write Back					
CLR	A = 0	Yes					
ED	$A = (x - y)^2$	No					
EDAC	$A = A + (x - y)^2$	No					
MAC	$A = A + (x \bullet y)$	Yes					
MAC	$A = A + x^2$	No					
MOVSAC	No change in A	Yes					
MPY	$A = x \bullet y$	No					
MPY	$A = x^2$	No					
MPY.N	$A = -x \bullet y$	No					
MSC	$A = A - x \bullet y$	Yes					

TABLE 3-2: DSP INSTRUCTIONS SUMMARY

4.2 Data Address Space

The dsPIC33EPXXXGP50X, dsPIC33EPXXXMC20X/ 50X and PIC24EPXXXGP/MC20X CPU has a separate 16-bit-wide data memory space. The Data Space is accessed using separate Address Generation Units (AGUs) for read and write operations. The data memory maps, which are presented by device family and memory size, are shown in Figure 4-7 through Figure 4-16.

All Effective Addresses (EAs) in the data memory space are 16 bits wide and point to bytes within the Data Space. This arrangement gives a base Data Space address range of 64 Kbytes (32K words).

The base Data Space address is used in conjunction with a Read or Write Page register (DSRPAG or DSWPAG) to form an Extended Data Space, which has a total address range of 16 Mbytes.

dsPIC33EPXXXGP50X, dsPIC33EPXXXMC20X/50X and PIC24EPXXXGP/MC20X devices implement up to 52 Kbytes of data memory (4 Kbytes of data memory for Special Function Registers and up to 48 Kbytes of data memory for RAM). If an EA points to a location outside of this area, an all-zero word or byte is returned.

4.2.1 DATA SPACE WIDTH

The data memory space is organized in byteaddressable, 16-bit-wide blocks. Data is aligned in data memory and registers as 16-bit words, but all Data Space EAs resolve to bytes. The Least Significant Bytes (LSBs) of each word have even addresses, while the Most Significant Bytes (MSBs) have odd addresses.

4.2.2 DATA MEMORY ORGANIZATION AND ALIGNMENT

To maintain backward compatibility with PIC[®] MCU devices and improve Data Space memory usage efficiency, the dsPIC33EPXXXGP50X, dsPIC33EPXXXMC20X/50X and PIC24EPXXXGP/ MC20X instruction set supports both word and byte operations. As a consequence of byte accessibility, all Effective Address calculations are internally scaled to step through word-aligned memory. For example, the core recognizes that Post-Modified Register Indirect Addressing mode [Ws++] results in a value of Ws + 1 for byte operations and Ws + 2 for word operations.

A data byte read, reads the complete word that contains the byte, using the LSb of any EA to determine which byte to select. The selected byte is placed onto the LSB of the data path. That is, data memory and registers are organized as two parallel, byte-wide entities with shared (word) address decode but separate write lines. Data byte writes only write to the corresponding side of the array or register that matches the byte address. All word accesses must be aligned to an even address. Misaligned word data fetches are not supported, so care must be taken when mixing byte and word operations, or translating from 8-bit MCU code. If a misaligned read or write is attempted, an address error trap is generated. If the error occurred on a read, the instruction underway is completed. If the error occurred on a write, the instruction is executed but the write does not occur. In either case, a trap is then executed, allowing the system and/or user application to examine the machine state prior to execution of the address Fault.

All byte loads into any W register are loaded into the LSB. The MSB is not modified.

A Sign-Extend (SE) instruction is provided to allow user applications to translate 8-bit signed data to 16-bit signed values. Alternatively, for 16-bit unsigned data, user applications can clear the MSB of any W register by executing a Zero-Extend (ZE) instruction on the appropriate address.

4.2.3 SFR SPACE

The first 4 Kbytes of the Near Data Space, from 0x0000 to 0x0FFF, is primarily occupied by Special Function Registers (SFRs). These are used by the dsPIC33EPXXXGP50X, dsPIC33EPXXXMC20X/50X and PIC24EPXXXGP/MC20X core and peripheral modules for controlling the operation of the device.

SFRs are distributed among the modules that they control and are generally grouped together by module. Much of the SFR space contains unused addresses; these are read as '0'.

Note: The actual set of peripheral features and interrupts varies by the device. Refer to the corresponding device tables and pinout diagrams for device-specific information.

4.2.4 NEAR DATA SPACE

The 8-Kbyte area, between 0x0000 and 0x1FFF, is referred to as the Near Data Space. Locations in this space are directly addressable through a 13-bit absolute address field within all memory direct instructions. Additionally, the whole Data Space is addressable using MOV instructions, which support Memory Direct Addressing mode with a 16-bit address field, or by using Indirect Addressing mode using a working register as an Address Pointer.





5.2 RTSP Operation

RTSP allows the user application to erase a single page of memory and to program two instruction words at a time. See the General Purpose and Motor Control Family tables (Table 1 and Table 2, respectively) for the page sizes of each device.

For more information on erasing and programming Flash memory, refer to "Flash Programming" (DS70609) in the "dsPIC33/PIC24 Family Reference Manual".

5.3 **Programming Operations**

A complete programming sequence is necessary for programming or erasing the internal Flash in RTSP mode. The processor stalls (waits) until the programming operation is finished.

For erase and program times, refer to Parameters D137a and D137b (Page Erase Time), and D138a and D138b (Word Write Cycle Time) in Table 30-14 in **Section 30.0 "Electrical Characteristics"**.

Setting the WR bit (NVMCON<15>) starts the operation and the WR bit is automatically cleared when the operation is finished.

5.3.1 PROGRAMMING ALGORITHM FOR FLASH PROGRAM MEMORY

Programmers can program two adjacent words (24 bits x 2) of program Flash memory at a time on every other word address boundary (0x000002, 0x000006, 0x00000A, etc.). To do this, it is necessary to erase the page that contains the desired address of the location the user wants to change.

For protection against accidental operations, the write initiate sequence for NVMKEY must be used to allow any erase or program operation to proceed. After the programming command has been executed, the user application must wait for the programming time until programming is complete. The two instructions following the start of the programming sequence should be NOPS.

Refer to **Flash Programming**" (DS70609) in the "*dsPIC33/PIC24 Family Reference Manual*" for details and codes examples on programming using RTSP.

5.4 Flash Memory Resources

Many useful resources are provided on the main product page of the Microchip web site for the devices listed in this data sheet. This product page, which can be accessed using this link, contains the latest updates and additional information.

Note:	In the event you are not able to access the
	product page using the link above, enter
	this URL in your browser:
	http://www.microchip.com/wwwproducts/
	Devices.aspx?dDocName=en555464

5.4.1 KEY RESOURCES

- "Flash Programming" (DS70609) in the "dsPIC33/PIC24 Family Reference Manual"
- Code Samples
- Application Notes
- Software Libraries
- Webinars
- All Related "dsPIC33/PIC24 Family Reference Manual" Sections
- Development Tools

5.5 Control Registers

Four SFRs are used to erase and write the program Flash memory: NVMCON, NVMKEY, NVMADRH and NVMADRL.

The NVMCON register (Register 5-1) enables and initiates Flash memory erase and write operations.

NVMKEY (Register 5-4) is a write-only register that is used for write protection. To start a programming or erase sequence, the user application must consecutively write 0x55 and 0xAA to the NVMKEY register.

There are two NVM Address registers: NVMADRH and NVMADRL. These two registers, when concatenated, form the 24-bit Effective Address (EA) of the selected word for programming operations or the selected page for erase operations.

The NVMADRH register is used to hold the upper 8 bits of the EA, while the NVMADRL register is used to hold the lower 16 bits of the EA.

Oscillator Mode	Oscillator Source	POSCMD<1:0>	FNOSC<2:0>	See Notes
Fast RC Oscillator with Divide-by-N (FRCDIVN)	Internal	xx	111	1, 2
Fast RC Oscillator with Divide-by-16 (FRCDIV16)	Internal	xx	110	1
Low-Power RC Oscillator (LPRC)	Internal	xx	101	1
Primary Oscillator (HS) with PLL (HSPLL)	Primary	10	011	
Primary Oscillator (XT) with PLL (XTPLL)	Primary	01	011	
Primary Oscillator (EC) with PLL (ECPLL)	Primary	0.0	011	1
Primary Oscillator (HS)	Primary	10	010	
Primary Oscillator (XT)	Primary	01	010	
Primary Oscillator (EC)	Primary	00	010	1
Fast RC Oscillator (FRC) with Divide-by-N and PLL (FRCPLL)	Internal	xx	001	1
Fast RC Oscillator (FRC)	Internal	xx	000	1

TABLE 9-1: CONFIGURATION BIT VALUES FOR CLOCK SELECTION

Note 1: OSC2 pin function is determined by the OSCIOFNC Configuration bit.

2: This is the default oscillator mode for an unprogrammed (erased) device.

9.2 Oscillator Resources

Many useful resources are provided on the main product page of the Microchip web site for the devices listed in this data sheet. This product page, which can be accessed using this link, contains the latest updates and additional information.

Note:	In the event you are not able to access the
	product page using the link above, enter
	this URL in your browser:
	http://www.microchip.com/wwwproducts/
	Devices.aspx?dDocName=en555464

9.2.1 KEY RESOURCES

- "Oscillator" (DS70580) in the "dsPIC33/PIC24 Family Reference Manual"
- Code Samples
- Application Notes
- Software Libraries
- Webinars
- All Related *"dsPIC33/PIC24 Family Reference Manual"* Sections
- · Development Tools

dsPIC33EPXXXGP50X, dsPIC33EPXXXMC20X/50X AND PIC24EPXXXGP/MC20X

INE OID LEN	ALGISTER 10-3. TIMDS. TERRI HERAE MODOLE DIGABLE CONTROL REGISTER 3						
U-0	U-0	U-0	U-0	U-0	R/W-0	U-0	U-0
	—	—	—	—	CMPMD	—	—
bit 15							bit 8
R/W-0	U-0	U-0	U-0	U-0	U-0	R/W-0	U-0
CRCMD	—	—	—	—	—	I2C2MD	—
bit 7		•				•	bit 0
Legend:							
R = Readable bit W = Writable bit		bit	U = Unimplemented bit, read as '0'				
-n = Value at POR '1' = Bit is set		'0' = Bit is cleared x = Bit is unknown			iown		
bit 15-11	Unimplement	ted: Read as 'o)'				

REGISTER 10-3: PMD3: PERIPHERAL MODULE DISABLE CONTROL REGISTER 3

bit 10	CMPMD: Comparator Module Disable bit
	1 = Comparator module is disabled
	0 = Comparator module is enabled
bit 9-8	Unimplemented: Read as '0'
bit 7	CRCMD: CRC Module Disable bit
	1 = CRC module is disabled
	0 = CRC module is enabled
bit 6-2	Unimplemented: Read as '0'
bit 1	I2C2MD: I2C2 Module Disable bit
	1 = I2C2 module is disabled
	0 = I2C2 module is enabled
bit 0	Unimplemented: Read as '0'

REGISTER 10-4: PMD4: PERIPHERAL MODULE DISABLE CONTROL REGISTER 4

U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—		—	—
						bit 8
U-0	U-0	U-0	R/W-0	R/W-0	U-0	U-0
	—	—	REFOMD	CTMUMD	—	—
		•	•			bit 0
	U-0 — U-0 —	U-0 U-0 — — U-0 U-0 — —	U-0 U-0 U-0 — — — — U-0 U-0 U-0 — — — —	U-0 U-0 U-0 U-0 	U-0 U-0 U-0 U-0 - - - - - U-0 U-0 U-0 U-0 - U-0 U-0 U-0 R/W-0 R/W-0 - - - REFOMD CTMUMD	U-0 U-0 U-0 U-0 U-0 - - - - - - U-0 U-0 U-0 U-0 U-0 - U-0 U-0 U-0 R/W-0 U-0 - U-0 U-0 R/W-0 R/W-0 U-0 - - - REFOMD CTMUMD -

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read	1 as '0'
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15-4	Unimplemented: Read as '0'
bit 3	REFOMD: Reference Clock Module Disable bit
	1 = Reference clock module is disabled
	0 = Reference clock module is enabled
bit 2	CTMUMD: CTMU Module Disable bit
	1 = CTMU module is disabled
	0 = CTMU module is enabled
bit 1-0	Unimplemented: Read as '0'

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11.4 Peripheral Pin Select (PPS)

A major challenge in general purpose devices is providing the largest possible set of peripheral features while minimizing the conflict of features on I/O pins. The challenge is even greater on low pin count devices. In an application where more than one peripheral needs to be assigned to a single pin, inconvenient workarounds in application code, or a complete redesign, may be the only option.

Peripheral Pin Select configuration provides an alternative to these choices by enabling peripheral set selection and their placement on a wide range of I/O pins. By increasing the pinout options available on a particular device, users can better tailor the device to their entire application, rather than trimming the application to fit the device.

The Peripheral Pin Select configuration feature operates over a fixed subset of digital I/O pins. Users may independently map the input and/or output of most digital peripherals to any one of these I/O pins. Hardware safeguards are included that prevent accidental or spurious changes to the peripheral mapping once it has been established.

11.4.1 AVAILABLE PINS

The number of available pins is dependent on the particular device and its pin count. Pins that support the Peripheral Pin Select feature include the label, "RPn" or "RPIn", in their full pin designation, where "n" is the remappable pin number. "RP" is used to designate pins that support both remappable input and output functions, while "RPI" indicates pins that support remappable input functions only.

11.4.2 AVAILABLE PERIPHERALS

The peripherals managed by the Peripheral Pin Select are all digital-only peripherals. These include general serial communications (UART and SPI), general purpose timer clock inputs, timer-related peripherals (input capture and output compare) and interrupt-on-change inputs. In comparison, some digital-only peripheral modules are never included in the Peripheral Pin Select feature. This is because the peripheral's function requires special I/O circuitry on a specific port and cannot be easily connected to multiple pins. These modules include I^2C^{TM} and the PWM. A similar requirement excludes all modules with analog inputs, such as the ADC Converter.

A key difference between remappable and nonremappable peripherals is that remappable peripherals are not associated with a default I/O pin. The peripheral must always be assigned to a specific I/O pin before it can be used. In contrast, non-remappable peripherals are always available on a default pin, assuming that the peripheral is active and not conflicting with another peripheral.

When a remappable peripheral is active on a given I/O pin, it takes priority over all other digital I/O and digital communication peripherals associated with the pin. Priority is given regardless of the type of peripheral that is mapped. Remappable peripherals never take priority over any analog functions associated with the pin.

11.4.3 CONTROLLING PERIPHERAL PIN SELECT

Peripheral Pin Select features are controlled through two sets of SFRs: one to map peripheral inputs and one to map outputs. Because they are separately controlled, a particular peripheral's input and output (if the peripheral has both) can be placed on any selectable function pin without constraint.

The association of a peripheral to a peripheralselectable pin is handled in two different ways, depending on whether an input or output is being mapped.

dsPIC33EPXXXGP50X, dsPIC33EPXXXMC20X/50X AND PIC24EPXXXGP/MC20X

U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
—	—	-	_	_	—	_	—
bit 15							bit 8
U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
—				OCFAR<6:0>	>		
bit 7	-						bit 0
Legend:							

REGISTER 11-6: RPINR11: PERIPHERAL PIN SELECT INPUT REGISTER 11

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read	l as '0'
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15-7 Unimplemented: Read as '0'

bit 6-0 OCFAR<6:0>: Assign Output Compare Fault A (OCFA) to the Corresponding RPn Pin bits (see Table 11-2 for input pin selection numbers) 1111001 = Input tied to RPI121

> . 0000001 = Input tied to CMP1 0000000 = Input tied to Vss

R/W-0	U-0	U-0	U-0	U-0	U-0	R/W-0	R/W-0
CHPCLKEN	—	—	—	_	—	CHOPC	LK<9:8>
bit 15							bit 8
R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
			CHOPC	LK<7:0>			
bit 7							bit 0
Legend:							
R = Readable I	oit	W = Writable	bit	U = Unimple	mented bit, read	as '0'	
-n = Value at P	OR	'1' = Bit is set		'0' = Bit is cle	eared	x = Bit is unki	nown
bit 15 bit 14-10 bit 9-0	CHPCLKEN: 1 = Chop cloc 0 = Chop cloc Unimplemen CHOPCLK<9 The frequenc Chop Frequen	Enable Chop ck generator is ck generator is ited: Read as 9:0>: Chop Clo cy of the chop c ncy = (FP/PCL	Clock Genera enabled disabled o' ock Divider bits clock signal is KDIV<2:0)/(Cl	tor bit given by the fc HOPCLK<9:0>	llowing expressi + 1)	on:	

REGISTER 16-5: CHOP: PWMx CHOP CLOCK GENERATOR REGISTER

REGISTER 16-6: MDC: PWMx MASTER DUTY CYCLE REGISTER

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
			MDC	<15:8>			
bit 15							bit 8
R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
			MDO	C<7:0>			
bit 7							bit 0
Legend:							
R = Readable	bit	W = Writable	bit	U = Unimpler	mented bit, rea	ad as '0'	
-n = Value at F	POR	'1' = Bit is set		'0' = Bit is cle	ared	x = Bit is unki	nown

bit 15-0 MDC<15:0>: PWMx Master Duty Cycle Value bits

21.2 Modes of Operation

The ECAN module can operate in one of several operation modes selected by the user. These modes include:

- · Initialization mode
- Disable mode
- Normal Operation mode
- · Listen Only mode
- Listen All Messages mode
- Loopback mode

Modes are requested by setting the REQOP<2:0> bits (CxCTRL1<10:8>). Entry into a mode is Acknowledged by monitoring the OPMODE<2:0> bits (CxCTRL1<7:5>). The module does not change the mode and the OPMODEx bits until a change in mode is acceptable, generally during bus Idle time, which is defined as at least 11 consecutive recessive bits.

21.3 ECAN Resources

Many useful resources are provided on the main product page of the Microchip web site for the devices listed in this data sheet. This product page, which can be accessed using this link, contains the latest updates and additional information.

Note:	In the event you are not able to access the
	product page using the link above, enter
	this URL in your browser:
	http://www.microchip.com/wwwproducts/
	Devices.aspx?dDocName=en555464

21.3.1 KEY RESOURCES

- "Enhanced Controller Area Network (ECAN™)" (DS70353) in the "dsPIC33/PIC24 Family Reference Manual"
- · Code Samples
- Application Notes
- Software Libraries
- Webinars
- All Related *"dsPIC33/PIC24 Family Reference Manual"* Sections
- · Development Tools

23.4 ADC Control Registers

REGISTER 23-1: AD1CON1: ADC1 CONTROL REGISTER 1

R/W-0	U-0	R/W-0	R/W-0	U-0	R/W-0	R/W-0	R/W-0				
ADON	—	ADSIDL	ADDMABM	—	AD12B	FORM1	FORM0				
bit 15	bit 15 bit 8										
R/W-0	R/W-0 R/W-0 R/W-0 R/W-0 R/W-0, HC, HS R/C-0, HC, I										
SSRC2	SSRC1	SSRC0	SSRCG	SIMSAM	ASAM	SAMP	DONE ⁽³⁾				
bit 7							bit 0				
Legend:		HC = Hardwa	re Clearable bit	HS = Hardwa	re Settable bit	C = Clearable bi	t				
R = Readab	le bit	W = Writable I	bit	U = Unimpler	nented bit, read	d as '0'					
-n = Value at	t POR	'1' = Bit is set		'0' = Bit is clea	ared	x = Bit is unknow	vn				
bit 15	ADON: ADO	C1 Operating N	lode bit								
	1 = ADC mo	odule is operati	ng								
	0 = ADC is	off									
bit 14	Unimpleme	ented: Read as	'0'								
bit 13	ADSIDL: AI	DC1 Stop in Idle	e Mode bit								
	1 = Disconti	inues module o	peration when	device enters	Idle mode						
	0 = Continu	es module ope	ration in Idle mo	ode							
bit 12	ADDMABM	: DMA Buffer E	Build Mode bit								
	1 = DMA b	uffers are writte	en in the order	of conversion	; the module p	provides an addre	ess to the DMA				
	0 = DMA bi	uffers are writte	en in Scatter/Ga	ther mode: the	e module prov	ides a Scatter/Ga	ther address to				
	the DM	A channel, bas	ed on the index	of the analog	input and the	size of the DMA	ouffer.				
bit 11	Unimpleme	ented: Read as	'0'								
bit 10	AD12B: AD	C1 10-Bit or 12	2-Bit Operation	Mode bit							
	1 = 12-bit, 1	-channel ADC	operation								
	0 = 10-bit, 4	-channel ADC	operation								
bit 9-8	FORM<1:0	>: Data Output	Format bits								
	For 10-Bit C	Operation:									
	11 = Signed	d fractional (Do	UT = sddd ddd	ld dd00 000	0, where $s = $.	NOT.d<9>)					
	10 = Fractions	hai (DOUT = ac	iaa aaaa aau = cccc cccd		where $c = N($	(<0>b TC					
	00 = Intege	r (Dout = 0000	00dd dddd	dddd)		51.u (0 ²)					
	For 12-Bit C	Deration:		,							
	11 = Signed	fractional (Do	UT = sddd ddd	ld dddd 000	0, where $s = .$	NOT.d<11>)					
	10 = Fractic	onal (Dout = do	ldd dddd ddd	ld 0000)							
	00 = Intege	r (DOUT = 0.000)	- ssss sada) dddd dddd	aaaa aaad, dddd)	where $s = .NC$	JI.U<112)					
		. (2001 - 0000		adduj							
Note 1: S	See Section 24	1.0 "Peripheral	l Trigger Gene	rator (PTG) M	odule" for info	ormation on this s	election.				

- 2: This setting is available in dsPIC33EPXXXMC20X/50X and PIC24EPXXXMC20X devices only.
- 3: Do not clear the DONE bit in software if Auto-Sample is enabled (ASAM = 1).

dsPIC33EPXXXGP50X, dsPIC33EPXXXMC20X/50X AND PIC24EPXXXGP/MC20X

R/W-0	R/W	-0	R/W-0	U-0	U-0	R/W-0	R/W-0	R/W-0
VCFG2	VCFC	G1	VCFG0		_	CSCNA	CHPS1	CHPS0
bit 15								bit 8
R-0	R/W	-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
BUFS	SMP	14	SMPI3	SMPI2	SMPI1	SMPI0	BUFM	ALTS
bit 7								bit 0
Legend:								
R = Readable	e bit		W = Writable	bit	U = Unimpl	emented bit, read	d as '0'	
-n = Value at	POR		'1' = Bit is set		'0' = Bit is c	cleared	x = Bit is unk	nown
bit 15-13	VCFG<	2:0>:	Converter Volt	age Reference	Configuratio	on bits		
	Value		VREFH	VREFL				
	000		Avdd	Avss				
	001	Ext	ernal VREF+	Avss				
	010		Avdd	External VRE	F-			
	011	Ext	ernal VREF+	External VRE	F-			
	lxx		Avdd	Avss				
bit 12-11	Unimple	emen	ted: Read as '	0'				
bit 10	CSCNA	: Inpu	t Scan Select	bit				
	1 = Sca 0 = Doe	ns inp s not	outs for CH0+ o scan inputs	luring Sample N	<i>I</i> UXA			
bit 9-8	CHPS<	1:0>:	Channel Selec	t bits				
	<u>In 12-bit</u>	tmode	e (AD21B = 1)	, the CHPS<1:0	> bits are U	nimplemented ar	nd are Read as	<u>'0':</u>
	1x = Co 01 = Co 00 = Co	onverts onverts onverts	s CH0, CH1, C s CH0 and CH s CH0	H2 and CH3 1				
bit 7	BUFS:	Buffer	Fill Status bit	onlv valid wher	BUFM = 1)		
	1 = AD	C is cı	urrently filling t	ne second half c	of the buffer;	the user applicat	ion should acc	ess data in the
	first 0 = AD sec	t half o C is c ond h	of the buffer urrently filling alf of the buffe	the first half of t r	the buffer; tl	ne user applicatio	on should acce	ess data in the
bit 6-2	SMPI<4	: 0>:	ncrement Rate	bits				
	When A	DDM/	AEN = 0:					
	x1111 =	= Gen	erates interrup	t after completion	on of every	16th sample/conv	ersion operation	on
	x1110 =	= Gen	erates interrup	t after completion	on of every	15th sample/conv	ersion operation	on
	•							
	•							
	x0001 = x0000 =	= Gen = Gen	erates interrup erates interrup	t after completion t after completion	on of every 2 on of every 3	2nd sample/conv sample/conversic	ersion operation	n
	When A	DDM/	AEN = 1:					
	11111 =	= Incre	ements the DM	IA address after	completion	of every 32nd sa	ample/conversi	ion operation
	11110 =	= Incre	ements the DM	IA address after	r completion	of every 31st sa	mple/conversion	on operation
	•							
	•							
	00001 = 00000 =	= Incre = Incre	ements the DM ements the DM	IA address aftei IA address aftei	^r completion ^r completion	of every 2nd sar	nple/conversio /conversion op	n operation eration

. . ACOND. ADCA CONTROL DECISTED 2

bit 3-0	Step Command	OPTION<3:0>	Option Description						
	PTGWHI(1)	0000	PWM Special Event Trigger. ⁽³⁾						
	or	0001	PWM master time base synchronization output. ⁽³⁾						
	P.I.GWLO(''	0010	PWM1 interrupt. ⁽³⁾						
		0011	PWM2 interrupt. ⁽³⁾						
		0100	PWM3 interrupt. ⁽³⁾						
		0101	Reserved.						
		0110	Reserved.						
		0111	OC1 Trigger event.						
		1000	OC2 Trigger event.						
		1001	IC1 Trigger event.						
		1010	CMP1 Trigger event.						
		1011	CMP2 Trigger event.						
		1100	CMP3 Trigger event.						
		1101	CMP4 Trigger event.						
		1110	ADC conversion done interrupt.						
		1111	INT2 external interrupt.						
	PTGIRQ(1)	0000	Generate PTG Interrupt 0.						
		0001	Generate PTG Interrupt 1.						
		0010	Generate PTG Interrupt 2.						
		0011	Generate PTG Interrupt 3.						
		0100	Reserved.						
		•	•						
		•	•						
		•	•						
	(2)	1111	Reserved.						
	PTGTRIG ⁽²⁾	00000	PTGO0.						
		00001	PTGO1.						
		•	•						
		•	•						
		•							
		11110	PTGO30.						
		11111	PTGO31.						

TABLE 24-1: PTG STEP COMMAND FORMAT (CONTINUED)

Note 1: All reserved commands or options will execute but have no effect (i.e., execute as a NOP instruction).

2: Refer to Table 24-2 for the trigger output descriptions.

3: This feature is only available on dsPIC33EPXXXMC20X/50X and PIC24EPXXXMC20X devices.

REGISTER 25-3: CM4CON: COMPARATOR 4 CONTROL REGISTER (CONTINUED)

- bit 5 Unimplemented: Read as '0'
- bit 4 **CREF:** Comparator Reference Select bit (VIN+ input)⁽¹⁾
 - 1 = VIN+ input connects to internal CVREFIN voltage
 - 0 = VIN+ input connects to C4IN1+ pin
- bit 3-2 Unimplemented: Read as '0'
- bit 1-0 CCH<1:0>: Comparator Channel Select bits⁽¹⁾
 - 11 = VIN- input of comparator connects to OA3/AN6
 - 10 = VIN- input of comparator connects to OA2/AN0
 - 01 = VIN- input of comparator connects to OA1/AN3
 - 00 = VIN- input of comparator connects to C4IN1-
- Note 1: Inputs that are selected and not available will be tied to Vss. See the "Pin Diagrams" section for available inputs for each package.

NOTES:

Field	Description
Wm,Wn	Dividend, Divisor working register pair (direct addressing)
Wm*Wm	Multiplicand and Multiplier working register pair for Square instructions ∈ {W4 * W4,W5 * W5,W6 * W6,W7 * W7}
Wm*Wn	Multiplicand and Multiplier working register pair for DSP instructions ∈ {W4 * W5,W4 * W6,W4 * W7,W5 * W6,W5 * W7,W6 * W7}
Wn	One of 16 working registers ∈ {W0W15}
Wnd	One of 16 destination working registers ∈ {W0W15}
Wns	One of 16 source working registers ∈ {W0W15}
WREG	W0 (working register used in file register instructions)
Ws	Source W register ∈ { Ws, [Ws], [Ws++], [Ws], [++Ws], [Ws] }
Wso	Source W register ∈ { Wns, [Wns], [Wns++], [Wns], [++Wns], [Wns], [Wns+Wb] }
Wx	X Data Space Prefetch Address register for DSP instructions ∈ {[W8] + = 6, [W8] + = 4, [W8] + = 2, [W8], [W8] - = 6, [W8] - = 4, [W8] - = 2, [W9] + = 6, [W9] + = 4, [W9] + = 2, [W9], [W9] - = 6, [W9] - = 4, [W9] - = 2, [W9 + W12], none}
Wxd	X Data Space Prefetch Destination register for DSP instructions ∈ {W4W7}
Wy	Y Data Space Prefetch Address register for DSP instructions ∈ {[W10] + = 6, [W10] + = 4, [W10] + = 2, [W10], [W10] - = 6, [W10] - = 4, [W10] - = 2, [W11] + = 6, [W11] + = 4, [W11] + = 2, [W11], [W11] - = 6, [W11] - = 4, [W11] - = 2, [W11 + W12], none}
Wyd	Y Data Space Prefetch Destination register for DSP instructions ∈ {W4W7}

TABLE 28-1:	SYMBOLS USED IN OPCODE DESCRIPTIONS ((CONTINUED)

DC CHARACTERISTICS			$\begin{array}{l} \mbox{Standard Operating Conditions: 3.0V to 3.6V} \\ \mbox{(unless otherwise stated)} \\ \mbox{Operating temperature} & -40^{\circ}C \leq TA \leq +85^{\circ}C \mbox{ for Industrial} \\ & -40^{\circ}C \leq TA \leq +125^{\circ}C \mbox{ for Extended} \end{array}$					
Param No.	Symbol	Characteristic	Min.	Min. Typ. ⁽¹⁾ Max. Units Conditions				
		Program Flash Memory						
D130	Eр	Cell Endurance	10,000		_	E/W	-40°C to +125°C	
D131	Vpr	VDD for Read	3.0		3.6	V		
D132b	VPEW	VDD for Self-Timed Write	3.0		3.6	V		
D134	TRETD	Characteristic Retention	20	—	—	Year	Provided no other specifications are violated, -40°C to +125°C	
D135	IDDP	Supply Current during Programming ⁽²⁾	—	10	—	mA		
D136	IPEAK	Instantaneous Peak Current During Start-up	_	_	150	mA		
D137a	Тре	Page Erase Time	17.7	—	22.9	ms	TPE = 146893 FRC cycles, Ta = +85°C (See Note 3)	
D137b	Тре	Page Erase Time	17.5	_	23.1	ms	TPE = 146893 FRC cycles, TA = +125°C (See Note 3)	
D138a	Tww	Word Write Cycle Time	41.7	_	53.8	μs	Tww = 346 FRC cycles, TA = +85°C (See Note 3)	
D138b	Tww	Word Write Cycle Time	41.2	—	54.4	μs	Tww = 346 FRC cycles, Ta = +125°C (See Note 3)	

TABLE 30-14: DC CHARACTERISTICS: PROGRAM MEMORY

Note 1: Data in "Typical" column is at 3.3V, +25°C unless otherwise stated.

2: Parameter characterized but not tested in manufacturing.

3: Other conditions: FRC = 7.37 MHz, TUN<5:0> = 011111 (for Minimum), TUN<5:0> = 100000 (for Maximum). This parameter depends on the FRC accuracy (see Table 30-19) and the value of the FRC Oscillator Tuning register (see Register 9-4). For complete details on calculating the Minimum and Maximum time, see Section 5.3 "Programming Operations".

FIGURE 30-7: OUTPUT COMPARE x MODULE (OCx) TIMING CHARACTERISTICS



TABLE 30-27: OUTPUT COMPARE x MODULE TIMING REQUIREMENTS

AC CHARACTERISTICS			$\begin{array}{l} \mbox{Standard Operating Conditions: 3.0V to 3.6V} \\ \mbox{(unless otherwise stated)} \\ \mbox{Operating temperature} & -40^{\circ}C \leq TA \leq +85^{\circ}C \mbox{ for Industrial} \\ -40^{\circ}C \leq TA \leq +125^{\circ}C \mbox{ for Extended} \end{array}$					
Param No.	Symbol	Characteristic ⁽¹⁾	Min. Typ. Max. Units Conditions					
OC10	TccF	OCx Output Fall Time	—			ns	See Parameter DO32	
OC11	TccR	OCx Output Rise Time	—	—	—	ns	See Parameter DO31	

Note 1: These parameters are characterized but not tested in manufacturing.

FIGURE 30-8: OCx/PWMx MODULE TIMING CHARACTERISTICS



TABLE 30-28: OCx/PWMx MODE TIMING REQUIREMENTS

AC CHARACTERISTICS			Standard Operating Conditions: 3.0V to 3.6V(unless otherwise stated)Operating temperature $-40^{\circ}C \le TA \le +85^{\circ}C$ for Industrial $-40^{\circ}C \le TA \le +125^{\circ}C$ for Extended					
Param No.	Symbol	Characteristic ⁽¹⁾	Min. Typ. Max. Units Conditions					
OC15	TFD	Fault Input to PWMx I/O Change	—	_	Tcy + 20	ns		
OC20	TFLT	Fault Input Pulse Width	Tcy + 20	_	—	ns		

Note 1: These parameters are characterized but not tested in manufacturing.



FIGURE 30-12: QEA/QEB INPUT CHARACTERISTICS (dsPIC33EPXXXMC20X/50X and PIC24EPXXXMC20X DEVICES ONLY)

TABLE 30-31: QUADRATURE DECODER TIMING REQUIREMENTS (dsPIC33EPXXXMC20X/50X and PIC24EPXXXMC20X DEVICES ONLY)

AC CHARACTERISTICS			$\begin{array}{l} \mbox{Standard Operating Conditions: 3.0V to 3.6V} \\ \mbox{(unless otherwise stated)} \\ \mbox{Operating temperature} & -40^{\circ}C \leq TA \leq +85^{\circ}C \mbox{ for Industrial} \\ & -40^{\circ}C \leq TA \leq +125^{\circ}C \mbox{ for Extended} \end{array}$			
Param No.	Symbol	Characteristic ⁽¹⁾	Тур. ⁽²⁾	Max.	Units	Conditions
TQ30	TQUL	Quadrature Input Low Time	6 Tcy		ns	
TQ31	ΤουΗ	Quadrature Input High Time	6 Tcy	—	ns	
TQ35	ΤουΙΝ	Quadrature Input Period	12 Tcy	—	ns	
TQ36	TQUP	Quadrature Phase Period	3 TCY	—	ns	
TQ40	TQUFL	Filter Time to Recognize Low, with Digital Filter	3 * N * Tcy	—	ns	N = 1, 2, 4, 16, 32, 64, 128 and 256 (Note 3)
TQ41	TQUFH	Filter Time to Recognize High, with Digital Filter	3 * N * Tcy		ns	N = 1, 2, 4, 16, 32, 64, 128 and 256 (Note 3)

Note 1: These parameters are characterized but not tested in manufacturing.

2: Data in "Typical" column is at 3.3V, +25°C unless otherwise stated. Parameters are for design guidance only and are not tested.

3: N = Index Channel Digital Filter Clock Divide Select bits. Refer to "Quadrature Encoder Interface (QEI)" (DS70601) in the "*dsPIC33/PIC24 Family Reference Manual*". Please see the Microchip web site for the latest family reference manual sections.

AC CHARACTERISTICS				$\begin{array}{l} \mbox{Standard Operating Conditions: 3.0V to 3.6V} \\ \mbox{(unless otherwise stated)}^{(1)} \\ \mbox{Operating temperature} & -40^{\circ}C \leq TA \leq +85^{\circ}C \mbox{ for Industrial} \\ & -40^{\circ}C \leq TA \leq +125^{\circ}C \mbox{ for Extended} \end{array}$								
Param No.	Symbol	Characteristic	Min.	Тур.	Max.	Units	Conditions					
Clock Parameters												
AD50	TAD	ADC Clock Period	76			ns						
AD51	tRC	ADC Internal RC Oscillator Period ⁽²⁾	—	250	_	ns						
Conversion Rate												
AD55	tCONV	Conversion Time	—	12 Tad	_	—						
AD56	FCNV	Throughput Rate	—	—	1.1	Msps	Using simultaneous sampling					
AD57a	TSAMP	Sample Time when Sampling any ANx Input	2 Tad	—	_	—						
AD57b	TSAMP	Sample Time when Sampling the Op Amp Outputs (Configuration A and Configuration B) ^(4,5)	4 Tad	_	_	—						
Timing Parameters												
AD60	tPCS	Conversion Start from Sample Trigger ^(2,3)	2 Tad	—	3 Tad	_	Auto-convert trigger is not selected					
AD61	tpss	Sample Start from Setting Sample (SAMP) bit ^(2,3))	2 Tad	—	3 Tad	—						
AD62	tcss	Conversion Completion to Sample Start (ASAM = 1) ^(2,3)	—	0.5 TAD	_	—						
AD63	tdpu	Time to Stabilize Analog Stage from ADC Off to ADC On ^(2,3)		_	20	μS	(Note 6)					

TABLE 30-61: ADC CONVERSION (10-BIT MODE) TIMING REQUIREMENTS

Note 1: Device is functional at VBORMIN < VDD < VDDMIN, but will have degraded performance. Device functionality is tested, but not characterized. Analog modules (ADC, op amp/comparator and comparator voltage reference) may have degraded performance. Refer to Parameter BO10 in Table 30-13 for the minimum and maximum BOR values.

- 2: Parameters are characterized but not tested in manufacturing.
- **3:** Because the sample caps will eventually lose charge, clock rates below 10 kHz may affect linearity performance, especially at elevated temperatures.
- 4: See Figure 25-6 for configuration information.
- 5: See Figure 25-7 for configuration information.
- 6: The parameter, tDPU, is the time required for the ADC module to stabilize at the appropriate level when the module is turned on (ADON (AD1CON1<15>) = 1). During this time, the ADC result is indeterminate.

TABLE 30-62: DMA MODULE TIMING REQUIREMENTS

АС СН/	ARACTERISTICS	$\begin{array}{l} \mbox{Standard Operating Conditions: 3.0V to 3.6V} \\ \mbox{(unless otherwise stated)} \\ \mbox{Operating temperature} & -40^\circ C \leq TA \leq +85^\circ C \mbox{ for Industrial} \\ & -40^\circ C \leq TA \leq +125^\circ C \mbox{ for Extended} \end{array}$						
Param No.	Characteristic	Min.	Тур. ⁽¹⁾	Max.	Units	Conditions		
DM1	DMA Byte/Word Transfer Latency	1 Tcy (2)	—	_	ns			

Note 1: These parameters are characterized, but not tested in manufacturing.

2: Because DMA transfers use the CPU data bus, this time is dependent on other functions on the bus.

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