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### What is "[Embedded - Microcontrollers](#)"?

"[Embedded - Microcontrollers](#)" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

### Applications of "[Embedded - Microcontrollers](#)"

#### Details

Product Status	Active
Core Processor	PIC
Core Size	16-Bit
Speed	60 MIPS
Connectivity	I <sup>2</sup> C, IrDA, LINbus, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, DMA, POR, PWM, WDT
Number of I/O	35
Program Memory Size	128KB (43K x 24)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	8K x 16
Voltage - Supply (Vcc/Vdd)	3V ~ 3.6V
Data Converters	A/D 9x10b/12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 125°C (TA)
Mounting Type	Surface Mount
Package / Case	48-UFQFN Exposed Pad
Supplier Device Package	48-UQFN (6x6)
Purchase URL	<a href="https://www.e-xfl.com/product-detail/microchip-technology/pic24ep128gp204-e-mv">https://www.e-xfl.com/product-detail/microchip-technology/pic24ep128gp204-e-mv</a>

FIGURE 2-7: INTERLEAVED PFC

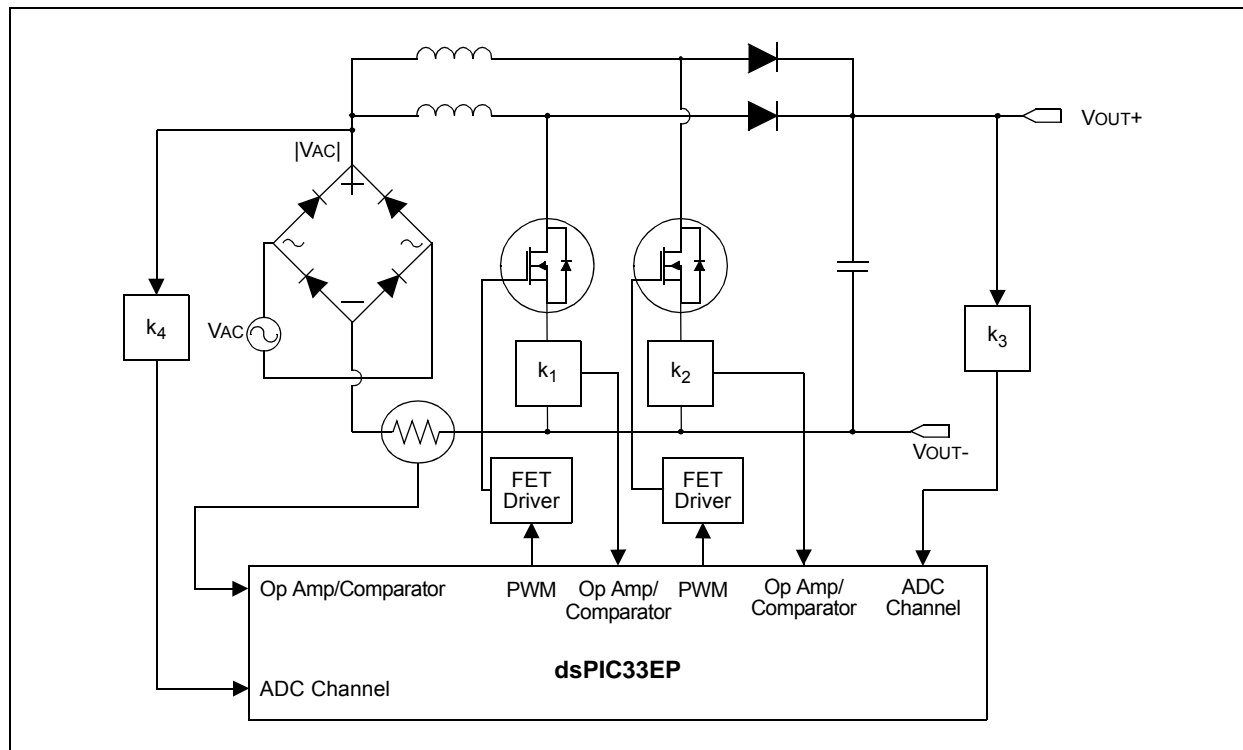
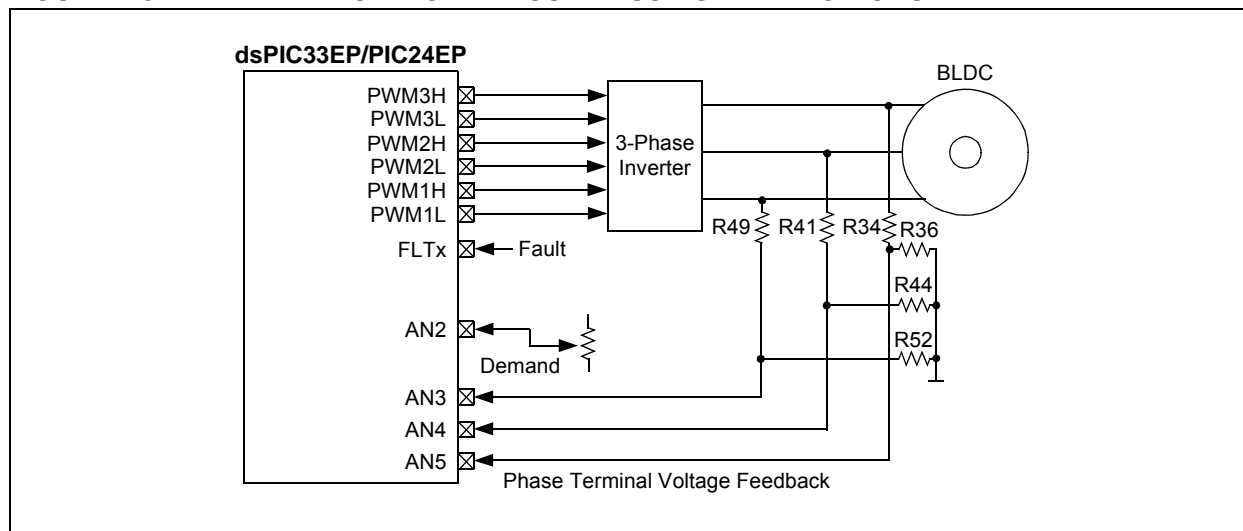


FIGURE 2-8: BEMF VOLTAGE MEASURED USING THE ADC MODULE



**TABLE 4-5: INTERRUPT CONTROLLER REGISTER MAP FOR dsPIC33EPXXXGP50X DEVICES ONLY (CONTINUED)**

File Name	Addr.	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	All Resets
INTCON1	08C0	NSTDIS	OVAERR	OVBERR	COVAERR	COVBERR	OVATE	OVBT	COVTE	SFTACERR	DIV0ERR	DMACERR	MATHERR	ADDRERR	STKERR	OSCFAIL	—	0000
INTCON2	08C2	GIE	DISI	SWTRAP	—	—	—	—	—	—	—	—	—	—	INT2EP	INT1EP	INT0EP	8000
INTCON3	08C4	—	—	—	—	—	—	—	—	—	—	DAE	DOOVR	—	—	—	—	0000
INTCON4	08C6	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	SGHT	0000
INTTREG	08C8	—	—	—	—	ILR<3:0>				VECNUM<7:0>								0000

**Legend:** — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

#### 4.8.1 DATA ACCESS FROM PROGRAM MEMORY USING TABLE INSTRUCTIONS

The TBLRDH and TBLWTL instructions offer a direct method of reading or writing the lower word of any address within the Program Space without going through Data Space. The TBLRDH and TBLWTL instructions are the only method to read or write the upper 8 bits of a Program Space word as data.

The PC is incremented by two for each successive 24-bit program word. This allows program memory addresses to directly map to Data Space addresses. Program memory can thus be regarded as two 16-bit-wide word address spaces, residing side by side, each with the same address range. TBLRDH and TBLWTL access the space that contains the least significant data word. TBLRDH and TBLWTL access the space that contains the upper data byte.

Two table instructions are provided to move byte or word-sized (16-bit) data to and from Program Space. Both function as either byte or word operations.

- TBLRDH (Table Read High):
  - In Word mode, this instruction maps the lower word of the Program Space location ( $P<15:0>$ ) to a data address ( $D<15:0>$ )

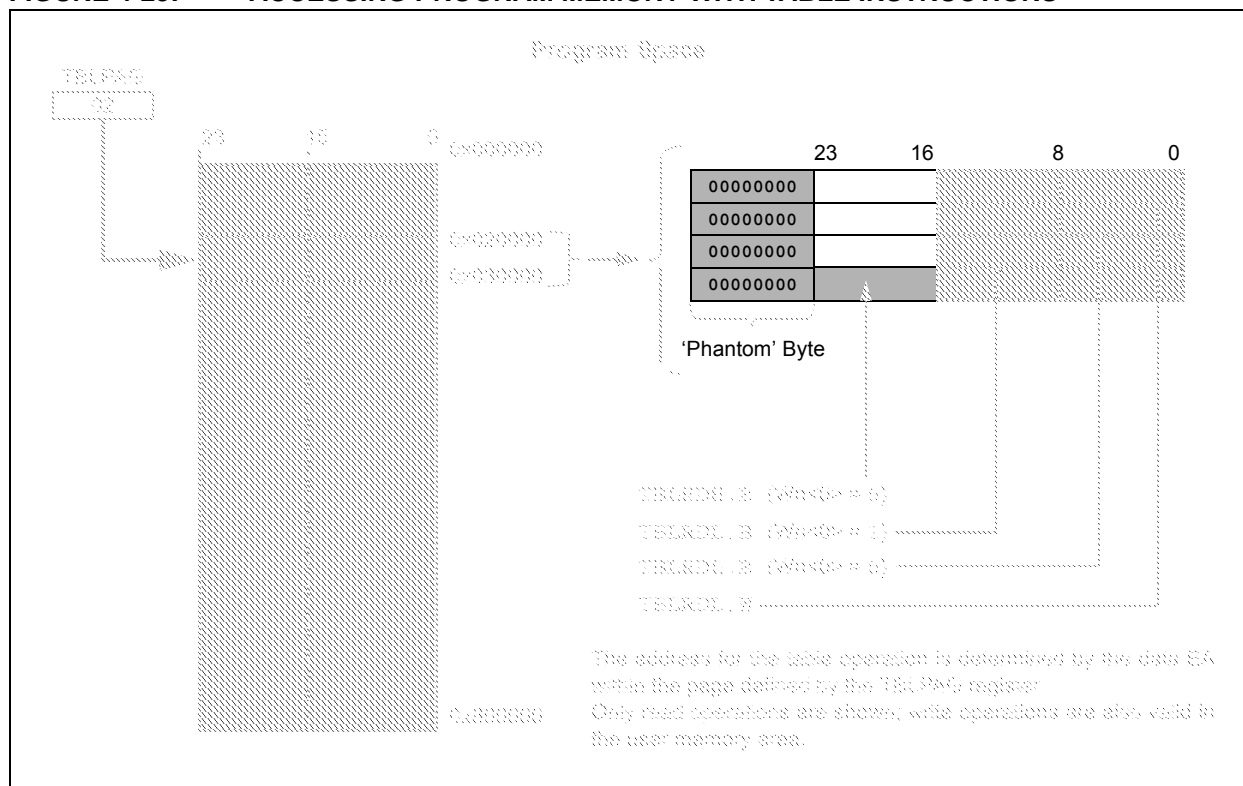
- In Byte mode, either the upper or lower byte of the lower program word is mapped to the lower byte of a data address. The upper byte is selected when Byte Select is '1'; the lower byte is selected when it is '0'.

- TBLRDH (Table Read High):
  - In Word mode, this instruction maps the entire upper word of a program address ( $P<23:16>$ ) to a data address. The 'phantom' byte ( $D<15:8>$ ) is always '0'.
  - In Byte mode, this instruction maps the upper or lower byte of the program word to  $D<7:0>$  of the data address in the TBLRDH instruction. The data is always '0' when the upper 'phantom' byte is selected (Byte Select = 1).

In a similar fashion, two table instructions, TBLWTH and TBLWTL, are used to write individual bytes or words to a Program Space address. The details of their operation are explained in **Section 5.0 "Flash Program Memory"**.

For all table operations, the area of program memory space to be accessed is determined by the Table Page register (TBLPAG). TBLPAG covers the entire program memory space of the device, including user application and configuration spaces. When  $TBLPAG<7> = 0$ , the table page is located in the user memory space. When  $TBLPAG<7> = 1$ , the page is located in configuration space.

**FIGURE 4-23: ACCESSING PROGRAM MEMORY WITH TABLE INSTRUCTIONS**



**REGISTER 7-5: INTCON3: INTERRUPT CONTROL REGISTER 3**

U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
—	—	—	—	—	—	—	—
bit 15							bit 8

U-0	U-0	R/W-0	R/W-0	U-0	U-0	U-0	U-0
—	—	DAE	DOOVR	—	—	—	—
bit 7							bit 0

**Legend:**

R = Readable bit                      W = Writable bit                      U = Unimplemented bit, read as '0'  
-n = Value at POR                      '1' = Bit is set                      '0' = Bit is cleared                      x = Bit is unknown

bit 15-6                      **Unimplemented:** Read as '0'  
bit 5                      **DAE:** DMA Address Error Soft Trap Status bit  
                                 1 = DMA address error soft trap has occurred  
                                 0 = DMA address error soft trap has not occurred  
bit 4                      **DOOVR:** DO Stack Overflow Soft Trap Status bit  
                                 1 = DO stack overflow soft trap has occurred  
                                 0 = DO stack overflow soft trap has not occurred  
bit 3-0                      **Unimplemented:** Read as '0'

**REGISTER 7-6: INTCON4: INTERRUPT CONTROL REGISTER 4**

U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
—	—	—	—	—	—	—	—
bit 15							bit 8

U-0	U-0	U-0	U-0	U-0	U-0	U-0	R/W-0
—	—	—	—	—	—	—	SGHT
bit 7							bit 0

**Legend:**

R = Readable bit                      W = Writable bit                      U = Unimplemented bit, read as '0'  
-n = Value at POR                      '1' = Bit is set                      '0' = Bit is cleared                      x = Bit is unknown

bit 15-1                      **Unimplemented:** Read as '0'  
bit 0                      **SGHT:** Software Generated Hard Trap Status bit  
                                 1 = Software generated hard trap has occurred  
                                 0 = Software generated hard trap has not occurred

**REGISTER 8-1: DMAxCON: DMA CHANNEL x CONTROL REGISTER**

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	U-0	U-0	U-0
CHEN	SIZE	DIR	HALF	NULLW	—	—	—
bit 15							bit 8

U-0	U-0	R/W-0	R/W-0	U-0	U-0	R/W-0	R/W-0
—	—	AMODE1	AMODE0	—	—	MODE1	MODE0
bit 7				bit 0			

**Legend:**

R = Readable bit

W = Writable bit

U = Unimplemented bit, read as '0'

-n = Value at POR

'1' = Bit is set

'0' = Bit is cleared

x = Bit is unknown

- bit 15      **CHEN:** DMA Channel Enable bit  
             1 = Channel is enabled  
             0 = Channel is disabled
- bit 14      **SIZE:** DMA Data Transfer Size bit  
             1 = Byte  
             0 = Word
- bit 13      **DIR:** DMA Transfer Direction bit (source/destination bus select)  
             1 = Reads from RAM address, writes to peripheral address  
             0 = Reads from peripheral address, writes to RAM address
- bit 12      **HALF:** DMA Block Transfer Interrupt Select bit  
             1 = Initiates interrupt when half of the data has been moved  
             0 = Initiates interrupt when all of the data has been moved
- bit 11      **NULLW:** Null Data Peripheral Write Mode Select bit  
             1 = Null data write to peripheral in addition to RAM write (DIR bit must also be clear)  
             0 = Normal operation
- bit 10-6    **Unimplemented:** Read as '0'
- bit 5-4      **AMODE<1:0>:** DMA Channel Addressing Mode Select bits  
             11 = Reserved  
             10 = Peripheral Indirect Addressing mode  
             01 = Register Indirect without Post-Increment mode  
             00 = Register Indirect with Post-Increment mode
- bit 3-2      **Unimplemented:** Read as '0'
- bit 1-0      **MODE<1:0>:** DMA Channel Operating Mode Select bits  
             11 = One-Shot, Ping-Pong modes are enabled (one block transfer from/to each DMA buffer)  
             10 = Continuous, Ping-Pong modes are enabled  
             01 = One-Shot, Ping-Pong modes are disabled  
             00 = Continuous, Ping-Pong modes are disabled

TABLE 9-1: CONFIGURATION BIT VALUES FOR CLOCK SELECTION

Oscillator Mode	Oscillator Source	POSCMD<1:0>	FNOSC<2:0>	See Notes
Fast RC Oscillator with Divide-by-N (FRCDIVN)	Internal	xx	111	1, 2
Fast RC Oscillator with Divide-by-16 (FRCDIV16)	Internal	xx	110	1
Low-Power RC Oscillator (LPRC)	Internal	xx	101	1
Primary Oscillator (HS) with PLL (HSPLL)	Primary	10	011	
Primary Oscillator (XT) with PLL (XTPLL)	Primary	01	011	
Primary Oscillator (EC) with PLL (ECPLL)	Primary	00	011	1
Primary Oscillator (HS)	Primary	10	010	
Primary Oscillator (XT)	Primary	01	010	
Primary Oscillator (EC)	Primary	00	010	1
Fast RC Oscillator (FRC) with Divide-by-N and PLL (FRCPLL)	Internal	xx	001	1
Fast RC Oscillator (FRC)	Internal	xx	000	1

**Note 1:** OSC2 pin function is determined by the OSCIOFNC Configuration bit.

**2:** This is the default oscillator mode for an unprogrammed (erased) device.

## 9.2 Oscillator Resources

Many useful resources are provided on the main product page of the Microchip web site for the devices listed in this data sheet. This product page, which can be accessed using this link, contains the latest updates and additional information.

**Note:** In the event you are not able to access the product page using the link above, enter this URL in your browser:  
<http://www.microchip.com/wwwproducts/Devices.aspx?dDocName=en555464>

### 9.2.1 KEY RESOURCES

- “**Oscillator**” (DS70580) in the “*dsPIC33/PIC24 Family Reference Manual*”
- Code Samples
- Application Notes
- Software Libraries
- Webinars
- All Related “*dsPIC33/PIC24 Family Reference Manual*” Sections
- Development Tools

**REGISTER 9-5: REFOCON: REFERENCE OSCILLATOR CONTROL REGISTER**

R/W-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
ROON	—	ROSSLP	ROSEL	RODIV3 <sup>(1)</sup>	RODIV2 <sup>(1)</sup>	RODIV1 <sup>(1)</sup>	RODIV0 <sup>(1)</sup>
bit 15							bit 8

U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
—	—	—	—	—	—	—	—
bit 7							bit 0

**Legend:**

R = Readable bit                      W = Writable bit                      U = Unimplemented bit, read as '0'  
 -n = Value at POR                      '1' = Bit is set                      '0' = Bit is cleared                      x = Bit is unknown

- bit 15            **ROON:** Reference Oscillator Output Enable bit  
                   1 = Reference oscillator output is enabled on the REFCLK pin<sup>(2)</sup>  
                   0 = Reference oscillator output is disabled
- bit 14            **Unimplemented:** Read as '0'
- bit 13            **ROSSLP:** Reference Oscillator Run in Sleep bit  
                   1 = Reference oscillator output continues to run in Sleep  
                   0 = Reference oscillator output is disabled in Sleep
- bit 12            **ROSEL:** Reference Oscillator Source Select bit  
                   1 = Oscillator crystal is used as the reference clock  
                   0 = System clock is used as the reference clock
- bit 11-8        **RODIV<3:0>:** Reference Oscillator Divider bits<sup>(1)</sup>  
                   1111 = Reference clock divided by 32,768  
                   1110 = Reference clock divided by 16,384  
                   1101 = Reference clock divided by 8,192  
                   1100 = Reference clock divided by 4,096  
                   1011 = Reference clock divided by 2,048  
                   1010 = Reference clock divided by 1,024  
                   1001 = Reference clock divided by 512  
                   1000 = Reference clock divided by 256  
                   0111 = Reference clock divided by 128  
                   0110 = Reference clock divided by 64  
                   0101 = Reference clock divided by 32  
                   0100 = Reference clock divided by 16  
                   0011 = Reference clock divided by 8  
                   0010 = Reference clock divided by 4  
                   0001 = Reference clock divided by 2  
                   0000 = Reference clock
- bit 7-0        **Unimplemented:** Read as '0'

- Note 1:** The reference oscillator output must be disabled (ROON = 0) before writing to these bits.  
**Note 2:** This pin is remappable. See **Section 11.4 “Peripheral Pin Select (PPS)”** for more information.



**NOTES:**

### 11.1.1 OPEN-DRAIN CONFIGURATION

In addition to the PORTx, LATx and TRISx registers for data control, port pins can also be individually configured for either digital or open-drain output. This is controlled by the Open-Drain Control register, ODCx, associated with each port. Setting any of the bits configures the corresponding pin to act as an open-drain output.

The open-drain feature allows the generation of outputs other than VDD by using external pull-up resistors. The maximum open-drain voltage allowed on any pin is the same as the maximum VIH specification for that particular pin.

See the “Pin Diagrams” section for the available 5V tolerant pins and Table 30-11 for the maximum VIH specification for each pin.

## 11.2 Configuring Analog and Digital Port Pins

The ANSELx register controls the operation of the analog port pins. The port pins that are to function as analog inputs or outputs must have their corresponding ANSELx and TRISx bits set. In order to use port pins for I/O functionality with digital modules, such as Timers, UARTs, etc., the corresponding ANSELx bit must be cleared.

The ANSELx register has a default value of 0xFFFF; therefore, all pins that share analog functions are analog (not digital) by default.

Pins with analog functions affected by the ANSELx registers are listed with a buffer type of analog in the Pinout I/O Descriptions (see Table 1-1).

If the TRISx bit is cleared (output) while the ANSELx bit is set, the digital output level (VOH or VOL) is converted by an analog peripheral, such as the ADC module or comparator module.

When the PORTx register is read, all pins configured as analog input channels are read as cleared (a low level).

Pins configured as digital inputs do not convert an analog input. Analog levels on any pin defined as a digital input (including the ANx pins) can cause the input buffer to consume current that exceeds the device specifications.

### 11.2.1 I/O PORT WRITE/READ TIMING

One instruction cycle is required between a port direction change or port write operation and a read operation of the same port. Typically this instruction would be a NOP, as shown in Example 11-1.

## 11.3 Input Change Notification (ICN)

The Input Change Notification function of the I/O ports allows devices to generate interrupt requests to the processor in response to a Change-of-State (COS) on selected input pins. This feature can detect input Change-of-States even in Sleep mode, when the clocks are disabled. Every I/O port pin can be selected (enabled) for generating an interrupt request on a Change-of-State.

Three control registers are associated with the Change Notification (CN) functionality of each I/O port. The CNENx registers contain the CN interrupt enable control bits for each of the input pins. Setting any of these bits enables a CN interrupt for the corresponding pins.

Each I/O pin also has a weak pull-up and a weak pull-down connected to it. The pull-ups and pull-downs act as a current source or sink source connected to the pin and eliminate the need for external resistors when push button, or keypad devices are connected. The pull-ups and pull-downs are enabled separately, using the CNPUPx and the CNPDPx registers, which contain the control bits for each of the pins. Setting any of the control bits enables the weak pull-ups and/or pull-downs for the corresponding pins.

**Note:** Pull-ups and pull-downs on Change Notification pins should always be disabled when the port pin is configured as a digital output.

### EXAMPLE 11-1: PORT WRITE/READ EXAMPLE

```
MOV    0xFF00, W0    ; Configure PORTB<15:8>
                        ; as inputs
MOV    W0, TRISB      ; and PORTB<7:0>
                        ; as outputs
NOP                                ; Delay 1 cycle
BTSS   PORTB, #13     ; Next Instruction
```

## 14.0 INPUT CAPTURE

**Note 1:** This data sheet summarizes the features of the dsPIC33EPXXXGP50X, dsPIC33EPXXXMC20X/50X and PIC24EPXXXGP/MC20X families of devices. It is not intended to be a comprehensive reference source. To complement the information in this data sheet, refer to “**Input Capture**” (DS70352) in the “*dsPIC33/dsPIC24 Family Reference Manual*”, which is available from the Microchip web site ([www.microchip.com](http://www.microchip.com)).

**2:** Some registers and associated bits described in this section may not be available on all devices. Refer to **Section 4.0 “Memory Organization”** in this data sheet for device-specific register and bit information.

The input capture module is useful in applications requiring frequency (period) and pulse measurement. The dsPIC33EPXXXGP50X, dsPIC33EPXXXMC20X/50X and PIC24EPXXXGP/MC20X devices support four input capture channels.

Key features of the input capture module include:

- Hardware-configurable for 32-bit operation in all modes by cascading two adjacent modules
- Synchronous and Trigger modes of output compare operation, with up to 19 user-selectable Trigger/Sync sources available
- A 4-level FIFO buffer for capturing and holding timer values for several events
- Configurable interrupt generation
- Up to six clock sources available for each module, driving a separate internal 16-bit counter

**FIGURE 14-1: INPUT CAPTURE x MODULE BLOCK DIAGRAM**

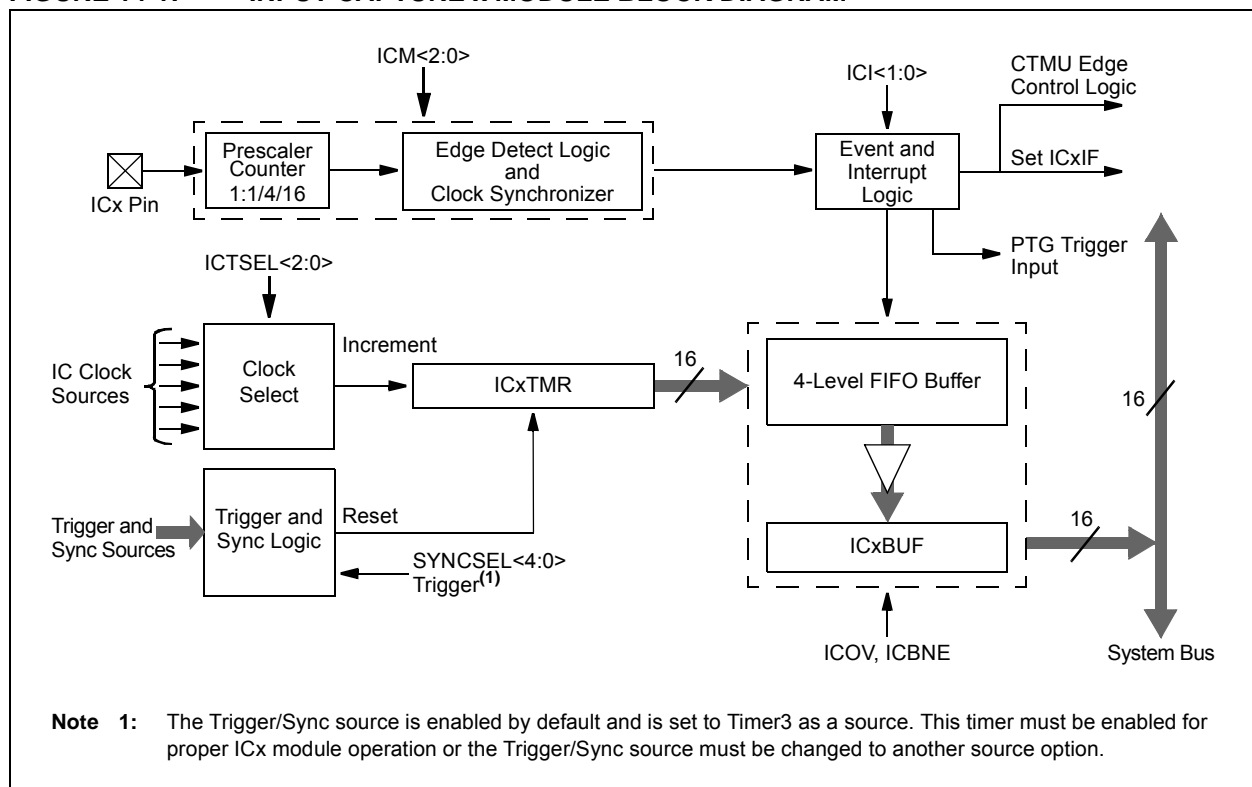
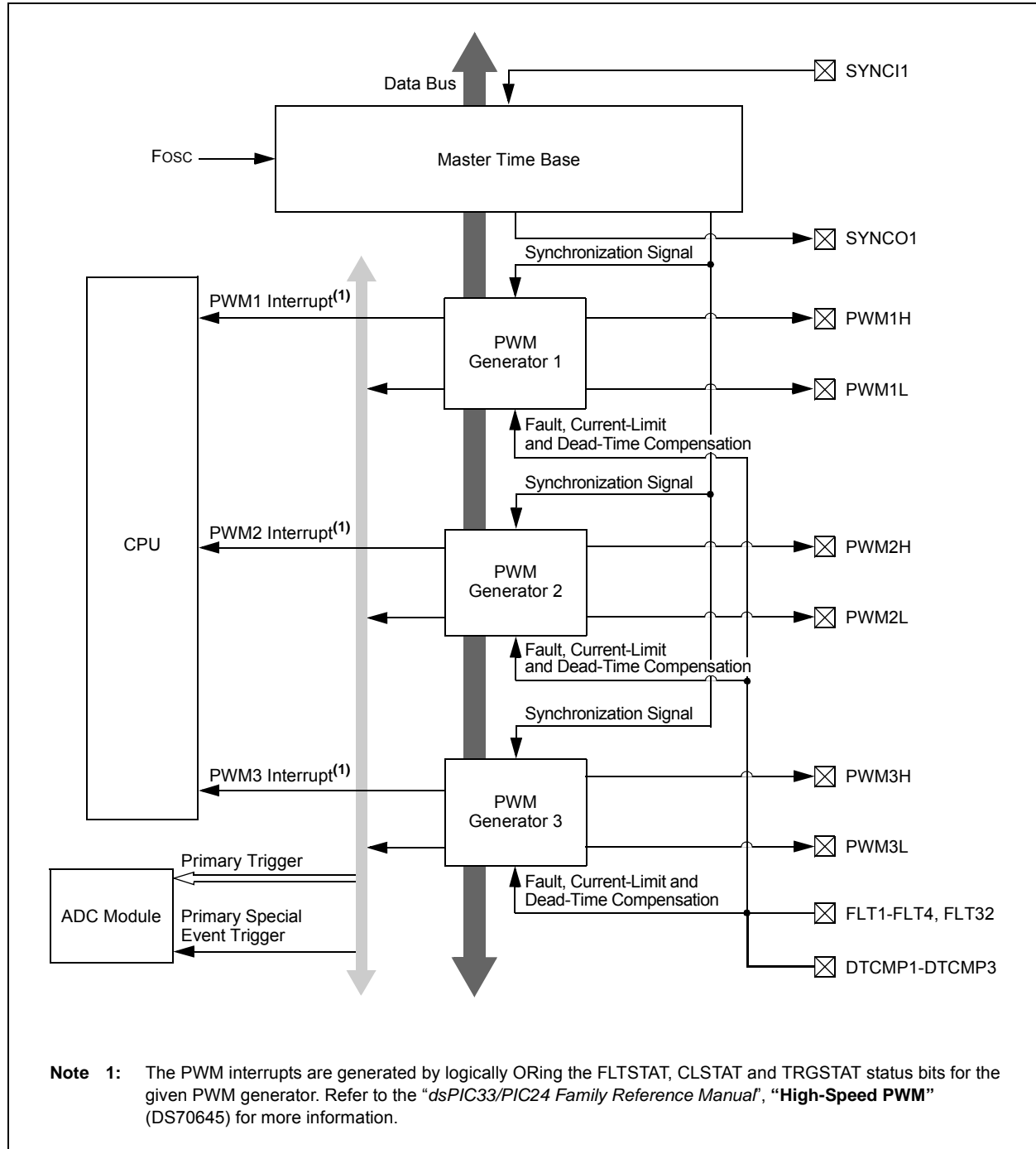


FIGURE 16-1: HIGH-SPEED PWMx MODULE ARCHITECTURAL OVERVIEW



## 17.0 QUADRATURE ENCODER INTERFACE (QEI) MODULE (dsPIC33EPXXXMC20X/50X and PIC24EPXXXMC20X DEVICES ONLY)

**Note 1:** This data sheet summarizes the features of the dsPIC33EPXXXGP50X, dsPIC33EPXXXMC20X/50X and PIC24EPXXXGP/MC20X families of devices. It is not intended to be a comprehensive reference source. To complement the information in this data sheet, refer to “**Quadrature Encoder Interface (QEI)**” (DS70601) in the “*dsPIC33/PIC24 Family Reference Manual*”, which is available from the Microchip web site ([www.microchip.com](http://www.microchip.com)).

**2:** Some registers and associated bits described in this section may not be available on all devices. Refer to **Section 4.0 “Memory Organization”** in this data sheet for device-specific register and bit information.

This chapter describes the Quadrature Encoder Interface (QEI) module and associated operational modes. The QEI module provides the interface to incremental encoders for obtaining mechanical position data.

The operational features of the QEI module include:

- 32-Bit Position Counter
- 32-Bit Index Pulse Counter
- 32-Bit Interval Timer
- 16-Bit Velocity Counter
- 32-Bit Position Initialization/Capture/Compare High register
- 32-Bit Position Compare Low register
- x4 Quadrature Count mode
- External Up/Down Count mode
- External Gated Count mode
- External Gated Timer mode
- Internal Timer mode

Figure 17-1 illustrates the QEI block diagram.

**REGISTER 18-2: SPIxCON1: SPIx CONTROL REGISTER 1**

U-0	U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
—	—	—	DISSCK	DISSDO	MODE16	SMP	CKE <sup>(1)</sup>
bit 15							bit 8

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
SSEN <sup>(2)</sup>	CKP	MSTEN	SPRE2 <sup>(3)</sup>	SPRE1 <sup>(3)</sup>	SPRE0 <sup>(3)</sup>	PPRE1 <sup>(3)</sup>	PPRE0 <sup>(3)</sup>
bit 7							bit 0

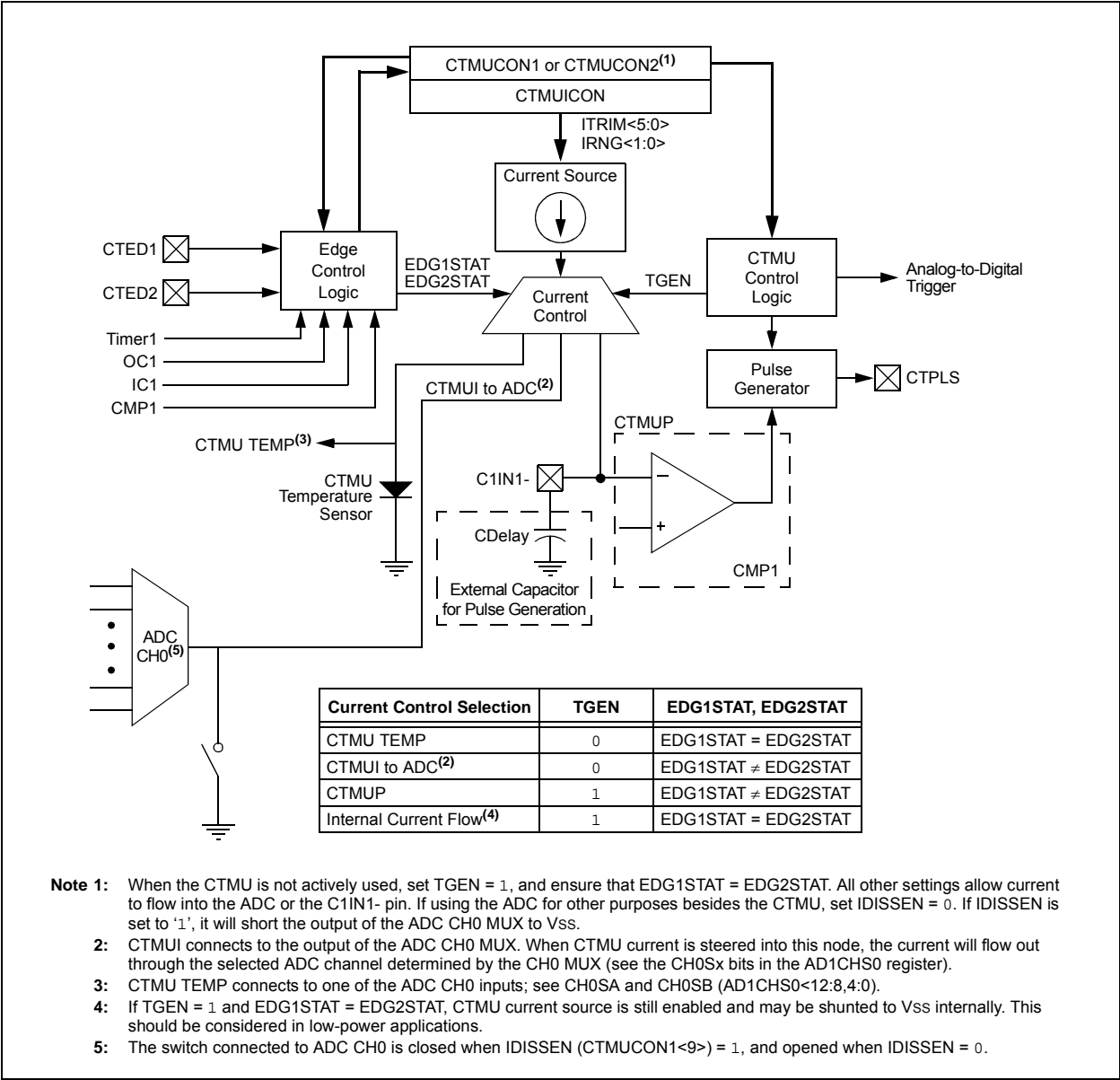
**Legend:**

R = Readable bit                      W = Writable bit                      U = Unimplemented bit, read as '0'  
 -n = Value at POR                      '1' = Bit is set                      '0' = Bit is cleared                      x = Bit is unknown

- bit 15-13      **Unimplemented:** Read as '0'
- bit 12      **DISSCK:** Disable SCKx Pin bit (SPIx Master modes only)  
 1 = Internal SPIx clock is disabled, pin functions as I/O  
 0 = Internal SPIx clock is enabled
- bit 11      **DISSDO:** Disable SDOx Pin bit  
 1 = SDOx pin is not used by the module; pin functions as I/O  
 0 = SDOx pin is controlled by the module
- bit 10      **MODE16:** Word/Byte Communication Select bit  
 1 = Communication is word-wide (16 bits)  
 0 = Communication is byte-wide (8 bits)
- bit 9      **SMP:** SPIx Data Input Sample Phase bit  
Master mode:  
 1 = Input data is sampled at end of data output time  
 0 = Input data is sampled at middle of data output time  
Slave mode:  
 SMP must be cleared when SPIx is used in Slave mode.
- bit 8      **CKE:** SPIx Clock Edge Select bit<sup>(1)</sup>  
 1 = Serial output data changes on transition from active clock state to Idle clock state (refer to bit 6)  
 0 = Serial output data changes on transition from Idle clock state to active clock state (refer to bit 6)
- bit 7      **SSEN:** Slave Select Enable bit (Slave mode)<sup>(2)</sup>  
 1 =  $\overline{SSx}$  pin is used for Slave mode  
 0 =  $\overline{SSx}$  pin is not used by the module; pin is controlled by port function
- bit 6      **CKP:** Clock Polarity Select bit  
 1 = Idle state for clock is a high level; active state is a low level  
 0 = Idle state for clock is a low level; active state is a high level
- bit 5      **MSTEN:** Master Mode Enable bit  
 1 = Master mode  
 0 = Slave mode

- Note 1:** The CKE bit is not used in Framed SPI modes. Program this bit to '0' for Framed SPI modes (FRMEN = 1).  
**Note 2:** This bit must be cleared when FRMEN = 1.  
**Note 3:** Do not set both primary and secondary prescalers to the value of 1:1.

FIGURE 22-1: CTMU BLOCK DIAGRAM



22.1 CTMU Resources

Many useful resources are provided on the main product page of the Microchip web site for the devices listed in this data sheet. This product page, which can be accessed using this link, contains the latest updates and additional information.

**Note:** In the event you are not able to access the product page using the link above, enter this URL in your browser:  
<http://www.microchip.com/wwwproducts/Devices.aspx?dDocName=en555464>

22.1.1 KEY RESOURCES

- “Charge Time Measurement Unit (CTMU)” (DS70661) in the “dsPIC33/PIC24 Family Reference Manual”
- Code Samples
- Application Notes
- Software Libraries
- Webinars
- All Related “dsPIC33/PIC24 Family Reference Manual” Sections
- Development Tools

## 23.2 ADC Helpful Tips

1. The SMP1x control bits in the AD1CON2 register:
  - a) Determine when the ADC interrupt flag is set and an interrupt is generated, if enabled.
  - b) When the CSCNA bit in the AD1CON2 registers is set to '1', this determines when the ADC analog scan channel list, defined in the AD1CSSL/AD1CSSH registers, starts over from the beginning.
  - c) When the DMA peripheral is not used (ADDMAEN = 0), this determines when the ADC Result Buffer Pointer to ADC1BUF0-ADC1BUFF gets reset back to the beginning at ADC1BUF0.
  - d) When the DMA peripheral is used (ADDMAEN = 1), this determines when the DMA Address Pointer is incremented after a sample/conversion operation. ADC1BUF0 is the only ADC buffer used in this mode. The ADC Result Buffer Pointer to ADC1BUF0-ADC1BUFF gets reset back to the beginning at ADC1BUF0. The DMA address is incremented after completion of every 32nd sample/conversion operation. Conversion results are stored in the ADC1BUF0 register for transfer to RAM using DMA.
2. When the DMA module is disabled (ADDMAEN = 0), the ADC has 16 result buffers. ADC conversion results are stored sequentially in ADC1BUF0-ADC1BUFF, regardless of which analog inputs are being used subject to the SMP1x bits and the condition described in 1c) above. There is no relationship between the ANx input being measured and which ADC buffer (ADC1BUF0-ADC1BUFF) that the conversion results will be placed in.
3. When the DMA module is enabled (ADDMAEN = 1), the ADC module has only 1 ADC result buffer (i.e., ADC1BUF0) per ADC peripheral and the ADC conversion result must be read, either by the CPU or DMA Controller, before the next ADC conversion is complete to avoid overwriting the previous value.
4. The DONE bit (AD1CON1<0>) is only cleared at the start of each conversion and is set at the completion of the conversion, but remains set indefinitely, even through the next sample phase until the next conversion begins. If application code is monitoring the DONE bit in any kind of software loop, the user must consider this behavior because the CPU code execution is faster than the ADC. As a result, in Manual Sample mode, particularly where the user's code is setting the SAMP bit (AD1CON1<1>), the DONE bit should also be cleared by the user application just before setting the SAMP bit.

5. Enabling op amps, comparator inputs and external voltage references can limit the availability of analog inputs (ANx pins). For example, when Op Amp 2 is enabled, the pins for AN0, AN1 and AN2 are used by the op amp's inputs and output. This negates the usefulness of Alternate Input mode since the MUXA selections use AN0-AN2. Carefully study the ADC block diagram to determine the configuration that will best suit your application. Configuration examples are available in the "**Analog-to-Digital Converter (ADC)**" (DS70621) section in the "*dsPIC33/PIC24 Family Reference Manual*".

## 23.3 ADC Resources

Many useful resources are provided on the main product page of the Microchip web site for the devices listed in this data sheet. This product page, which can be accessed using this link, contains the latest updates and additional information.

**Note:** In the event you are not able to access the product page using the link above, enter this URL in your browser:  
<http://www.microchip.com/wwwproducts/Devices.aspx?dDocName=en555464>

### 23.3.1 KEY RESOURCES

- "**Analog-to-Digital Converter (ADC)**" (DS70621) in the "*dsPIC33/PIC24 Family Reference Manual*"
- Code Samples
- Application Notes
- Software Libraries
- Webinars
- All Related "*dsPIC33/PIC24 Family Reference Manual*" Sections
- Development Tools



## 24.0 PERIPHERAL TRIGGER GENERATOR (PTG) MODULE

**Note 1:** This data sheet summarizes the features of the dsPIC33EPXXXGP50X, dsPIC33EPXXXMC20X/50X and PIC24EPXXXGP/MC20X families of devices. It is not intended to be a comprehensive reference source. To complement the information in this data sheet, refer to “**Peripheral Trigger Generator (PTG)**” (DS70669) in the “*dsPIC33/PIC24 Family Reference Manual*”, which is available from the Microchip web site ([www.microchip.com](http://www.microchip.com)).

**2:** Some registers and associated bits described in this section may not be available on all devices. Refer to **Section 4.0 “Memory Organization”** in this data sheet for device-specific register and bit information.

### 24.1 Module Introduction

The Peripheral Trigger Generator (PTG) provides a means to schedule complex high-speed peripheral operations that would be difficult to achieve using software. The PTG module uses 8-bit commands, called “Steps”, that the user writes to the PTG Queue registers (PTGQUE0-PTGQUE7), which perform operations, such as wait for input signal, generate output trigger and wait for timer.

The PTG module has the following major features:

- Multiple clock sources
- Two 16-bit general purpose timers
- Two 16-bit general limit counters
- Configurable for rising or falling edge triggering
- Generates processor interrupts to include:
  - Four configurable processor interrupts
  - Interrupt on a Step event in Single-Step mode
  - Interrupt on a PTG Watchdog Timer time-out
- Able to receive trigger signals from these peripherals:
  - ADC
  - PWM
  - Output Compare
  - Input Capture
  - Op Amp/Comparator
  - INT2
- Able to trigger or synchronize to these peripherals:
  - Watchdog Timer
  - Output Compare
  - Input Capture
  - ADC
  - PWM
  - Op Amp/Comparator

### 25.1.2 OP AMP CONFIGURATION B

Figure 25-7 shows a typical inverting amplifier circuit with the output of the op amp (OAxOUT) externally routed to a separate analog input pin (ANy) on the device. This op amp configuration is slightly different in terms of the op amp output and the ADC input connection, therefore, RINT1 is not included in the transfer function. However, this configuration requires the designer to externally route the op amp output (OAxOUT) to another analog input pin (ANy). See Table 30-53 in **Section 30.0 “Electrical Characteristics”** for the typical value of RINT1. Table 30-60 and Table 30-61 in **Section 30.0 “Electrical Characteristics”** describe the minimum sample time (TSAMP) requirements for the ADC module in this configuration.

Figure 25-7 also defines the equation to be used to calculate the expected voltage at point VOAxOUT. This is the typical inverting amplifier equation.

## 25.2 Op Amp/Comparator Resources

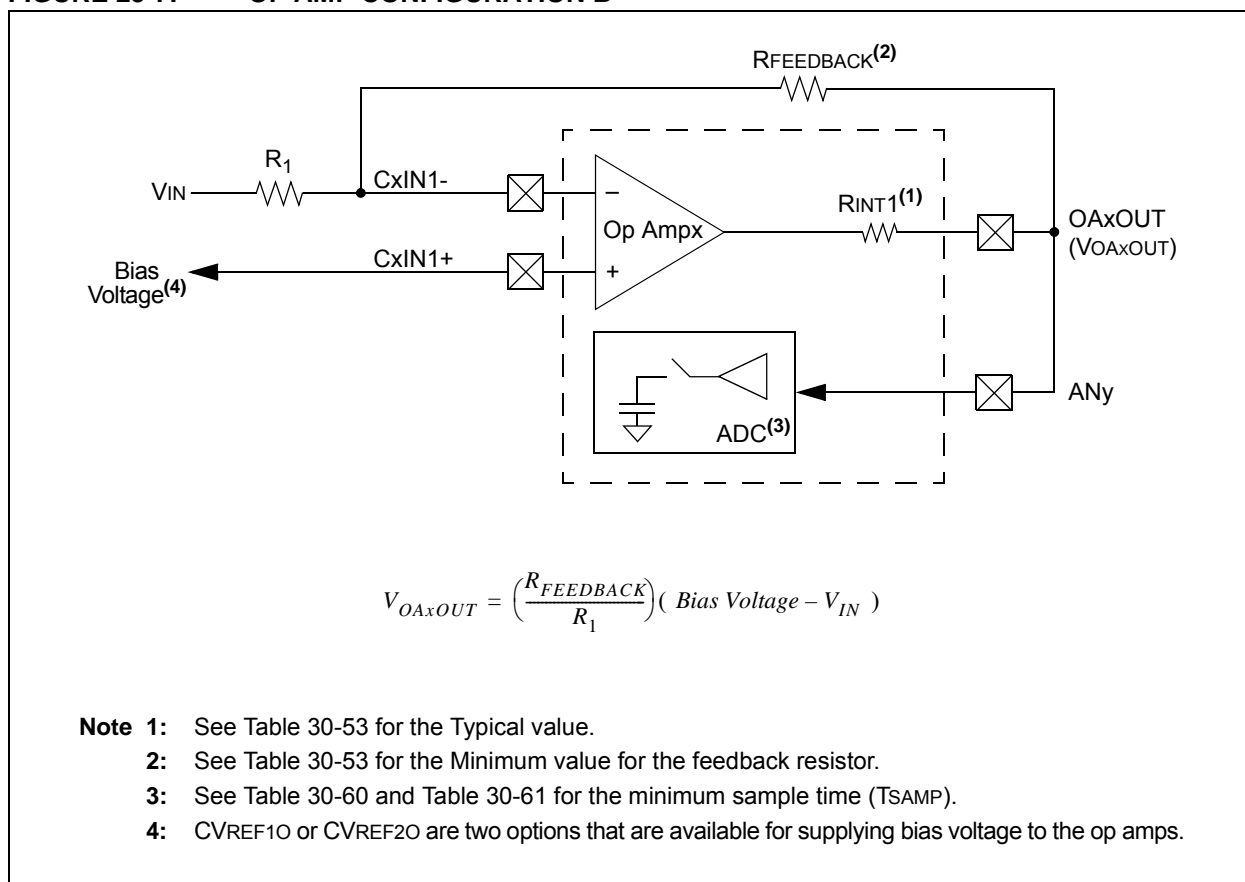
Many useful resources are provided on the main product page of the Microchip web site for the devices listed in this data sheet. This product page, which can be accessed using this link, contains the latest updates and additional information.

**Note:** In the event you are not able to access the product page using the link above, enter this URL in your browser:  
<http://www.microchip.com/wwwproducts/Devices.aspx?dDocName=en555464>

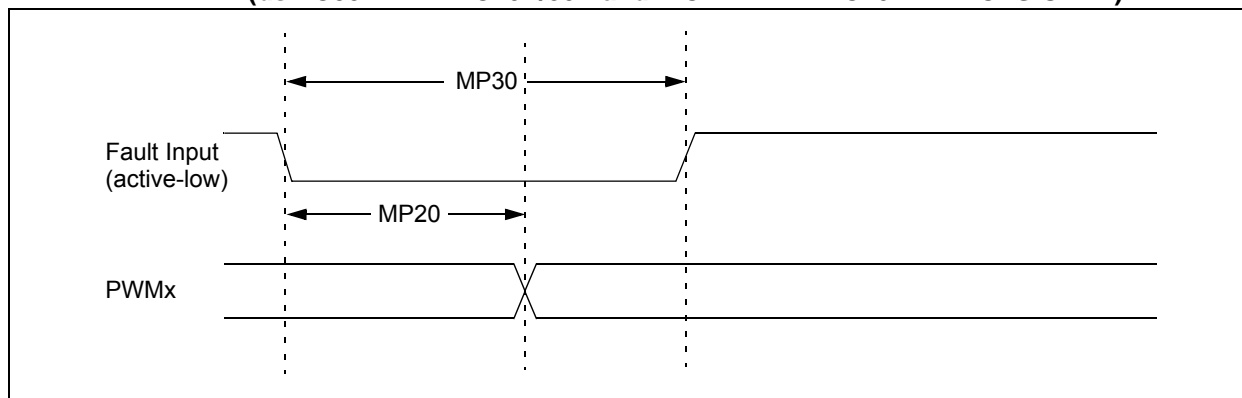
### 25.2.1 KEY RESOURCES

- “Op Amp/Comparator” (DS70357) in the “dsPIC33/PIC24 Family Reference Manual”
- Code Samples
- Application Notes
- Software Libraries
- Webinars
- All Related “dsPIC33/PIC24 Family Reference Manual” Sections
- Development Tools

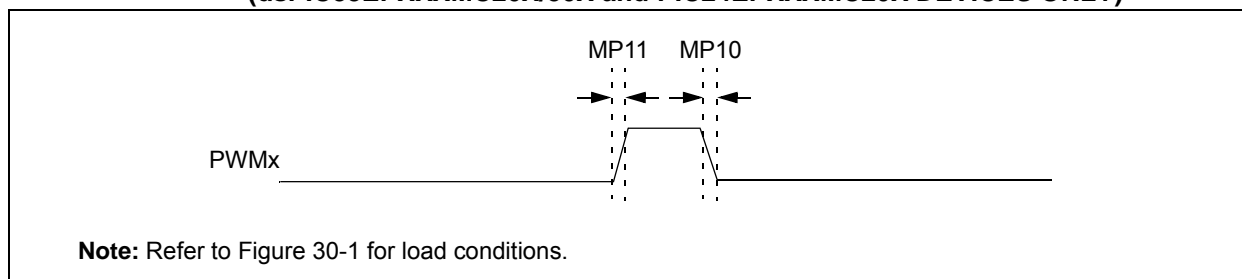
**FIGURE 25-7: OP AMP CONFIGURATION B**



**FIGURE 30-9: HIGH-SPEED PWMx MODULE FAULT TIMING CHARACTERISTICS**  
(dsPIC33EPXXXMC20X/50X and PIC24EPXXXMC20X DEVICES ONLY)



**FIGURE 30-10: HIGH-SPEED PWMx MODULE TIMING CHARACTERISTICS**  
(dsPIC33EPXXXMC20X/50X and PIC24EPXXXMC20X DEVICES ONLY)



**TABLE 30-29: HIGH-SPEED PWMx MODULE TIMING REQUIREMENTS**  
(dsPIC33EPXXXMC20X/50X and PIC24EPXXXMC20X DEVICES ONLY)

AC CHARACTERISTICS			Standard Operating Conditions: 3.0V to 3.6V (unless otherwise stated) Operating temperature $-40^{\circ}\text{C} \leq T_A \leq +85^{\circ}\text{C}$ for Industrial $-40^{\circ}\text{C} \leq T_A \leq +125^{\circ}\text{C}$ for Extended				
Param No.	Symbol	Characteristic <sup>(1)</sup>	Min.	Typ.	Max.	Units	Conditions
MP10	T <sub>FPWM</sub>	PWMx Output Fall Time	—	—	—	ns	See Parameter DO32
MP11	T <sub>RPWM</sub>	PWMx Output Rise Time	—	—	—	ns	See Parameter DO31
MP20	T <sub>FD</sub>	Fault Input ↓ to PWMx I/O Change	—	—	15	ns	
MP30	T <sub>FIH</sub>	Fault Input Pulse Width	15	—	—	ns	

**Note 1:** These parameters are characterized but not tested in manufacturing.

TABLE 31-12: ADC MODULE SPECIFICATIONS (12-BIT MODE)

AC CHARACTERISTICS			Standard Operating Conditions: 3.0V to 3.6V (unless otherwise stated) Operating temperature $-40^{\circ}\text{C} \leq T_A \leq +150^{\circ}\text{C}$				
Param No.	Symbol	Characteristic	Min	Typ	Max	Units	Conditions
ADC Accuracy (12-Bit Mode) <sup>(1)</sup>							
HAD20a	Nr	Resolution <sup>(3)</sup>	12 Data Bits			bits	
HAD21a	INL	Integral Nonlinearity	-5.5	—	5.5	LSb	V <sub>INL</sub> = AV <sub>SS</sub> = V <sub>REFL</sub> = 0V, AV <sub>DD</sub> = V <sub>REFH</sub> = 3.6V
HAD22a	DNL	Differential Nonlinearity	-1	—	1	LSb	V <sub>INL</sub> = AV <sub>SS</sub> = V <sub>REFL</sub> = 0V, AV <sub>DD</sub> = V <sub>REFH</sub> = 3.6V
HAD23a	GERR	Gain Error	-10	—	10	LSb	V <sub>INL</sub> = AV <sub>SS</sub> = V <sub>REFL</sub> = 0V, AV <sub>DD</sub> = V <sub>REFH</sub> = 3.6V
HAD24a	EOFF	Offset Error	-5	—	5	LSb	V <sub>INL</sub> = AV <sub>SS</sub> = V <sub>REFL</sub> = 0V, AV <sub>DD</sub> = V <sub>REFH</sub> = 3.6V
Dynamic Performance (12-Bit Mode) <sup>(2)</sup>							
HAD33a	FNYQ	Input Signal Bandwidth	—	—	200	kHz	

**Note 1:** These parameters are characterized, but are tested at 20 ksp/s only.

**2:** These parameters are characterized by similarity, but are not tested in manufacturing.

**3:** Injection currents  $> |0|$  can affect the ADC results by approximately 4-6 counts.

TABLE 31-13: ADC MODULE SPECIFICATIONS (10-BIT MODE)

AC CHARACTERISTICS			Standard Operating Conditions: 3.0V to 3.6V (unless otherwise stated) Operating temperature $-40^{\circ}\text{C} \leq T_A \leq +150^{\circ}\text{C}$				
Param No.	Symbol	Characteristic	Min	Typ	Max	Units	Conditions
ADC Accuracy (10-Bit Mode) <sup>(1)</sup>							
HAD20b	Nr	Resolution <sup>(3)</sup>	10 Data Bits			bits	
HAD21b	INL	Integral Nonlinearity	-1.5	—	1.5	LSb	V <sub>INL</sub> = AV <sub>SS</sub> = V <sub>REFL</sub> = 0V, AV <sub>DD</sub> = V <sub>REFH</sub> = 3.6V
HAD22b	DNL	Differential Nonlinearity	-0.25	—	0.25	LSb	V <sub>INL</sub> = AV <sub>SS</sub> = V <sub>REFL</sub> = 0V, AV <sub>DD</sub> = V <sub>REFH</sub> = 3.6V
HAD23b	GERR	Gain Error	-2.5	—	2.5	LSb	V <sub>INL</sub> = AV <sub>SS</sub> = V <sub>REFL</sub> = 0V, AV <sub>DD</sub> = V <sub>REFH</sub> = 3.6V
HAD24b	EOFF	Offset Error	-1.25	—	1.25	LSb	V <sub>INL</sub> = AV <sub>SS</sub> = V <sub>REFL</sub> = 0V, AV <sub>DD</sub> = V <sub>REFH</sub> = 3.6V
Dynamic Performance (10-Bit Mode) <sup>(2)</sup>							
HAD33b	FNYQ	Input Signal Bandwidth	—	—	400	kHz	

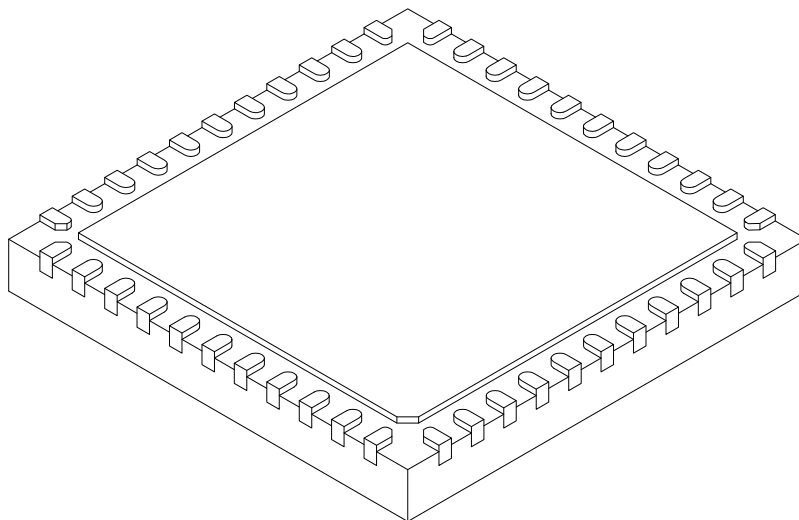
**Note 1:** These parameters are characterized, but are tested at 20 ksp/s only.

**2:** These parameters are characterized by similarity, but are not tested in manufacturing.

**3:** Injection currents  $> |0|$  can affect the ADC results by approximately 4-6 counts.

**44-Lead Plastic Quad Flat, No Lead Package (ML) - 8x8 mm Body [QFN]**

**Note:** For the most current package drawings, please see the Microchip Packaging Specification located at <http://www.microchip.com/packaging>



Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Number of Pins	N	44		
Pitch	e	0.65 BSC		
Overall Height	A	0.80	0.90	1.00
Standoff	A1	0.00	0.02	0.05
Terminal Thickness	A3	0.20 REF		
Overall Width	E	8.00 BSC		
Exposed Pad Width	E2	6.25	6.45	6.60
Overall Length	D	8.00 BSC		
Exposed Pad Length	D2	6.25	6.45	6.60
Terminal Width	b	0.20	0.30	0.35
Terminal Length	L	0.30	0.40	0.50
Terminal-to-Exposed-Pad	K	0.20	-	-

**Notes:**

- Pin 1 visual index feature may vary, but must be located within the hatched area.
- Package is saw singulated
- Dimensioning and tolerancing per ASME Y14.5M

BSC: Basic Dimension. Theoretically exact value shown without tolerances.

REF: Reference Dimension. usually without tolerance. for information purposes only.

Microchip Technology Drawing C04-103C Sheet 2 of 2