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Applications of "<u>Embedded -</u> <u>Microcontrollers</u>"

Details

Product Status	Obsolete
Core Processor	PIC
Core Size	16-Bit
Speed	60 MIPs
Connectivity	I ² C, IrDA, LINbus, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, DMA, POR, PWM, WDT
Number of I/O	35
Program Memory Size	128KB (43K x 24)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	8K x 16
Voltage - Supply (Vcc/Vdd)	3V ~ 3.6V
Data Converters	A/D 9x10b/12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 125°C (TA)
Mounting Type	Surface Mount
Package / Case	44-VFTLA Exposed Pad
Supplier Device Package	44-VTLA (6x6)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/pic24ep128gp204-e-tl

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3.5 **Programmer's Model**

The programmer's model for the dsPIC33EPXXXGP50X, dsPIC33EPXXXMC20X/50X and PIC24EPXXXGP/MC20X is shown in Figure 3-2. All registers in the programmer's model are memory mapped and can be manipulated directly by instructions. Table 3-1 lists a description of each register.

In addition to the registers contained in the programmer's model, the dsPIC33EPXXXGP50X, dsPIC33EPXXXMC20X/50X and PIC24EPXXXGP/

MC20X devices contain control registers for Modulo Addressing (dsPIC33EPXXXMC20X/50X and dsPIC33EPXXXGP50X devices only), Bit-Reversed Addressing (dsPIC33EPXXXMC20X/50X and dsPIC33EPXXXGP50X devices only) and interrupts. These registers are described in subsequent sections of this document.

All registers associated with the programmer's model are memory mapped, as shown in Table 4-1.

Register(s) Name	Description
W0 through W15	Working Register Array
ACCA, ACCB	40-Bit DSP Accumulators
PC	23-Bit Program Counter
SR	ALU and DSP Engine STATUS Register
SPLIM	Stack Pointer Limit Value Register
TBLPAG	Table Memory Page Address Register
DSRPAG	Extended Data Space (EDS) Read Page Register
DSWPAG	Extended Data Space (EDS) Write Page Register
RCOUNT	REPEAT Loop Count Register
DCOUNT ⁽¹⁾	DO Loop Count Register
DOSTARTH ^(1,2) , DOSTARTL ^(1,2)	DO Loop Start Address Register (High and Low)
DOENDH ⁽¹⁾ , DOENDL ⁽¹⁾	DO Loop End Address Register (High and Low)
CORCON	Contains DSP Engine, DO Loop Control and Trap Status bits

TABLE 3-1: PROGRAMMER'S MODEL REGISTER DESCRIPTIONS

Note 1: This register is available on dsPIC33EPXXXMC20X/50X and dsPIC33EPXXXGP50X devices only.

2: The DOSTARTH and DOSTARTL registers are read-only.

TABLE 4-37: PMD REGISTER MAP FOR PIC24EPXXXGP20X DEVICES ONLY

File Name	Addr.	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	All Resets
PMD1	0760	T5MD	T4MD	T3MD	T2MD	T1MD	-	-	-	I2C1MD	U2MD	U1MD	SPI2MD	SPI1MD	—	—	AD1MD	0000
PMD2	0762	_	_	—	_	IC4MD	IC3MD	IC2MD	IC1MD	_	_	_	-	OC4MD	OC3MD	OC2MD	OC1MD	0000
PMD3	0764	_	_	_	_	_	CMPMD	_	_	CRCMD	_	_	_	_	_	I2C2MD	_	0000
PMD4	0766	_	_	_	_	_	_	_	_	_	_	_	_	REFOMD	CTMUMD	_	_	0000
PMD6	076A	_	_	_	_	_	_	_	_	_	_	_	_	_	_	_	_	0000
													DMA0MD					
	0760												DMA1MD	DTCMD				0000
PMD7 076C -	_	_	_	_	_	_	_	_	_	_	_	DMA2MD	PIGMD	_	_	_	0000	
												DMA3MD						

Legend: — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

TABLE 4-38: PMD REGISTER MAP FOR PIC24EPXXXMC20X DEVICES ONLY

File Name	Addr.	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	All Resets
PMD1	0760	T5MD	T4MD	T3MD	T2MD	T1MD	QEI1MD	PWMMD	_	I2C1MD	U2MD	U1MD	SPI2MD	SPI1MD	_	_	AD1MD	0000
PMD2	0762	_	—	—	—	IC4MD	IC3MD	IC2MD	IC1MD	—	_	—		OC4MD	OC3MD	OC2MD	OC1MD	0000
PMD3	0764	_	_	_	_	_	CMPMD	_	_	CRCMD	_	_	_	_	_	I2C2MD	_	0000
PMD4	0766	_	_	_	_	_	_	_	_	_	_	_	_	REFOMD	CTMUMD	_	_	0000
PMD6	076A	_	_	_	_	_	PWM3MD	PWM2MD	PWM1MD	_	_	_	_	_	_	_	_	0000
													DMA0MD					
	0760												DMA1MD	DTCMD				0000
FIND	0700	_	_	_	_	_	_	_	_	_	_	_	DMA2MD	FIGND	_	_		0000
													DMA3MD					1

Legend: — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

TABLE 4-59: PORTA REGISTER MAP FOR PIC24EPXXXGP/MC202 AND dsPIC33EPXXXGP/MC202/502 DEVICES ONLY

File Name	Addr.	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	All Resets
TRISA	0E00		—	—				—			—		TRISA4	TRISA3	TRISA2	TRISA1	TRISA0	001F
PORTA	0E02		—	_		_		—			—		RA4	RA3	RA2	RA1	RA0	0000
LATA	0E04		—	—				—			—		LATA4	LATA3	LATA2	LA1TA1	LA0TA0	0000
ODCA	0E06		—	—				—			—		ODCA4	ODCA3	ODCA2	ODCA1	ODCA0	0000
CNENA	0E08		—	—				—			—		CNIEA4	CNIEA3	CNIEA2	CNIEA1	CNIEA0	0000
CNPUA	0E0A		—	—				—			—		CNPUA4	CNPUA3	CNPUA2	CNPUA1	CNPUA0	0000
CNPDA	0E0C		—	—				—			—		CNPDA4	CNPDA3	CNPDA2	CNPDA1	CNPDA0	0000
ANSELA	0E0E	-	—	—			-	—		_	_		ANSA4	_	—	ANSA1	ANSA0	0013

Legend: — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

TABLE 4-60: PORTB REGISTER MAP FOR PIC24EPXXXGP/MC202 AND dsPIC33EPXXXGP/MC202/502 DEVICES ONLY

File Name	Addr.	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	All Resets
TRISB	0E10	TRISB15	TRISB14	TRISB13	TRISB12	TRISB11	TRISB10	TRISB9	TRISB8	TRISB7	TRISB6	TRISB5	TRISB4	TRISB3	TRISB2	TRISB1	TRISB0	FFFF
PORTB	0E12	RB15	RB14	RB13	RB12	RB11	RB10	RB9	RB8	RB7	RB6	RB5	RB4	RB3	RB2	RB1	RB0	xxxx
LATB	0E14	LATB15	LATB14	LATB13	LATB12	LATB11	LATB10	LATB9	LATB8	LATB7	LATB6	LATB5	LATB4	LATB3	LATB2	LATB1	LATB0	xxxx
ODCB	0E16	ODCB15	ODCB14	ODCB13	ODCB12	ODCB11	ODCB10	ODCB9	ODCB8	ODCB7	ODCB6	ODCB5	ODCB4	ODCB3	ODCB2	ODCB1	ODCB0	0000
CNENB	0E18	CNIEB15	CNIEB14	CNIEB13	CNIEB12	CNIEB11	CNIEB10	CNIEB9	CNIEB8	CNIEB7	CNIEB6	CNIEB5	CNIEB4	CNIEB3	CNIEB2	CNIEB1	CNIEB0	0000
CNPUB	0E1A	CNPUB15	CNPUB14	CNPUB13	CNPUB12	CNPUB11	CNPUB10	CNPUB9	CNPUB8	CNPUB7	CNPUB6	CNPUB5	CNPUB4	CNPUB3	CNPUB2	CNPUB1	CNPUB0	0000
CNPDB	0E1C	CNPDB15	CNPDB14	CNPDB13	CNPDB12	CNPDB11	CNPDB10	CNPDB9	CNPDB8	CNPDB7	CNPDB6	CNPDB5	CNPDB4	CNPDB3	CNPDB2	CNPDB1	CNPDB0	0000
ANSELB	0E1E			_	-	—	—	—	ANSB8		_	—		ANSB3	ANSB2	ANSB1	ANSB0	010F

Legend: x = unknown value on Reset, — = unimplemented, read as '0'. Reset values are shown in hexadecimal.



EXAMPLE 4-3: PAGED DATA MEMORY SPACE

dsPIC33EPXXXGP50X, dsPIC33EPXXXMC20X/50X AND PIC24EPXXXGP/MC20X

REGISTER 17-7: VEL1CNT: VELOCITY COUNTER 1 REGISTER

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0					
			VELC	NT<15:8>								
bit 15							bit 8					
R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0					
			VELC	NT<7:0>								
bit 7							bit 0					
Legend:												
R = Readable b	= Readable bit W = Writable bit U = Unimplemented bit, read as '0'											
-n = Value at P	a = Value at POR (1' = Bit is set (0' = Bit is cleared x = Bit is unknown											

bit 15-0 VELCNT<15:0>: Velocity Counter bits

REGISTER 17-8: INDX1CNTH: INDEX COUNTER 1 HIGH WORD REGISTER

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
			INDXCN	T<31:24>			
bit 15							bit 8
R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
			INDXCN	T<23:16>			
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit	, read as '0'
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15-0 INDXCNT<31:16>: High Word Used to Form 32-Bit Index Counter Register (INDX1CNT) bits

REGISTER 17-9: INDX1CNTL: INDEX COUNTER 1 LOW WORD REGISTER

'1' = Bit is set

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
			INDXC	NT<15:8>			
bit 15							bit 8
R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
			INDXC	NT<7:0>			
bit 7							bit 0
Legend:							
R = Readable b	it	W = Writable bit	:	U = Unimpler	mented bit, read	l as '0'	

'0' = Bit is cleared

bit 15-0 INDXCNT<15:0>: Low Word Used to Form 32-Bit Index Counter Register (INDX1CNT) bits

-n = Value at POR

x = Bit is unknown

REGISTER 18-2: SPIXCON1: SPIX CONTROL REGISTER 1 (CONTINUED)

- SPRE<2:0>: Secondary Prescale bits (Master mode)⁽³⁾ bit 4-2 111 = Secondary prescale 1:1 110 = Secondary prescale 2:1 000 = Secondary prescale 8:1 bit 1-0 PPRE<1:0>: Primary Prescale bits (Master mode)⁽³⁾ 11 = Primary prescale 1:1
 - 10 = Primary prescale 4:1
 - 01 = Primary prescale 16:1
 - 00 = Primary prescale 64:1
- Note 1: The CKE bit is not used in Framed SPI modes. Program this bit to '0' for Framed SPI modes (FRMEN = 1).
 - 2: This bit must be cleared when FRMEN = 1.
 - 3: Do not set both primary and secondary prescalers to the value of 1:1.



FIGURE 19-1: I2Cx BLOCK DIAGRAM (X = 1 OR 2)

U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
_	_	_	_	_	_	_	_
bit 15							bit 8
R/W-0	R/W-0	R/W-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0
IVRIE	WAKIE	ERRIE	—	FIFOIE	RBOVIE	RBIE	TBIE
bit 7					·		bit 0
Legend:							
R = Readable	bit	W = Writable	bit	U = Unimpler	mented bit, read	as '0'	
-n = Value at F	POR	'1' = Bit is set		'0' = Bit is cle	ared	x = Bit is unkr	nown
bit 15-8	Unimplemen	ted: Read as ')'				
bit 7	IVRIE: Invalid	I Message Inter	rupt Enable b	bit			
	1 = Interrupt r	equest is enab	led				
		request is not e	nabled				
DIT 6	WAKIE: Bus	vvake-up Activi	ty interrupt Er	Table bit			
	$\perp = \text{Interrupt r}$ 0 = Interrupt r	request is enab	nabled				
bit 5	ERRIE: Frror	Interrupt Enab	le bit				
	1 = Interrupt r	request is enab	led				
	0 = Interrupt r	equest is not e	nabled				
bit 4	Unimplemen	ted: Read as ')'				
bit 3	FIFOIE: FIFO	Almost Full Int	errupt Enable	e bit			
	1 = Interrupt r	request is enab	led				
	0 = Interrupt r	request is not e	nabled				
bit 2	RBOVIE: RX	Buffer Overflov	v Interrupt En	able bit			
	1 = Interrupt r	request is enab	led nabled				
hit 1	BBIE: BX But	ffer Interrunt Fr	nable hit				
bit 1	1 = Interrupt r	request is enab	led				
	0 = Interrupt r	request is not e	nabled				
bit 0	TBIE: TX Buff	fer Interrupt En	able bit				
	1 = Interrupt r	request is enab	led				
	0 = Interrupt r	request is not e	nabled				

REGISTER 21-7: CXINTE: ECANX INTERRUPT ENABLE REGISTER

REGISTER 21-13: CxBUFPNT2: ECANx FILTER 4-7 BUFFER POINTER REGISTER 2

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	F7BP	<3:0>			F6BI	><3:0>	
bit 15							bit 8
R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	F5BP	<3:0>			F4BI	><3:0>	
bit 7							bit 0
Legend:							
R = Readable	bit	W = Writable	bit	U = Unimpleme	nted bit, rea	d as '0'	
-n = Value at I	POR	'1' = Bit is set		'0' = Bit is cleare	ed	x = Bit is unkr	nown
bit 15-12	F7BP<3:0>: 1111 = Filter	RX Buffer Masl	k for Filter 7 b	its ffer			

1110 = Filter hits received in RX Buffer 14
•
•
0001 = Filter hits received in RX Buffer 1 0000 = Filter hits received in RX Buffer 0
F6BP<3:0>: RX Buffer Mask for Filter 6 bits (same values as bits<15:12>)
F5BP<3:0>: RX Buffer Mask for Filter 5 bits (same values as bits<15:12>)
F4BP<3:0>: RX Buffer Mask for Filter 4 bits (same values as bits<15:12>)

REGISTER 21-14: CxBUFPNT3: ECANx FILTER 8-11 BUFFER POINTER REGISTER 3

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	F11BF	P<3:0>			F10B	P<3:0>	
bit 15							bit 8
R/W_0	R/M-0	R/M/-0	R/M-0	R/\\/_0	R/W/-0	R/M/-0	R/\/_0
10,00-0	F9BP	>	1000-0	10,00-0	F8B	P<3:0>	1477-0
bit 7							bit 0
Legend:							
R = Readable	e bit	W = Writable	bit	U = Unimpler	nented bit, rea	d as '0'	
-n = Value at	POR	'1' = Bit is set		'0' = Bit is cleared		x = Bit is unknown	
bit 15-12	F11BP<3:0> 1111 = Filter 1110 = Filter • • • 0001 = Filter 0000 = Filter	RX Buffer Mar hits received ir hits received ir hits received ir hits received ir	sk for Filter 1 n RX FIFO bu n RX Buffer 1 n RX Buffer 1 n RX Buffer 0	1 bits iffer 4			
bit 11-8 bit 7-4	F10BP<3:0> F9BP<3:0>:	RX Buffer Ma	sk for Filter 1 k for Filter 9 t	0 bits (same val bits (same value	lues as bits<15 s as bits<15:1	5:12>) 2>)	
bit 3-0	F8BP<3:0>:	RX Buffer Mas	k for Filter 8 k	oits (same value	s as bits<15:1	2>)	

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NOTES:

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
ADCTS	4 ADCTS3	ADCTS2	ADCTS1	IC4TSS	IC3TSS	IC2TSS	IC1TSS
bit 15							bit 8
						=	=
R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
00408	00308	OC2CS	OC1CS	OC41SS	OC31SS	OC21SS	OCTISS
DIT 7							Dit U
l egend:							
R = Reada	able bit	W = Writable	bit	U = Unimpler	mented bit. read	d as '0'	
-n = Value	at POR	'1' = Bit is set		'0' = Bit is cle	eared	x = Bit is unkr	nown
bit 15	ADCTS4: Sa	mple Trigger P	TGO15 for AE	DC bit			
	1 = Generate	s Trigger wher	the broadcas	t command is	executed		
	0 = Does not	generate Trigg	er when the b	roadcast comr	mand is execute	ed	
bit 14	ADCIS3: Sa	mple Trigger P	IGO14 for AL	DC bit	overuted		
	0 = Does not	generate Trigo	er when the b	roadcast com	mand is execute	ed	
bit 13	ADCTS2: Sa	mple Trigger P	TGO13 for AE	DC bit			
	1 = Generate	s Trigger wher	the broadcas	t command is	executed		
	0 = Does not	generate Trigg	er when the b	roadcast comr	mand is execute	ed	
bit 12	ADCIS1: Sa	mple Trigger P	IGO12 for AL	DC bit	overuted		
	0 = Does not	generate Trigo	er when the b	roadcast com	mand is execute	ed	
bit 11	IC4TSS: Trig	ger/Synchroniz	ation Source	for IC4 bit			
	1 = Generate	s Trigger/Sync	hronization wh	nen the broadc	ast command is	s executed	
	0 = Does not	generate Trigg	jer/Synchroniz	ation when the	e broadcast con	nmand is execu	ited
bit 10	IC3TSS: Irig	ger/Synchroniz	ation Source	for IC3 bit	act command is	avagutad	
	0 = Does not	generate Trigo	er/Synchroniz	ation when the	e broadcast con	nmand is execu	ited
bit 9	IC2TSS: Trig	ger/Synchroniz	ation Source	for IC2 bit			
	1 = Generate	s Trigger/Sync	hronization wh	nen the broadd	ast command is	s executed	
	0 = Does not	generate Trigg	jer/Synchroniz	ation when the	e broadcast con	nmand is execu	ited
bit 8	IC1TSS: Trig	ger/Synchroniz	ation Source	for IC1 bit			
	0 = Does not	aenerate Triac	ier/Svnchroniz	ation when the	e broadcast con	nmand is execu	ited
bit 7	OC4CS: Cloc	ck Source for C	0C4 bit				
	1 = Generate	s clock pulse v	when the broad	dcast comman	d is executed		
	0 = Does not	generate clock	c pulse when t	he broadcast o	command is exe	ecuted	
bit 6	OC3CS: Cloc	ck Source for C	C3 bit		-l :		
	⊥ = Generate 0 = Does not	aenerate clock	onen the broad	he broadcast c	u is executed command is exe	ecuted	
bit 5	OC2CS: Cloc	ck Source for C	C2 bit				
	1 = Generate	s clock pulse v	when the broad	dcast comman	d is executed		
	0 = Does not	generate clock	c pulse when t	he broadcast o	command is exe	ecuted	
Note 1:	This register is rea PTGSTRT = 1).	ad-only when th	ne PTG modul	e is executing	Step commands	s (PTGEN = 1 a	and
2:	This register is onl	v used with the	PTGCTRL O	PTION = 1111	Step command	1.	

REGISTER 24-3: PTGBTE: PTG BROADCAST TRIGGER ENABLE REGISTER^(1,2)

REGISTER 24-10: PTGADJ: PTG ADJUST REGISTER⁽¹⁾

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
			PTGA	DJ<15:8>			
bit 15							bit 8
R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
			PTGA	DJ<7:0>			
bit 7							bit 0
Legend:							
R = Readable bit W = Writable bit			bit	U = Unimplemented bit, read as '0'			
-n = Value at POR '1' = Bit is set			'0' = Bit is cleared x = Bit is unkno		nown		

bit 15-0 **PTGADJ<15:0>:** PTG Adjust Register bits This register holds user-supplied data to be added to the PTGTxLIM, PTGCxLIM, PTGSDLIM or PTGL0 registers with the PTGADD command.

REGISTER 24-11: PTGL0: PTG LITERAL 0 REGISTER⁽¹⁾

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	
PTGL0<15:8>								
bit 15 bit 8								

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	
PTGL0<7:0>								
bit 7								

Legend:					
R = Readable bit	W = Writable bit	it U = Unimplemented bit, read as '0'			
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown		

bit 15-0 PTGL0<15:0>: PTG Literal 0 Register bits

This register holds the 16-bit value to be written to the AD1CHS0 register with the ${\tt PTGCTRL}$ Step command.

Note 1: This register is read-only when the PTG module is executing Step commands (PTGEN = 1 and PTGSTRT = 1).

Note 1: This register is read-only when the PTG module is executing Step commands (PTGEN = 1 and PTGSTRT = 1).







25.3 Op Amp/Comparator Registers

R/W-0	U-0	U-0	U-0	R-0	R-0	R-0	R-0
PSIDL				C4EVT ⁽¹⁾	C3EVT ⁽¹⁾	C2EVT ⁽¹⁾	C1EVT ⁽¹⁾
bit 15				1	L		bit 8
U-0	U-0	U-0	U-0	R-0	R-0	R-0	R-0
		—		C4OUT ⁽²⁾	C3OUT ⁽²⁾	C2OUT ⁽²⁾	C10UT ⁽²⁾
bit 7							bit 0
r							
Legend:							
R = Readable	bit	W = Writable	bit	U = Unimpler	nented bit, read	l as '0'	
-n = Value at P	POR	'1' = Bit is set		0' = Bit is cle	ared	x = Bit is unkn	iown
hit 15		arator Stop in	dla Mada hit				
DIL 15	1 = Discontinu	ues operation of	of all comparat	ors when devi	ce enters Idle n	node	
	0 = Continues	operation of a	Il comparators	s in Idle mode			
bit 14-12	Unimplement	ted: Read as ')'				
bit 11	C4EVT: Op A	mp/Comparato	r 4 Event Stat	us bit ⁽¹⁾			
	1 = Op amp/c	omparator eve	nt occurred				
h# 40	0 = Op amp/c	omparator eve		Jr			
DIE TU	1 = Comparat	or event occur	Status Diter				
	0 = Comparat	or event did no	ot occur				
bit 9	C2EVT: Comp	parator 2 Event	: Status bit ⁽¹⁾				
	1 = Comparat	or event occur	red				
	0 = Comparat	or event did no	ot occur				
bit 8	C1EVT: Comp	parator 1 Event	Status bit ⁽¹⁾				
	1 = Comparat	or event occur	rea ot occur				
bit 7-4	Unimplement	ted: Read as ')'				
bit 3	C4OUT: Com	parator 4 Outp	ut Status bit ⁽²⁾				
	When CPOL =	<u>= 0:</u>					
	1 = VIN + > VIN	N-					
	0 = VIN + < VIN	N- = 1 ·					
	1 = VIN + < VIN	<u> </u>					
	0 = VIN + > VIN	N-					
bit 2	C3OUT: Com	parator 3 Outp	ut Status bit ⁽²⁾				
	When CPOL = $1 = V_{\rm IN} + > V_{\rm IN}$	<u>= 0:</u>					
	0 = VIN + < VIN	N- N-					
	When CPOL =	= 1:					
	1 = VIN + < VIN	N-					
	v = v i N + > V I N	N-					

REGISTER 25-1: CMSTAT: OP AMP/COMPARATOR STATUS REGISTER

- **Note 1:** Reflects the value of the of the CEVT bit in the respective Op Amp/Comparator Control register, CMxCON<9>.
 - 2: Reflects the value of the COUT bit in the respective Op Amp/Comparator Control register, CMxCON<8>.

27.2 User ID Words

dsPIC33EPXXXGP50X, dsPIC33EPXXXMC20X/50X and PIC24EPXXXGP/MC20X devices contain four User ID Words, located at addresses, 0x800FF8 through 0x800FFE. The User ID Words can be used for storing product information such as serial numbers, system manufacturing dates, manufacturing lot numbers and other application-specific information.

The User ID Words register map is shown in Table 27-3.

TABLE 27-3:USER ID WORDS REGISTER
MAP

File Name	Address	Bits 23-16	Bits 15-0
FUID0	0x800FF8	—	UID0
FUID1	0x800FFA	—	UID1
FUID2	0x800FFC	—	UID2
FUID3	0x800FFE	—	UID3

Legend: — = unimplemented, read as '1'.

27.3 On-Chip Voltage Regulator

All of the dsPIC33EPXXXGP50X, dsPIC33EPXXXMC20X/50X and PIC24EPXXXGP/ MC20X devices power their core digital logic at a nominal 1.8V. This can create a conflict for designs that are required to operate at a higher typical voltage, such as 3.3V. To simplify system design, all devices in the dsPIC33EPXXXGP50X, dsPIC33EPXXXMC20X/50X and PIC24EPXXXGP/MC20X family incorporate an onchip regulator that allows the device to run its core logic from VDD.

The regulator provides power to the core from the other VDD pins. A low-ESR (less than 1 Ohm) capacitor (such as tantalum or ceramic) must be connected to the VCAP pin (Figure 27-1). This helps to maintain the stability of the regulator. The recommended value for the filter capacitor is provided in Table 30-5 located in **Section 30.0 "Electrical Characteristics"**.

Note: It is important for the low-ESR capacitor to be placed as close as possible to the VCAP pin.

FIGURE 27-1: CONNECTIONS FOR THE ON-CHIP VOLTAGE

REGULATOR^(1,2,3)



27.4 Brown-out Reset (BOR)

The Brown-out Reset (BOR) module is based on an internal voltage reference circuit that monitors the regulated supply voltage, VCAP. The main purpose of the BOR module is to generate a device Reset when a brown-out condition occurs. Brown-out conditions are generally caused by glitches on the AC mains (for example, missing portions of the AC cycle waveform due to bad power transmission lines or voltage sags due to excessive current draw when a large inductive load is turned on).

A BOR generates a Reset pulse, which resets the device. The BOR selects the clock source, based on the device Configuration bit values (FNOSC<2:0> and POSCMD<1:0>).

If an oscillator mode is selected, the BOR activates the Oscillator Start-up Timer (OST). The system clock is held until OST expires. If the PLL is used, the clock is held until the LOCK bit (OSCCON<5>) is '1'.

Concurrently, the PWRT Time-out (TPWRT) is applied before the internal Reset is released. If TPWRT = 0 and a crystal oscillator is being used, then a nominal delay of TFSCM is applied. The total delay in this case is TFSCM. Refer to Parameter SY35 in Table 30-22 of **Section 30.0 "Electrical Characteristics"** for specific TFSCM values.

The BOR status bit (RCON<1>) is set to indicate that a BOR has occurred. The BOR circuit continues to operate while in Sleep or Idle modes and resets the device should VDD fall below the BOR threshold voltage.



FIGURE 30-36: ADC CONVERSION (12-BIT MODE) TIMING CHARACTERISTICS (ASAM = 0, SSRC<2:0> = 000, SSRCG = 0)

NOTES:

44-Terminal Very Thin Leadless Array Package (TL) – 6x6x0.9 mm Body With Exposed Pad [VTLA]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



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44-Lead Plastic Quad Flat, No Lead Package (ML) - 8x8 mm Body [QFN]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



	MILLIMETERS				
Dimension	Limits	MIN	NOM	MAX	
Number of Pins	N		44		
Pitch	е		0.65 BSC		
Overall Height	A	0.80	0.90	1.00	
Standoff	A1	0.00	0.02	0.05	
Terminal Thickness	A3	0.20 REF			
Overall Width	E		8.00 BSC		
Exposed Pad Width	E2	6.25	6.45	6.60	
Overall Length	D		8.00 BSC		
Exposed Pad Length	D2	6.25	6.45	6.60	
Terminal Width	b	0.20	0.30	0.35	
Terminal Length	Terminal Length L 0.30 0.40			0.50	
Terminal-to-Exposed-Pad	K	0.20	-	-	

Notes:

1. Pin 1 visual index feature may vary, but must be located within the hatched area.

2. Package is saw singulated

3. Dimensioning and tolerancing per ASME Y14.5M

BSC: Basic Dimension. Theoretically exact value shown without tolerances.

REF: Reference Dimension. usually without tolerance. for information purposes only.

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44-Lead Plastic Quad Flat, No Lead Package (ML) - 8x8 mm Body [QFN]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



	MILLIMETERS			
Dimension	Limits	MIN	NOM	MAX
Contact Pitch	E		0.65 BSC	
Optional Center Pad Width	W2			6.60
Optional Center Pad Length	T2			6.60
Contact Pad Spacing	C1		8.00	
Contact Pad Spacing	C2		8.00	
Contact Pad Width (X44)	X1			0.35
Contact Pad Length (X44)	Y1			0.85
Distance Between Pads	G	0.25		

Notes:

1. Dimensioning and tolerancing per ASME Y14.5M

BSC: Basic Dimension. Theoretically exact value shown without tolerances.

Microchip Technology Drawing No. C04-2103B