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"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "<u>Embedded -</u> <u>Microcontrollers</u>"

Details

E·XFI

Product Status	Active
Core Processor	PIC
Core Size	16-Bit
Speed	70 MIPs
Connectivity	I ² C, IrDA, LINbus, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, DMA, POR, PWM, WDT
Number of I/O	35
Program Memory Size	128KB (43K x 24)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	8K x 16
Voltage - Supply (Vcc/Vdd)	3V ~ 3.6V
Data Converters	A/D 9x10b/12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	44-VQFN Exposed Pad
Supplier Device Package	44-QFN (8x8)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/pic24ep128gp204-i-ml

Email: info@E-XFL.COM

Address: Room A, 16/F, Full Win Commercial Centre, 573 Nathan Road, Mongkok, Hong Kong

Pin Name ⁽⁴⁾	Pin Type	Buffer Type	PPS	Description					
U2CTS	1	ST	No	UART2 Clear-To-Send.					
U2RTS	0		No	UART2 Ready-To-Send.					
U2RX	I.	ST	Yes	UART2 receive.					
U2TX	Ó	_	Yes	UART2 transmit.					
BCLK2	Ō	ST	No	UART2 IrDA [®] baud clock output.					
SCK1	I/O	ST	No	Synchronous serial clock input/output for SPI1.					
SDI1	I	ST	No	SPI1 data in.					
SDO1	0	—	No	SPI1 data out.					
SS1	I/O	ST	No	SPI1 slave synchronization or frame pulse I/O.					
SCK2	I/O	ST	Yes	Synchronous serial clock input/output for SPI2.					
SDI2	I	ST	Yes	SPI2 data in.					
SDO2	0	—	Yes	SPI2 data out.					
SS2	I/O	ST	Yes	SPI2 slave synchronization or frame pulse I/O.					
SCL1	I/O	ST	No	Synchronous serial clock input/output for I2C1.					
SDA1	I/O	ST	No	Synchronous serial data input/output for I2C1.					
ASCL1	I/O	ST	No	Alternate synchronous serial clock input/output for I2C1.					
ASDA1	I/O	ST	No	Alternate synchronous serial data input/output for I2C1.					
SCL2	I/O	ST	No	Synchronous serial clock input/output for I2C2.					
SDA2	I/O	ST	No	Synchronous serial data input/output for I2C2.					
ASCL2	I/O	ST	No	Alternate synchronous serial clock input/output for I2C2.					
ASDA2	I/O	ST	No	Alternate synchronous serial data input/output for I2C2.					
TMS ⁽⁵⁾	Ι	ST	No	JTAG Test mode select pin.					
TCK	I	ST	No	JTAG test clock input pin.					
TDI	I	ST	No	JTAG test data input pin.					
TDO	0	_	No	JTAG test data output pin.					
C1RX ⁽²⁾	I	ST	Yes	ECAN1 bus receive pin.					
C1TX ⁽²⁾	0	_	Yes	ECAN1 bus transmit pin.					
FLT1 ⁽¹⁾ , FLT2 ⁽¹⁾	I	ST	Yes	PWM Fault Inputs 1 and 2.					
FLT3 ⁽¹⁾ , FLT4 ⁽¹⁾	I	ST	No	PWM Fault Inputs 3 and 4.					
FLT32 ^(1,3)	I	ST	No	PWM Fault Input 32 (Class B Fault).					
DTCMP1-DTCMP3 ⁽¹⁾	I	ST	Yes	PWM Dead-Time Compensation Inputs 1 through 3.					
PWM1L-PWM3L ⁽¹⁾	0	—	No	PWM Low Outputs 1 through 3.					
PWM1H-PWM3H ⁽¹⁾	0	—	No	PWM High Outputs 1 through 3.					
SYNCI1 ⁽¹⁾	I	ST	Yes	PWM Synchronization Input 1.					
SYNCO1 ⁽¹⁾	0	—	Yes	PWM Synchronization Output 1.					
INDX1 ⁽¹⁾	Ι	ST	Yes	Quadrature Encoder Index1 pulse input.					
HOME1 ⁽¹⁾	I	ST	Yes	Quadrature Encoder Home1 pulse input.					
QEA1 ⁽¹⁾	I	ST	Yes	Quadrature Encoder Phase A input in QEI1 mode. Auxiliary timer					
(4)				external clock/gate input in Timer mode.					
QEB1 ⁽¹⁾	I	ST	Yes	Quadrature Encoder Phase B input in QEI1 mode. Auxiliary timer					
				external clock/gate input in Timer mode.					
CNTCMP1''	υ	—	Yes	Quadrature Encoder Compare Output 1.					

TABLE 1-1: PINOUT I/O DESCRIPTIONS (CONTINUED)

 Legend:
 CMOS = CMOS compatible input or output
 Analog = Analog input

 ST = Schmitt Trigger input with CMOS levels
 O = Output

 PPS = Peripheral Pin Select
 TTL = TTL input buffer

P = Power I = Input

Note 1: This pin is available on dsPIC33EPXXXMC20X/50X and PIC24EPXXXMC20X devices only.

2: This pin is available on dsPIC33EPXXXGP/MC50X devices only.

3: This is the default Fault on Reset for dsPIC33EPXXXMC20X/50X and PIC24EPXXXMC20X devices. See Section 16.0 "High-Speed PWM Module (dsPIC33EPXXXMC20X/50X and PIC24EPXXXMC20X Devices Only)" for more information.

4: Not all pins are available in all packages variants. See the "Pin Diagrams" section for pin availability.

5: There is an internal pull-up resistor connected to the TMS pin when the JTAG interface is active. See the JTAGEN bit field in Table 27-2.



2.2.1 TANK CAPACITORS

On boards with power traces running longer than six inches in length, it is suggested to use a tank capacitor for integrated circuits including DSCs to supply a local power source. The value of the tank capacitor should be determined based on the trace resistance that connects the power supply source to the device and the maximum current drawn by the device in the application. In other words, select the tank capacitor so that it meets the acceptable voltage sag at the device. Typical values range from 4.7 μ F to 47 μ F.

2.3 CPU Logic Filter Capacitor Connection (VCAP)

A low-ESR (< 1 Ohm) capacitor is required on the VCAP pin, which is used to stabilize the voltage regulator output voltage. The VCAP pin must not be connected to VDD and must have a capacitor greater than 4.7 μ F (10 μ F is recommended), 16V connected to ground. The type can be ceramic or tantalum. See **Section 30.0** "**Electrical Characteristics**" for additional information.

The placement of this capacitor should be close to the VCAP pin. It is recommended that the trace length not exceeds one-quarter inch (6 mm). See **Section 27.3 "On-Chip Voltage Regulator"** for details.

2.4 Master Clear (MCLR) Pin

The MCLR pin provides two specific device functions:

- Device Reset
- Device Programming and Debugging.

During device programming and debugging, the resistance and capacitance that can be added to the pin must be considered. Device programmers and debuggers drive the MCLR pin. Consequently, specific voltage levels (VIH and VIL) and fast signal transitions must not be adversely affected. Therefore, specific values of R and C will need to be adjusted based on the application and PCB requirements.

For example, as shown in Figure 2-2, it is recommended that the capacitor, C, be isolated from the $\overline{\text{MCLR}}$ pin during programming and debugging operations.

Place the components as shown in Figure 2-2 within one-quarter inch (6 mm) from the MCLR pin.





File Name	Addr	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	All
	0.400								Cas dafini	tion								Resets
	0400- 041E								See defini	tion when wi	IN = x							
C1BUFPNT1	0420		F3B	P<3:0>			F2BI	><3:0>			F1BP	o<3:0>			F0BP	<3:0>		0000
C1BUFPNT2	0422		F7B	P<3:0>			F6BI	><3:0>			F5BP	2 <3:0>			F4BP	<3:0>		0000
C1BUFPNT3	0424		F11B	3P<3:0>		F10BP<3:0>			F9BP<3:0>			F8BP<3:0>				0000		
C1BUFPNT4	0426		F15E	3P<3:0>		F14BP<3:0>			F13BP<3:0>			F12BP<3:0>				0000		
C1RXM0SID	0430				SID	:10:3>					SID<2:0>		_	MIDE	_	EID<	17:16>	xxxx
C1RXM0EID	0432				EID≪	:15:8>							EID<	:7:0>				xxxx
C1RXM1SID	0434				SID	:10:3>					SID<2:0>		—	MIDE	—	EID<	17:16>	xxxx
C1RXM1EID	0436				EID<	:15:8>							EID<	:7:0>				xxxx
C1RXM2SID	0438				SID<	:10:3>					SID<2:0>		—	MIDE	—	EID<	17:16>	xxxx
C1RXM2EID	043A				EID<	:15:8>							EID<	7:0>		-		xxxx
C1RXF0SID	0440				SID<	:10:3>					SID<2:0>		—	EXIDE	—	EID<	17:16>	xxxx
C1RXF0EID	0442				EID<	:15:8>							EID<	7:0>		-		xxxx
C1RXF1SID	0444				SID<	:10:3>					SID<2:0>		—	EXIDE	—	EID<	17:16>	xxxx
C1RXF1EID	0446		EID<15:8>							EID<	:7:0>		-		xxxx			
C1RXF2SID	0448				SID<	:10:3>					SID<2:0>		—	EXIDE	_	EID<	17:16>	xxxx
C1RXF2EID	044A				EID<	:15:8>							EID<	:7:0>	_	_		xxxx
C1RXF3SID	044C				SID<	:10:3>					SID<2:0>			EXIDE	_	EID<	17:16>	xxxx
C1RXF3EID	044E				EID<	:15:8>				EID<				<7:0>				xxxx
C1RXF4SID	0450				SID<	:10:3>					SID<2:0>			EXIDE	_	EID<	17:16>	xxxx
C1RXF4EID	0452				EID<	:15:8>							EID<	:7:0>	_	_		xxxx
C1RXF5SID	0454				SID<	:10:3>					SID<2:0>			EXIDE	_	EID<	17:16>	xxxx
C1RXF5EID	0456				EID<	:15:8>							EID<	:7:0>	_	_		xxxx
C1RXF6SID	0458				SID<	:10:3>					SID<2:0>			EXIDE	_	EID<	17:16>	xxxx
C1RXF6EID	045A				EID<	:15:8>							EID<	:7:0>		-		xxxx
C1RXF7SID	045C				SID<	:10:3>				_	SID<2:0>			EXIDE	—	EID<	17:16>	xxxx
C1RXF7EID	045E				EID<	:15:8>							EID<	:7:0>	_	_		xxxx
C1RXF8SID	0460				SID<	:10:3>					SID<2:0>			EXIDE	_	EID<	17:16>	xxxx
C1RXF8EID	0462				EID<	:15:8>							EID<	:7:0>	_	_		xxxx
C1RXF9SID	0464				SID<	:10:3>					SID<2:0>			EXIDE	_	EID<	17:16>	xxxx
C1RXF9EID	0466				EID<	:15:8>							EID<	:7:0>		-		xxxx
C1RXF10SID	0468				SID<	:10:3>					SID<2:0>		—	EXIDE	—	EID<	17:16>	xxxx
C1RXF10EID	046A				EID	:15:8>							EID<	7:0>		_		xxxx
C1RXF11SID	046C				SID	:10:3>					SID<2:0>		—	EXIDE	_	EID<	17:16>	xxxx

TABLE 4-23: ECAN1 REGISTER MAP WHEN WIN (C1CTRL1<0>) = 1 FOR dsPIC33EPXXXMC/GP50X DEVICES ONLY

Legend: x = unknown value on Reset, — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

TABLE 4-49: PORTD REGISTER MAP FOR PIC24EPXXXGP/MC206 AND dsPIC33EPXXXGP/MC206/506 DEVICES ONLY

File Name	Addr.	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	All Resets
TRISD	0E30			_	_	—			TRISD8	_	TRISD6	TRISD5	_					0160
PORTD	0E32	_	_	_	_	_	_	_	RD8	_	RD6	RD5		_	_	_	_	xxxx
LATD	0E34	_	_	_	_	_	_	_	LATD8	_	LATD6	LATD5		_	_	_	_	xxxx
ODCD	0E36	_	_	_	_	_	_	_	ODCD8	_	ODCD6	ODCD5		_	_	_	_	0000
CNEND	0E38	_	_	_	_	_	_	_	CNIED8	_	CNIED6	CNIED5		_	_	_	_	0000
CNPUD	0E3A	_	_	_	_	_	_	_	CNPUD8	_	CNPUD6	CNPUD5	_	_	_	_	_	0000
CNPDD	0E3C	_	_	_	_	_	_	_	CNPDD8	_	CNPDD6	CNPDD5		_	_	_	_	0000

Legend: x = unknown value on Reset, - = unimplemented, read as '0'. Reset values are shown in hexadecimal.

TABLE 4-50: PORTE REGISTER MAP FOR PIC24EPXXXGP/MC206 AND dsPIC33EPXXXGP/MC206/506 DEVICES ONLY

File Name	Addr.	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	All Resets
TRISE	0E40	TRISE15	TRISE14	TRISE13	TRISE12	-	_	_	—	_	-	-	_	—	—	—	—	F000
PORTE	0E42	RE15	RE14	RE13	RE12	—	_	_	_	—	_		_	—	—	_	_	xxxx
LATE	0E44	LATE15	LATE14	LATE13	LATE12	—	_	_	_	_	_	_	_		—	_	_	xxxx
ODCE	0E46	ODCE15	ODCE14	ODCE13	ODCE12	—	—	—	—	-	—	—	—	-	—	—	—	0000
CNENE	0E48	CNIEE15	CNIEE14	CNIEE13	CNIEE12	—	_	_	_	—	_		_	—	—	_	_	0000
CNPUE	0E4A	CNPUE15	CNPUE14	CNPUE13	CNPUE12	—	_	_	_	—	_	_	_	_	—	_	_	0000
CNPDE	0E4C	CNPDE15	CNPDE14	CNPDE13	CNPDE12	—	_	_	—	—	_	_	_	—	—	—	_	0000
ANSELE	0E4E	ANSE15	ANSE14	ANSE13	ANSE12	—	_	—	_	_	—	_	—	—	—	_		F000

Legend: x = unknown value on Reset, - = unimplemented, read as '0'. Reset values are shown in hexadecimal.

TABLE 4-51: PORTF REGISTER MAP FOR PIC24EPXXXGP/MC206 AND dsPIC33EPXXXGP/MC206/506 DEVICES ONLY

File Name	Addr.	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	All Resets
TRISF	0E50	—	—	_	—	—	_	—	_	—	_	—	_	_	_	TRISF1	TRISF0	0003
PORTF	0E52	—	—	—	_	—	_	_	_	—	_	—	_	_	_	RF1	RF0	xxxx
LATF	0E54	—	—	—	—	—	—	_	_	—	—	—	—	_	_	LATF1	LATF0	xxxx
ODCF	0E56	_	—	-	-	—	_	_	_	—		—		_	_	ODCF1	ODCF0	0000
CNENF	0E58		—		-	—	—	_	—	—	-	—		—	—	CNIEF1	CNIEF0	0000
CNPUF	0E5A	—	—	—	—	—	—	_	_	—	—	—	—	_	_	CNPUF1	CNPUF0	0000
CNPDF	0E5C	_	—	-	-	—	_	_	_	—		—		_	_	CNPDF1	CNPDF0	0000

Legend: x = unknown value on Reset, - = unimplemented, read as '0'. Reset values are shown in hexadecimal.

NOTES:

NOTES:

14.2 Input Capture Registers

REGISTER 14-1: ICxCON1: INPUT CAPTURE x CONTROL REGISTER 1

U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	U-0	U-0
—	—	ICSIDL	ICTSEL2	ICTSEL1	ICTSEL0	_	—
bit 15							bit 8

U-0	R/W-0	R/W-0	R/HC/HS-0	R/HC/HS-0	R/W-0	R/W-0	R/W-0
—	ICI1	ICI0	ICOV	ICBNE	ICM2	ICM1	ICM0
bit 7							bit 0

Legend:	HC = Hardware Clearable bit	HS = Hardware Settable bit	
R = Readable bit	W = Writable bit	U = Unimplemented bit, rea	d as '0'
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15-14	Unimplemented: Read as '0'
bit 13	ICSIDL: Input Capture Stop in Idle Control bit
	1 = Input capture will Halt in CPU Idle mode
	0 = Input capture will continue to operate in CPU Idle mode
bit 12-10	ICTSEL<2:0>: Input Capture Timer Select bits
	111 = Peripheral clock (FP) is the clock source of the ICx
	110 = Reserved
	101 = Reserved
	100 - 11 CLR is the clock source of the ICx (only the synchronous clock is supported) 011 = T5CLK is the clock source of the ICx
	010 = T4CLK is the clock source of the ICx
	001 = T2CLK is the clock source of the ICx
	000 = T3CLK is the clock source of the ICx
bit 9-7	Unimplemented: Read as '0'
bit 6-5	ICI<1:0>: Number of Captures per Interrupt Select bits (this field is not used if ICM<2:0> = 001 or 111)
	11 = Interrupt on every fourth capture event
	10 = Interrupt on every third capture event
	01 = Interrupt on every second capture event
hit 4	ICOV: Input Capture Overflow Status Flag bit (read-only)
Dit 4	1 = Input capture buffer overflow occurred
	0 = No input capture buffer overflow occurred
bit 3	ICBNE: Input Capture Buffer Not Empty Status bit (read-only)
	1 = Input capture buffer is not empty, at least one more capture value can be read
	0 = Input capture buffer is empty
bit 2-0	ICM<2:0>: Input Capture Mode Select bits
	111 = Input capture functions as interrupt pin only in CPU Sleep and Idle modes (rising edge detect only, all other control bits are not applicable)
	110 = Unused (module is disabled)
	101 = Capture mode, every 16th rising edge (Prescaler Capture mode)
	100 = Capture mode, every 4th rising edge (Prescaler Capture mode)
	011 = Capture mode, every falling edge (Simple Capture mode)
	001 = Capture mode, every edge rising and falling (Edge Detect mode (ICI<1:0>) is not used in this mode)
	000 = Input capture module is turned off

U-0	U-0	U-0	U-0	U-0	U-0	U-0	R/W-0
—	—	—	—	—	—	—	IC32
bit 15							bit 8
R/W-0	R/W/HS-0	U-0	R/W-0	R/W-1	R/W-1	R/W-0	R/W-1

REGISTER 14-2: ICxCON2: INPUT CAPTURE x CONTROL REGISTER 2

bit 7			bit 0
Legend:	HS = Hardware Settal	ble bit	
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	

SYNCSEL4⁽⁴⁾ SYNCSEL3⁽⁴⁾ SYNCSEL2⁽⁴⁾ SYNCSEL1⁽⁴⁾

SYNCSEL0⁽⁴⁾

		P	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15-9 Unimplemented: Read as '0'

TRIGSTAT⁽³⁾

ICTRIG⁽²⁾

bit 8

- IC32: Input Capture 32-Bit Timer Mode Select bit (Cascade mode)
 - 1 = Odd IC and Even IC form a single 32-bit input capture module⁽¹⁾
 - 0 = Cascade module operation is disabled

bit 7 ICTRIG: Input Capture Trigger Operation Select bit⁽²⁾

- 1 = Input source used to trigger the input capture timer (Trigger mode)
- 0 = Input source used to synchronize the input capture timer to a timer of another module (Synchronization mode)

bit 6 **TRIGSTAT:** Timer Trigger Status bit⁽³⁾

- 1 = ICxTMR has been triggered and is running
- 0 = ICxTMR has not been triggered and is being held clear

bit 5 Unimplemented: Read as '0'

- **Note 1:** The IC32 bit in both the Odd and Even IC must be set to enable Cascade mode.
 - 2: The input source is selected by the SYNCSEL<4:0> bits of the ICxCON2 register.
 - **3:** This bit is set by the selected input source (selected by SYNCSEL<4:0> bits). It can be read, set and cleared in software.
 - 4: Do not use the ICx module as its own Sync or Trigger source.
 - 5: This option should only be selected as a trigger source and not as a synchronization source.
 - 6: Each Input Capture x (ICx) module has one PTG input source. See Section 24.0 "Peripheral Trigger Generator (PTG) Module" for more information.

PTGO8 = IC1 PTGO9 = IC2 PTGO10 = IC3 PTGO11 = IC4

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15.2 Output Compare Control Registers

REGISTER 15-1: OCxCON1: OUTPUT COMPARE x CONTROL REGISTER 1

U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	U-0	R/W-0		
		OCSIDL	OCTSEL2	OCTSEL1	OCTSEL0	_	ENFLTB		
bit 15							bit 8		
R/W-0	U-0	R/W-0, HSC	R/W-0, HSC	R/W-0	R/W-0	R/W-0	R/W-0		
ENFLTA		OCFLTB	OCFLTA	TRIGMODE	OCM2	OCM1	OCM0		
bit 7							bit 0		
Legend:		HSC = Hardw	are Settable/Cl	earable bit					
R = Reada	ible bit	W = Writable I	bit	U = Unimplem	nented bit, read	as '0'			
-n = Value	at POR	'1' = Bit is set		'0' = Bit is clea	ared	x = Bit is unkr	nown		
bit 15-14	Unimplemen	ted: Read as '0)'						
bit 13	OCSIDL: Out	tput Compare x	Stop in Idle Mo	de Control bit					
	1 = Output C	compare x Halts	in CPU Idle me	ode via CDU Idia m	odo				
bit 12 10			nues lo operale		oue				
DIL 12-10	111 = Perinh	eral clock (Ep)	pare x Clock S						
	110 = Reserv	/ed							
	101 = PTGO	x clock ⁽²⁾							
	100 = T1CLK	is the clock so	urce of the OC	k (only the sync	hronous clock	is supported)			
	011 = 15CLK	is the clock sou	urce of the OC	Х У					
	010 = T4CLK 001 = T3CLK	is the clock so	urce of the OC	x X					
	000 = T2CLK	is the clock so	urce of the OC	ĸ					
bit 9	Unimplemen	ted: Read as '0)'						
bit 8	ENFLTB: Fau	ult B Input Enab	le bit						
	1 = Output C 0 = Output C	compare Fault B compare Fault B	input (OCFB) input (OCFB)	is enabled is disabled					
bit 7	ENFLTA: Fau	ult A Input Enabl	le bit						
	1 = Output C	ompare Fault A	input (OCFA)	is enabled					
	0 = Output C	ompare Fault A	input (OCFA)	is disabled					
bit 6	Unimplemen	ted: Read as '0)'						
bit 5	OCFLTB: PW	M Fault B Cond	dition Status bit						
	1 = PWM Fa 0 = No PWM	ult B condition of Fault B condition	on OCFB pin ha on on OCFB pi	as occurred n has occurred					
bit 4	OCFLTA: PW	/M Fault A Cond	dition Status bit						
	1 = PWM Fault A condition on OCFA pin has occurred								
	0 = No PWM	I Fault A condition	on on OCFA pi	n has occurred					
Note 1:	OCxR and OCxF	RS are double-b	ouffered in PWN	A mode only.					
2:	Each Output Cor	mpare x module	(OCx) has one	PTG clock sou	urce. See Secti	on 24.0 "Perip	oheral Trigger		
	Generator (PTG PTGO4 = OC1) wodule" for r	nore informatio	n.					
	PTGO5 = OC2								
	PTGO6 = OC3								
	PTGO7 = OC4	PTG07 = 0C4							

R-0, HSC	R-0, HSC	U-0	U-0	U-0	R/C-0, HS	R-0, HSC	R-0, HSC
ACKSTAT	TRSTAT	_	—	—	BCL	GCSTAT	ADD10
bit 15					•		bit 8
R/C-0, HS	R/C-0, HS	R-0, HSC	R/C-0, HSC	R/C-0, HSC	R-0, HSC	R-0, HSC	R-0, HSC
IWCOL	I2COV	D_A	Р	S	R_W	RBF	TBF
bit 7							bit 0
Legend:		C = Clearab	le bit	HS = Hardwa	re Settable bit	HSC = Hardware S	ettable/Clearable bit
R = Readable bit W = Writable bit			U = Unimplemented bit, read as '0'				
-n = Value at POR '1' = Bit is set '0'		'0' = Bit is cleared x = Bit is unknown					

REGISTER 19-2: I2CxSTAT: I2Cx STATUS REGISTER

bit 15	ACKSTAT: Acknowledge Status bit (when operating as I^2C^{TM} master, applicable to master transmit operation)
	1 = NACK received from slave 0 = ACK received from slave
	Hardware is set or clear at the end of slave Acknowledge.
bit 14	TRSTAT: Transmit Status bit (when operating as I^2C master, applicable to master transmit operation) 1 = Master transmit is in progress (8 bits + ACK)
	0 = Master transmit is not in progress Hardware is set at the beginning of master transmission. Hardware is clear at the end of slave Acknowledge.
bit 13-11	Unimplemented: Read as '0'
bit 10	BCL: Master Bus Collision Detect bit
	1 = A bus collision has been detected during a master operation0 = No bus collision detected
	Hardware is set at detection of a bus collision.
bit 9	GCSTAT: General Call Status bit
	1 = General call address was received
	0 = General call address was not received
1.11.0	Hardware is set when address matches general call address. Hardware is clear at Stop detection.
DIT 8	ADD10: 10-Bit Address Status bit
	I = 10-bit address was matched 0 = 10-bit address was not matched
	Hardware is set at the match of the 2nd byte of the matched 10-bit address. Hardware is clear at Stop detection.
bit 7	IWCOL: I2Cx Write Collision Detect bit
	1 = An attempt to write to the I2CxTRN register failed because the I^2 C module is busy 0 = No collision
	Hardware is set at the occurrence of a write to I2CxTRN while busy (cleared by software).
bit 6	I2COV: I2Cx Receive Overflow Flag bit
	 1 = A byte was received while the I2CxRCV register was still holding the previous byte 0 = No overflow
	Hardware is set at an attempt to transfer I2CxRSR to I2CxRCV (cleared by software).
bit 5	D_A: Data/Address bit (when operating as I ² C slave)
	1 = Indicates that the last byte received was data
	 Indicates that the last byte received was a device address Hardware is clear at a device address match. Hardware is set by reception of a slave byte.
bit 4	P: Stop bit
	1 = Indicates that a Stop bit has been detected last
	0 = Stop bit was not detected last
	Hardware is set or clear when a Start, Repeated Start or Stop is detected.

REGISTER 19-2: I2CxSTAT: I2Cx STATUS REGISTER (CONTINUED)

bit 3	S: Start bit
	1 = Indicates that a Start (or Repeated Start) bit has been detected last
	0 = Start bit was not detected last
	Hardware is set or clear when a Start, Repeated Start or Stop is detected.
bit 2	R_W: Read/Write Information bit (when operating as I ² C slave)
	1 = Read – Indicates data transfer is output from the slave
	0 = Write – Indicates data transfer is input to the slave
	Hardware is set or clear after reception of an I ² C device address byte.
bit 1	RBF: Receive Buffer Full Status bit
	1 = Receive is complete, I2CxRCV is full
	0 = Receive is not complete, I2CxRCV is empty
	Hardware is set when I2CxRCV is written with a received byte. Hardware is clear when software reads
	I2CxRCV.
bit 0	TBF: Transmit Buffer Full Status bit
	1 = Transmit in progress, I2CxTRN is full
	0 = Transmit is complete, I2CxTRN is empty
	Hardware is set when software writes to I2CxTRN. Hardware is clear at completion of a data transmission.

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R/W-0	R/W-0	R/W-0	U-0	R/W-0, HC	R/W-0	R-0	R-1
UTXISEL1	UTXINV	UTXISEL0	—	UTXBRK	UTXEN ⁽¹⁾	UTXBF	TRMT
bit 15							bit 8
R/W-0	R/W-0	R/W-0	R-1	R-0	R-0	R/C-0	R-0
URXISEL1	URXISEL0	ADDEN	RIDLE	PERR	FERR	OERR	URXDA
bit 7							bit 0
Legend:		HC = Hardwar	e Clearable bit	C = Clearable	e bit		
R = Readable	bit	W = Writable b	bit	U = Unimpler	mented bit, read	d as '0'	

REGISTER 20-2: UxSTA: UARTx STATUS AND CONTROL REGISTER

R = Readable bit	W = Writable bit	U = Unimplemented bit, read	d as '0'
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15,13 UTXISEL<1:0>: UARTx Transmission Interrupt Mode Selection bits

- 11 = Reserved; do not use
- 10 = Interrupt when a character is transferred to the Transmit Shift Register (TSR) and as a result, the transmit buffer becomes empty
- 01 = Interrupt when the last character is shifted out of the Transmit Shift Register; all transmit operations are completed
- 00 = Interrupt when a character is transferred to the Transmit Shift Register (this implies there is at least one character open in the transmit buffer)
- bit 14 UTXINV: UARTx Transmit Polarity Inversion bit
 - $\frac{\text{If IREN = 0:}}{1 = \text{UxTX Idle state is '0'}}$
 - 0 = UxTX Idle state is '1'
 - If IREN = 1:
 - 1 = IrDA encoded, UxTX Idle state is '1'
 - 0 = IrDA encoded, UxTX Idle state is '0'
- bit 12 Unimplemented: Read as '0'
- bit 11 UTXBRK: UARTx Transmit Break bit
 - 1 = Sends Sync Break on next transmission Start bit, followed by twelve '0' bits, followed by Stop bit; cleared by hardware upon completion
 - 0 = Sync Break transmission is disabled or completed
- bit 10 UTXEN: UARTx Transmit Enable bit⁽¹⁾ 1 = Transmit is enabled, UxTX pin is controlled by UARTx
 - 0 = Transmit is disabled, any pending transmission is aborted and buffer is reset; UxTX pin is controlled by the PORT
- bit 9 UTXBF: UARTx Transmit Buffer Full Status bit (read-only)
 - 1 = Transmit buffer is full
 - 0 = Transmit buffer is not full, at least one more character can be written
- bit 8 TRMT: Transmit Shift Register Empty bit (read-only)
 - 1 = Transmit Shift Register is empty and transmit buffer is empty (the last transmission has completed)
 - 0 = Transmit Shift Register is not empty, a transmission is in progress or queued
- bit 7-6 URXISEL<1:0>: UARTx Receive Interrupt Mode Selection bits
 - 11 = Interrupt is set on UxRSR transfer, making the receive buffer full (i.e., has 4 data characters)
 - 10 = Interrupt is set on UxRSR transfer, making the receive buffer 3/4 full (i.e., has 3 data characters)
 - 0x = Interrupt is set when any character is received and transferred from the UxRSR to the receive buffer; receive buffer has one or more characters
- **Note 1:** Refer to the "**UART**" (DS70582) section in the "*dsPIC33/PIC24 Family Reference Manual*" for information on enabling the UARTx module for transmit operation.

REGISTER 23-2: AD1CON2: ADC1 CONTROL REGISTER 2 (CONTINUED)

bit 1 BUFM: Buffer Fill Mode Select bit						
	 1 = Starts the buffer filling the first half of the buffer on the first interrupt and the second half of the buffer on next interrupt 0 = Always starts filling the buffer from the start address. 					
bit 0	ALTS: Alternate Input Sample Mode Select bit					

1 = Uses channel input selects for Sample MUXA on first sample and Sample MUXB on next sample 0 = Always uses channel input selects for Sample MUXA

REGISTER 24-8: PTGC1LIM: PTG COUNTER 1 LIMIT REGISTER⁽¹⁾

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0		
	PTGC1LIM<15:8>								
bit 15							bit 8		
R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0		
	PTGC1LIM<7:0>								
bit 7							bit 0		
Logond									

Legenu.				
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'		
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown	

bit 15-0 **PTGC1LIM<15:0>:** PTG Counter 1 Limit Register bits May be used to specify the loop count for the PTGJMPC1 Step command or as a limit register for the General Purpose Counter 1.

REGISTER 24-9: PTGHOLD: PTG HOLD REGISTER⁽¹⁾

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0		
PTGHOLD<15:8>									
bit 15							bit 8		

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0		
PTGHOLD<7:0>									
bit 7							bit 0		

Legend:					
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'			
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown		

bit 15-0 **PTGHOLD<15:0>:** PTG General Purpose Hold Register bits Holds user-supplied data to be copied to the PTGTxLIM, PTGCxLIM, PTGSDLIM or PTGL0 registers with the PTGCOPY command.

Note 1: This register is read-only when the PTG module is executing Step commands (PTGEN = 1 and PTGSTRT = 1).

Note 1: This register is read-only when the PTG module is executing Step commands (PTGEN = 1 and PTGSTRT = 1).

bit 3-0	Step Command	OPTION<3:0>	Option Description					
	PTGCTRL(1)	0000	Reserved.					
		0001	Reserved.					
		0010	Disable Step Delay Timer (PTGSD).					
		0011	Reserved.					
		0100	Reserved.					
		0101	Reserved.					
		0110	Enable Step Delay Timer (PTGSD).					
		0111	Reserved.					
		1000	Start and wait for the PTG Timer0 to match the Timer0 Limit Register.					
		1001	Start and wait for the PTG Timer1 to match the Timer1 Limit Register.					
		1010	Reserved.					
		1011	Wait for the software trigger bit transition from low-to-high before continuing (PTGSWT = 0 to 1).					
		1100	Copy contents of the Counter 0 register to the AD1CHS0 register.					
		1101	Copy contents of the Counter 1 register to the AD1CHS0 register.					
		1110	Copy contents of the Literal 0 register to the AD1CHS0 register.					
		1111	Generate triggers indicated in the Broadcast Trigger Enable register (PTGBTE).					
	PTGADD(1)	0000	Add contents of the PTGADJ register to the Counter 0 Limit register (PTGC0LIM).					
		0001	Add contents of the PTGADJ register to the Counter 1 Limit register (PTGC1LIM).					
		0010	Add contents of the PTGADJ register to the Timer0 Limit register (PTGT0LIM).					
		0011	Add contents of the PTGADJ register to the Timer1 Limit register (PTGT1LIM).					
		0100	Add contents of the PTGADJ register to the Step Delay Limit register (PTGSDLIM).					
		0101	Add contents of the PTGADJ register to the Literal 0 register (PTGL0).					
		0110	Reserved.					
		0111	Reserved.					
	PTGCOPY(1)	1000	Copy contents of the PTGHOLD register to the Counter 0 Limit register (PTGC0LIM).					
		1001	Copy contents of the PTGHOLD register to the Counter 1 Limit register (PTGC1LIM).					
		1010	Copy contents of the PTGHOLD register to the Timer0 Limit register (PTGT0LIM).					
		1011	Copy contents of the PTGHOLD register to the Timer1 Limit register (PTGT1LIM).					
		1100	Copy contents of the PTGHOLD register to the Step Delay Limit register (PTGSDLIM).					
		1101	Copy contents of the PTGHOLD register to the Literal 0 register (PTGL0).					
		1110	Reserved.					
		1111	Reserved.					

TABLE 24-1: PTG STEP COMMAND FORMAT (CONTINUED)

Note 1: All reserved commands or options will execute but have no effect (i.e., execute as a NOP instruction).

2: Refer to Table 24-2 for the trigger output descriptions.

3: This feature is only available on dsPIC33EPXXXMC20X/50X and PIC24EPXXXMC20X devices.

25.1 Op Amp Application Considerations

There are two configurations to take into consideration when designing with the op amp modules that available in the dsPIC33EPXXXGP50X. are dsPIC33EPXXXMC20X/50X and PIC24EPXXXGP/ MC20X devices. Configuration A (see Figure 25-6) takes advantage of the internal connection to the ADC module to route the output of the op amp directly to the ADC for measurement. Configuration B (see Figure 25-7) requires that the designer externally route the output of the op amp (OAxOUT) to a separate analog input pin (ANy) on the device. Table 30-55 in Section 30.0 "Electrical Characteristics" describes the performance characteristics for the op amps, distinguishing between the two configuration types where applicable.

25.1.1 OP AMP CONFIGURATION A

Figure 25-6 shows a typical inverting amplifier circuit taking advantage of the internal connections from the op amp output to the input of the ADC. The advantage of this configuration is that the user does not need to consume another analog input (ANy) on the device, and allows the user to simultaneously sample all three op amps with the ADC module, if needed. However, the presence of the internal resistance, RINT1, adds an error in the feedback path. Since RINT1 is an internal resistance, in relation to the op amp output (VOAXOUT) and ADC internal connection (VADC), RINT1 must be included in the numerator term of the transfer function. See Table 30-53 in Section 30.0 "Electrical Characteristics" for the typical value of RINT1. Table 30-60 and Table 30-61 in Section 30.0 "Electrical Characteristics" describe the minimum sample time (TSAMP) requirements for the ADC module in this configuration. Figure 25-6 also defines the equations that should be used when calculating the expected voltages at points, VADC and VOAXOUT.

FIGURE 25-6: OP AMP CONFIGURATION A



Note 1: See Table 30-53 for the Typical value.

- 2: See Table 30-53 for the Minimum value for the feedback resistor.
- 3: See Table 30-60 and Table 30-61 for the minimum sample time (TSAMP).
- 4: CVREF10 or CVREF20 are two options that are available for supplying bias voltage to the op amps.

REGISTER 25-1: CMSTAT: OP AMP/COMPARATOR STATUS REGISTER (CONTINUED)

- C2OUT: Comparator 2 Output Status bit⁽²⁾ bit 1 When CPOL = 0: 1 = VIN + > VIN -0 = VIN + < VIN-When CPOL = 1: 1 = VIN + < VIN-0 = VIN + > VIN -C10UT: Comparator 1 Output Status bit⁽²⁾ bit 0 When CPOL = 0: 1 = VIN + > VIN-0 = VIN + < VIN-When CPOL = 1: 1 = VIN + < VIN-0 = VIN + > VIN -
- **Note 1:** Reflects the value of the of the CEVT bit in the respective Op Amp/Comparator Control register, CMxCON<9>.
 - 2: Reflects the value of the COUT bit in the respective Op Amp/Comparator Control register, CMxCON<8>.

DC CHARACTERISTICS		Standard Operating Conditions: 3.0V to 3.6V(unless otherwise stated)Operating temperature $-40^{\circ}C \le TA \le +85^{\circ}C$ for Industrial $-40^{\circ}C \le TA \le +125^{\circ}C$ for Extended					
Param No.	Symbol	Characteristic	Min.	Тур.	Max.	Units	Conditions
	lı∟	Input Leakage Current ^(1,2)					
DI50		I/O Pins 5V Tolerant ⁽³⁾	-1	—	+1	μA	$Vss \le VPIN \le VDD$, Pin at high-impedance
DI51		I/O Pins Not 5V Tolerant ⁽³⁾	-1	_	+1	μA	$\label{eq:VSS} \begin{split} &Vss \leq V \text{PIN} \leq V \text{DD}, \\ &\text{Pin at high-impedance}, \\ &-40^\circ\text{C} \leq \text{TA} \leq +85^\circ\text{C} \end{split}$
DI51a		I/O Pins Not 5V Tolerant ⁽³⁾	-1	_	+1	μA	Analog pins shared with external reference pins, $-40^{\circ}C \le TA \le +85^{\circ}C$
DI51b		I/O Pins Not 5V Tolerant ⁽³⁾	-1	_	+1	μA	$\label{eq:VSS} \begin{array}{l} VSS \leq VPIN \leq VDD, \\ Pin \text{ at high-impedance}, \\ -40^\circC \leq TA \leq +125^\circC \end{array}$
DI51c		I/O Pins Not 5V Tolerant ⁽³⁾	-1	_	+1	μA	Analog pins shared with external reference pins, $-40^{\circ}C \le TA \le +125^{\circ}C$
DI55		MCLR	-5	_	+5	μA	$Vss \leq V \text{PIN} \leq V \text{DD}$
DI56		OSC1	-5	_	+5	μA	$\label{eq:VSS} \begin{array}{l} VSS \leq VPIN \leq VDD, \\ XT \text{ and } HS \text{ modes} \end{array}$

TABLE 30-11: DC CHARACTERISTICS: I/O PIN INPUT SPECIFICATIONS (CONTINUED)

Note 1: The leakage current on the MCLR pin is strongly dependent on the applied voltage level. The specified levels represent normal operating conditions. Higher leakage current can be measured at different input voltages.

- 2: Negative current is defined as current sourced by the pin.
- 3: See the "Pin Diagrams" section for the 5V tolerant I/O pins.
- 4: VIL source < (Vss 0.3). Characterized but not tested.
- **5:** Non-5V tolerant pins VIH source > (VDD + 0.3), 5V tolerant pins VIH source > 5.5V. Characterized but not tested.
- 6: Digital 5V tolerant pins cannot tolerate any "positive" input injection current from input sources > 5.5V.
- 7: Non-zero injection currents can affect the ADC results by approximately 4-6 counts.

8: Any number and/or combination of I/O pins not excluded under IICL or IICH conditions are permitted provided the mathematical "absolute instantaneous" sum of the input injection currents from all pins do not exceed the specified limit. Characterized but not tested.

FIGURE 30-17: SPI2 MASTER MODE (FULL-DUPLEX, CKE = 0, CKP = x, SMP = 1) TIMING CHARACTERISTICS



TABLE 30-36:SPI2 MASTER MODE (FULL-DUPLEX, CKE = 0, CKP = x, SMP = 1)TIMING REQUIREMENTS

AC CHARACTERISTICS		Standard Operating Conditions: 3.0V to 3.6V(unless otherwise stated)Operating temperature $-40^{\circ}C \le TA \le +85^{\circ}C$ for Industrial						
	i	<i>"</i>	$-40^{\circ}C \le TA \le +125^{\circ}C$ for Extended					
Param.	Symbol	Characteristic ⁽¹⁾	Min.	Typ. ⁽²⁾	Max.	Units	Conditions	
SP10	FscP	Maximum SCK2 Frequency	—	—	9	MHz	-40°C to +125°C (Note 3)	
SP20	TscF	SCK2 Output Fall Time	_	_		ns	See Parameter DO32 (Note 4)	
SP21	TscR	SCK2 Output Rise Time	—	_	_	ns	See Parameter DO31 (Note 4)	
SP30	TdoF	SDO2 Data Output Fall Time	—	—	_	ns	See Parameter DO32 (Note 4)	
SP31	TdoR	SDO2 Data Output Rise Time	—	_	_	ns	See Parameter DO31 (Note 4)	
SP35	TscH2doV, TscL2doV	SDO2 Data Output Valid after SCK2 Edge	—	6	20	ns		
SP36	TdoV2scH, TdoV2scL	SDO2 Data Output Setup to First SCK2 Edge	30	_		ns		
SP40	TdiV2scH, TdiV2scL	Setup Time of SDI2 Data Input to SCK2 Edge	30			ns		
SP41	TscH2diL, TscL2diL	Hold Time of SDI2 Data Input to SCK2 Edge	30			ns		

Note 1: These parameters are characterized, but are not tested in manufacturing.

2: Data in "Typical" column is at 3.3V, +25°C unless otherwise stated.

- **3:** The minimum clock period for SCK2 is 111 ns. The clock generated in Master mode must not violate this specification.
- 4: Assumes 50 pF load on all SPI2 pins.

NOTES: