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Details

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Product Status	Obsolete
Core Processor	PIC
Core Size	16-Bit
Speed	60 MIPs
Connectivity	I ² C, IrDA, LINbus, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, DMA, POR, PWM, WDT
Number of I/O	35
Program Memory Size	128KB (43K x 24)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	8K x 16
Voltage - Supply (Vcc/Vdd)	3V ~ 3.6V
Data Converters	A/D 9x10b/12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 125°C (TA)
Mounting Type	Surface Mount
Package / Case	44-VQFN Exposed Pad
Supplier Device Package	44-QFN (8x8)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/pic24ep128gp204t-e-ml

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FIGURE 4-9: DATA MEMORY MAP FOR dsPIC33EP128MC20X/50X AND dsPIC33EP128GP50X DEVICES

File Name	Addr	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	All
	0.400								Cas dafini	tion								Resets
	0400- 041E								See defini	tion when wi	IN = x							
C1BUFPNT1	0420		F3B	P<3:0>			F2BI	><3:0>			F1BP	o<3:0>			F0BP	<3:0>		0000
C1BUFPNT2	0422		F7B	P<3:0>			F6BI	><3:0>			F5BP	2 <3:0>			F4BP	<3:0>		0000
C1BUFPNT3	0424		F11B	3P<3:0>			F10B	P<3:0>			F9BP	2 <3:0>		F8BP<3:0>				0000
C1BUFPNT4	0426		F15E	3P<3:0>			F14B	P<3:0>			F13B	P<3:0>		F12BP<3:0>				0000
C1RXM0SID	0430				SID	:10:3>					SID<2:0>		_	MIDE	_	EID<	17:16>	xxxx
C1RXM0EID	0432				EID≪	:15:8>							EID<	:7:0>				xxxx
C1RXM1SID	0434				SID	:10:3>					SID<2:0>		—	MIDE	—	EID<	17:16>	xxxx
C1RXM1EID	0436				EID<	:15:8>							EID<	:7:0>				xxxx
C1RXM2SID	0438				SID<	:10:3>					SID<2:0>		—	MIDE	—	EID<	17:16>	xxxx
C1RXM2EID	043A				EID<	:15:8>							EID<	7:0>		-		xxxx
C1RXF0SID	0440				SID<	:10:3>					SID<2:0>		—	EXIDE	—	EID<	17:16>	xxxx
C1RXF0EID	0442				EID<	:15:8>							EID<	7:0>		-		xxxx
C1RXF1SID	0444				SID<	:10:3>					SID<2:0>		—	EXIDE	—	EID<	17:16>	xxxx
C1RXF1EID	0446				EID<	:15:8>							EID<	:7:0>		-		xxxx
C1RXF2SID	0448				SID<	:10:3>					SID<2:0>		—	EXIDE	_	EID<	17:16>	xxxx
C1RXF2EID	044A				EID<	:15:8>				EID			EID<	:7:0>	_	_		xxxx
C1RXF3SID	044C				SID<	:10:3>					SID<2:0>	GID<2:0> —			_	EID<	17:16>	xxxx
C1RXF3EID	044E				EID<	:15:8>							EID<	:7:0>	_	_		xxxx
C1RXF4SID	0450				SID<	:10:3>					SID<2:0>			EXIDE	_	EID<	17:16>	xxxx
C1RXF4EID	0452				EID<	:15:8>							EID<	:7:0>	_	_		xxxx
C1RXF5SID	0454				SID<	:10:3>					SID<2:0>			EXIDE	_	EID<	17:16>	xxxx
C1RXF5EID	0456				EID<	:15:8>							EID<	:7:0>	_	_		xxxx
C1RXF6SID	0458				SID<	:10:3>					SID<2:0>			EXIDE	_	EID<	17:16>	xxxx
C1RXF6EID	045A				EID<	:15:8>							EID<	:7:0>		-		xxxx
C1RXF7SID	045C				SID<	:10:3>					SID<2:0>			EXIDE	—	EID<	17:16>	xxxx
C1RXF7EID	045E				EID<	:15:8>							EID<	:7:0>	_	_		xxxx
C1RXF8SID	0460				SID<	:10:3>					SID<2:0>			EXIDE	_	EID<	17:16>	xxxx
C1RXF8EID	0462				EID<	:15:8>							EID<	:7:0>	_	_		xxxx
C1RXF9SID	0464				SID<	:10:3>					SID<2:0>			EXIDE	_	EID<	17:16>	xxxx
C1RXF9EID	0466				EID<	:15:8>							EID<	:7:0>		-		xxxx
C1RXF10SID	0468				SID<	:10:3>					SID<2:0>		—	EXIDE	—	EID<	17:16>	xxxx
C1RXF10EID	046A				EID	:15:8>							EID<	7:0>		_		xxxx
C1RXF11SID	046C				SID	:10:3>					SID<2:0>		—	EXIDE	_	EID<	17:16>	xxxx

TABLE 4-23: ECAN1 REGISTER MAP WHEN WIN (C1CTRL1<0>) = 1 FOR dsPIC33EPXXXMC/GP50X DEVICES ONLY

Legend: x = unknown value on Reset, — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

4.4.1 PAGED MEMORY SCHEME

The dsPIC33EPXXXGP50X, dsPIC33EPXXXMC20X/ 50X and PIC24EPXXXGP/MC20X architecture extends the available Data Space through a paging scheme, which allows the available Data Space to be accessed using MOV instructions in a linear fashion for pre-modified and post-modified Effective Addresses (EA). The upper half of the base Data Space address is used in conjunction with the Data Space Page registers, the 10-bit Read Page register (DSRPAG) or the 9-bit Write Page register (DSWPAG), to form an Extended Data Space (EDS) address or Program Space Visibility (PSV) address. The Data Space Page registers are located in the SFR space.

Construction of the EDS address is shown in Example 4-1. When DSRPAG<9> = 0 and the base address bit, EA<15> = 1, the DSRPAG<8:0> bits are concatenated onto EA<14:0> to form the 24-bit EDS read address. Similarly, when base address bit, EA<15> = 1, DSWPAG<8:0> are concatenated onto EA<14:0> to form the 24-bit EDS write address.





6.0 RESETS

- Note 1: This data sheet summarizes the features of the dsPIC33EPXXXGP50X, dsPIC33EPXXXMC20X/50X and PIC24EPXXXGP/MC20X families of devices. It is not intended to be a comprehensive reference source. To complement the information in this data sheet, refer to "Reset" (DS70602) in the "dsPIC33/PIC24 Family Reference Manual", which is available from the Microchip web site (www.microchip.com).
 - 2: Some registers and associated bits described in this section may not be available on all devices. Refer to Section 4.0 "Memory Organization" in this data sheet for device-specific register and bit information.

The Reset module combines all Reset sources and controls the device Master Reset Signal, SYSRST. The following is a list of device Reset sources:

- · POR: Power-on Reset
- · BOR: Brown-out Reset
- MCLR: Master Clear Pin Reset
- SWR: RESET Instruction
- WDTO: Watchdog Timer Time-out Reset
- CM: Configuration Mismatch Reset
- TRAPR: Trap Conflict Reset
- IOPUWR: Illegal Condition Device Reset
- Illegal Opcode Reset
- Uninitialized W Register Reset
- Security Reset

FIGURE 6-1: RESET SYSTEM BLOCK DIAGRAM

A simplified block diagram of the Reset module is shown in Figure 6-1.

Any active source of Reset will make the SYSRST signal active. On system Reset, some of the registers associated with the CPU and peripherals are forced to a known Reset state and some are unaffected.

Note: Refer to the specific peripheral section or Section 4.0 "Memory Organization" of this manual for register Reset states.

All types of device Reset set a corresponding status bit in the RCON register to indicate the type of Reset (see Register 6-1).

A POR clears all the bits, except for the POR and BOR bits (RCON<1:0>), that are set. The user application can set or clear any bit at any time during code execution. The RCON bits only serve as status bits. Setting a particular Reset status bit in software does not cause a device Reset to occur.

The RCON register also has other bits associated with the Watchdog Timer and device power-saving states. The function of these bits is discussed in other sections of this manual.

Note: The status bits in the RCON register should be cleared after they are read so that the next RCON register value after a device Reset is meaningful.

For all Resets, the default clock source is determined by the FNOSC<2:0> bits in the FOSCSEL Configuration register. The value of the FNOSC<2:0> bits is loaded into NOSC<2:0> (OSCCON<10:8>) on Reset, which in turn, initializes the system clock.



12.2 Timer1 Control Register

R/W-0	U-0	R/W-0	U-0	U-0	U-0	U-0	U-0
TON ⁽¹⁾	—	TSIDL	—	_	—	—	—
bit 15							bit 8
U-0	R/W-0	R/W-0	R/W-0	U-0	R/W-0	R/W-0	U-0
	TGATE	TCKPS1	TCKPS0	_	TSYNC ⁽¹⁾	TCS ⁽¹⁾	—
bit 7							bit 0
Legend:							
R = Readab	ole bit	W = Writable	bit	U = Unimpler	mented bit, read	as '0'	
-n = Value a	at POR	'1' = Bit is set		'0' = Bit is cle	ared	x = Bit is unkn	own
		(4)					
bit 15	TON: Timer1	On bit ⁽¹⁾					
	1 = Starts 16-	bit Limer1 bit Timer1					
bit 1/	Unimplement	ted: Pead as '	ı'				
bit 13		1 Stop in Idle N	lode hit				
DIC 15	1 = Discontinu	i stop in lae k	eration when a	device enters l	dle mode		
	0 = Continues	module opera	tion in Idle mo	ode			
bit 12-7	Unimplement	ted: Read as ')'				
bit 6	TGATE: Time	r1 Gated Time	Accumulation	Enable bit			
	When TCS =	<u>1:</u> prod					
	When TCS =	0. 0.					
	1 = Gated tim	<u>e</u> accumulatior	n is enabled				
	0 = Gated tim	e accumulatior	n is disabled				
bit 5-4	TCKPS<1:0>	: Timer1 Input	Clock Prescal	e Select bits			
	11 = 1:256						
	10 = 1:64 01 = 1:8						
	01 = 1.0 00 = 1.1						
bit 3	Unimplement	ted: Read as ')'				
bit 2	TSYNC: Time	er1 External Clo	ock Input Sync	chronization Se	elect bit ⁽¹⁾		
	When TCS =	1:					
	1 = Synchroni	izes external cl	ock input				
	0 = Does not	synchronize ex	ternal clock in	nput			
	This bit is jand	<u>ored</u> .					
bit 1	TCS: Timer1 (Clock Source S	Select bit ⁽¹⁾				
	1 = External c	lock is from pir	n, T1CK (on th	ne rising edge)			
	0 = Internal cl	ock (FP)		5 5-7			
bit 0	Unimplement	ted: Read as ')'				
Note 1: \	When Timer1 is en attempts by user so	abled in Exterr oftware to write	al Synchrono to the TMR1	us Counter mo register are ig	ode (TCS = 1, T nored.	SYNC = 1, TO	N = 1), any

REGISTER 12-1: T1CON: TIMER1 CONTROL REGISTER

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·							
R/W-1	R/W-1	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
PENH	PENL	POLH	POLL	PMOD1 ⁽¹⁾	PMOD0 ⁽¹⁾	OVRENH	OVRENL
bit 15							bit 8
R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
OVRDAT1	OVRDAT0	FLTDAT1	FLTDAT0	CLDAT1	CLDAT0	SWAP	OSYNC
bit 7							bit 0
Legend:							
R = Readable	bit	W = Writable	bit	U = Unimplei	mented bit, read	l as '0'	
-n = Value at F	POR	'1' = Bit is set		'0' = Bit is cle	eared	x = Bit is unkr	nown
bit 15	PENH: PWM	(H Output Pin (Ownership bit				
	1 = PWMx mc	dule controls I	PWMxH pin WMx⊟ pin				
hit 11							
DIL 14	1 = DM/Mx mc	a Output Pin C					
	1 = PWWX IIIC 0 = GPIO model	dule controls P	WMxL pin				
hit 13		H Output Pin I	Polarity bit				
	1 = PWMxH r	in is active-low	/				
	0 = PWMxH p	oin is active-hig	h				
bit 12	POLL: PWMx	L Output Pin F	olarity bit				
	1 = PWMxL p	in is active-low	,				
	0 = PWMxL p	in is active-hig	h				
bit 11-10	PMOD<1:0>:	PWMx # I/O P	in Mode bits ⁽¹)			
	11 = Reserve	d; do not use					
	10 = PWMx I/	O pin pair is in	the Push-Pul	I Output mode			
	01 = PWWx I/ 00 = PWMx I/	O pin pair is in O pin pair is in	the Complem	nt Output mod entary Output	mode		
hit 9	OVRENH: Ov	erride Enable i	for PWMxH P	in bit	mouo		
bit o	1 = OVRDAT	<1> controls or	itput on PWM	xH nin			
	0 = PWMx ge	nerator control	s PWMxH pin				
bit 8	OVRENL: Ov	erride Enable f	or PWMxL Pi	n bit			
	1 = OVRDAT	<0> controls ou	Itput on PWM	xL pin			
	0 = PWMx ge	nerator control	s PWMxL pin				
bit 7-6	OVRDAT<1:0	>: Data for PW	/MxH, PWMxl	L Pins if Overr	ide is Enabled b	its	
	If OVERENH	= 1, PWMxH is	s driven to the	state specifie	d by OVRDAT<	1>.	
	If OVERENL :	= 1, PWMxL is	driven to the	state specified	l by OVRDAT<0	>.	
bit 5-4	FLTDAT<1:0>	Data for PW	MxH and PWI	MxL Pins if FL	TMOD is Enable	ed bits	
	If Fault is activ	ve, PWMxH is	driven to the s	state specified	by FLTDAT<1>		
hit 2 0		VE, FVVIVIXL IS (UY FLIDAISUS.	hita	
UIL 3-2	LUAI <1:0>			IXL PILIS IT ULN			
	If current-limit	is active. PWN	/IxL is driven t	the state sp	ecified by CLDA	T<0>.	
Note 1: The	ese bits should i	not be changed	d after the PW	Mx module is	enabled (PTEN	= 1).	

REGISTER 16-13: IOCONx: PWMx I/O CONTROL REGISTER⁽²⁾

2: If the PWMLOCK Configuration bit (FOSCSEL<6>) is a '1', the IOCONx register can only be written after the unlock sequence has been executed.

R/C-0	R/C-0	R/C-0	R/C-0	R/C-0	R/C-0	R/C-0	R/C-0
RXOVF15	RXOVF14	RXOVF13	RXOVF12	RXOVF11	RXOVF10	RXOVF9	RXOVF8
bit 15							bit 8
R/C-0	R/C-0	R/C-0	R/C-0	R/C-0	R/C-0	R/C-0	R/C-0

REGISTER 21-24: CxRXOVF1: ECANx RECEIVE BUFFER OVERFLOW REGISTER 1

RXOVF7	RXOVF6	RXOVF5	RXOVF4	RXOVF3	RXOVF2	RXOVF1	RXOVF0
bit 7							bit 0
Legend:		C = Writable b	oit, but only '0'	can be writter	ו to clear the bit		

Legend:	C = Writable bit, but only '0' can be written to clear the bit					
R = Readable bit	W = Writable bit	U = Unimplemented bit, read	l as '0'			
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown			

bit 15-0 RXOVF<15:0>: Receive Buffer n Overflow bits

1 = Module attempted to write to a full buffer (set by module)

0 = No overflow condition (cleared by user software)

REGISTER 21-25: CxRXOVF2: ECANx RECEIVE BUFFER OVERFLOW REGISTER 2

| R/C-0 |
|---------|---------|---------|---------|---------|---------|---------|---------|
| RXOVF31 | RXOVF30 | RXOVF29 | RXOVF28 | RXOVF27 | RXOVF26 | RXOVF25 | RXOVF24 |
| bit 15 | | | | | | | bit 8 |

| R/C-0 |
|---------|---------|---------|---------|---------|---------|---------|---------|
| RXOVF23 | RXOVF22 | RXOVF21 | RXOVF20 | RXOVF19 | RXOVF18 | RXOVF17 | RXOVF16 |
| bit 7 | | | | | | | bit 0 |

Legend:	C = Writable bit, but only '0' can be written to clear the bit						
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'					
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown				

bit 15-0 RXOVF<31:16>: Receive Buffer n Overflow bits

1 = Module attempted to write to a full buffer (set by module)

0 = No overflow condition (cleared by user software)

BUFFER 21-7: ECAN™ MESSAGE BUFFER WORD 6

R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x
			By	te 7			
bit 15							bit 8
R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x
			By	te 6			
bit 7							bit 0
Legend:							
R = Readable bit W = Writable bit U = Unimplemented bit, read as '0'							
-n = Value at POR '1' = Bit is set '0' = Bit is cleared x = Bit is unknown						nown	

bit 15-8 Byte 7<15:8>: ECAN Message Byte 7 bits

bit 7-0 Byte 6<7:0>: ECAN Message Byte 6 bits

BUFFER 21-8: ECAN[™] MESSAGE BUFFER WORD 7

U-0	U-0	U-0	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x
	—	_	FILHIT4 ⁽¹⁾	FILHIT3 ⁽¹⁾	FILHIT2 ⁽¹⁾	FILHIT1 ⁽¹⁾	FILHITO ⁽¹⁾
bit 15							bit 8
U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
_	—	_	—	_	_	—	—
bit 7							bit 0
Leaend:							

Legena.			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read	as '0'
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15-13	Unimplemented: Read as '0'
bit 12-8	FILHIT<4:0>: Filter Hit Code bits ⁽¹⁾
	Encodes number of filter that resulted in writing this buffer.
bit 7-0	Unimplemented: Read as '0'

Note 1: Only written by module for receive buffers, unused for transmit buffers.

REGISTER 24-6:	PTGSDLIM: PTG STEP DELAY LIMIT REGISTER ^(1,2)

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
			PTGSD	LIM<15:8>			
bit 15							bit 8
R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
			PTGSE	DLIM<7:0>			
bit 7							bit 0
Legend:							
R = Readable	= Readable bit W = Writable bit U = Unimplemented		mented bit, rea	ad as '0'			
-n = Value at P	POR	R '1' = Bit is set '0' = Bit is cleared x = Bit		x = Bit is unkr	nown		

bit 15-0 **PTGSDLIM<15:0>:** PTG Step Delay Limit Register bits Holds a PTG Step delay value representing the number of additional PTG clocks between the start of a Step command and the completion of a Step command.

Note 1: A base Step delay of one PTG clock is added to any value written to the PTGSDLIM register (Step Delay = (PTGSDLIM) + 1).

2: This register is read-only when the PTG module is executing Step commands (PTGEN = 1 and PTGSTRT = 1).

REGISTER 24-7: PTGC0LIM: PTG COUNTER 0 LIMIT REGISTER⁽¹⁾

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
			PTGC0	LIM<15:8>			
bit 15							bit 8
R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
			PTGC)LIM<7:0>			
bit 7							bit 0
Legend:							
R = Readable bit W = Writable bit		pit	U = Unimpler	mented bit, rea	ad as '0'		
-n = Value at POR '1' = Bit is set			'0' = Bit is cle	ared	x = Bit is unkı	nown	

bit 15-0 **PTGC0LIM<15:0>:** PTG Counter 0 Limit Register bits May be used to specify the loop count for the PTGJMPC0 Step command or as a limit register for the General Purpose Counter 0.

Note 1: This register is read-only when the PTG module is executing Step commands (PTGEN = 1 and PTGSTRT = 1).

REGISTER 24-8: PTGC1LIM: PTG COUNTER 1 LIMIT REGISTER⁽¹⁾

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
			PTGC1L	IM<15:8>			
bit 15							bit 8
R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
			PTGC1L	_IM<7:0>			
bit 7							bit 0
Logond							

Legena.				
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'		
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown	

bit 15-0 **PTGC1LIM<15:0>:** PTG Counter 1 Limit Register bits May be used to specify the loop count for the PTGJMPC1 Step command or as a limit register for the General Purpose Counter 1.

REGISTER 24-9: PTGHOLD: PTG HOLD REGISTER⁽¹⁾

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	
	PTGHOLD<15:8>							
bit 15							bit 8	

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0		
	PTGHOLD<7:0>								
bit 7							bit 0		

Legend:				
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'		
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown	

bit 15-0 **PTGHOLD<15:0>:** PTG General Purpose Hold Register bits Holds user-supplied data to be copied to the PTGTxLIM, PTGCxLIM, PTGSDLIM or PTGL0 registers with the PTGCOPY command.

Note 1: This register is read-only when the PTG module is executing Step commands (PTGEN = 1 and PTGSTRT = 1).

Note 1: This register is read-only when the PTG module is executing Step commands (PTGEN = 1 and PTGSTRT = 1).

dsPIC33EPXXXGP50X, dsPIC33EPXXXMC20X/50X AND PIC24EPXXXGP/MC20X

REGISTER 24-12: PTGQPTR: PTG STEP QUEUE POINTER REGISTER⁽¹⁾

U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
—	—		—	_	—		—
bit 15							bit 8
U-0	U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
—	—	—	PTGQPTR<4:0>				
bit 7							bit 0

Legend:				
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'		
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown	

bit 15-5 Unimplemented: Read as '0'

bit 4-0 **PTGQPTR<4:0>:** PTG Step Queue Pointer Register bits This register points to the currently active Step command in the Step queue.

Note 1: This register is read-only when the PTG module is executing Step commands (PTGEN = 1 and PTGSTRT = 1).

REGISTER 24-13: PTGQUEX: PTG STEP QUEUE REGISTER x (x = 0-7)^(1,3)

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0			
STEP(2x + 1)<7:0> ⁽²⁾										
bit 15							bit 8			
R/M/-0	R/M_0	R/M_0	R///_0	R/W_0	R/W_0	R/M_0	R/W_0			

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0		
STEP(2x)<7:0> ⁽²⁾									
bit 7 bit 0									

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read	as '0'
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15-8	STEP(2x + 1)<7:0>: PTG Step Queue Pointer Register bits ⁽²⁾
	A queue location for storage of the STEP(2x + 1) command byte
bit 7-0	STEP(2x)<7:0>: PTG Step Queue Pointer Register bits ⁽²⁾
	A queue location for storage of the STEP(2x) command byte.

- **Note 1:** This register is read-only when the PTG module is executing Step commands (PTGEN = 1 and PTGSTRT = 1).
 - 2: Refer to Table 24-1 for the Step command encoding.

3: The Step registers maintain their values on any type of Reset.

					-					
R/W-0	R/W-0	R/W-0	U-0	U-0	R/W-0	R/W-0	R/W-0			
CON	COE ⁽²⁾	CPOL	_		OPMODE	CEVT	COUT			
bit 15						•	bit 8			
R/W-0	R/W-0	U-0	R/W-0	U-0	U-0	R/W-0	R/W-0			
EVPOL1	EVPOL0		CREF ⁽¹⁾	—	_	CCH1 ⁽¹⁾	CCH0 ⁽¹⁾			
bit 7 bit										
Legend:										
R = Readable	bit	W = Writable	bit		mented bit, read	as '0'				
-n = Value at I	POR	'1' = Bit is set		'0' = Bit is cle	eared	x = Bit is unkr	IOWN			
bit 1E		n/Comporator	Enabla bit							
DIL 15		ip/Comparator is e								
	1 = Op amp/comparator is enabled $0 = Op amp/comparator is disabled$									
bit 14	COE: Comparator Output Enable bit ⁽²⁾									
	1 = Compara	itor output is pr	esent on the C	xOUT pin						
	0 = Compara	itor output is int	ernal only							
bit 13	CPOL: Comp	parator Output	Polarity Select	bit						
	1 = Compara	tor output is inv	verted							
h: 40 44		itor output is no	o, inverted							
		ited: Read as	0 	- Maria Oalart						
DIT 10		p Amp/Compa	rator Operation	n Mode Select	DIT					
	1 = Circuit op 0 = Circuit op	perates as an o	p amp mparator							
bit 9	CEVT: Comp	arator Event bi	t							
	1 = Compara	ator event acco	ording to the E	VPOL<1:0> se	ettings occurred	; disables futur	e triggers and			
	interrupt	s until the bit is	cleared							
	0 = Compara	ator event did n	ot occur							
bit 8	COUT: Comp	parator Output I	oit							
	<u>When CPOL</u> $1 = V_{N+} > V_{1}$		ed polarity):							
	0 = VIN + < VI	IN-								
	When CPOL	= 1 (inverted p	olarity):							
	1 = VIN+ < VI	N-								
	0 = VIN + > VI	N-								
Note 1. Inn	uts that are sel	ected and not a	vailable will be	tied to Vss. S	See the " Pin Dia	arams" section	n for available			

REGISTER 25-2: CMxCON: COMPARATOR x CONTROL REGISTER (x = 1, 2 OR 3)

- Note 1: Inputs that are selected and not available will be tied to Vss. See the "Pin Diagrams" section for available inputs for each package.
 - 2: This output is not available when OPMODE (CMxCON<10>) = 1.

dsPIC33EPXXXGP50X, dsPIC33EPXXXMC20X/50X AND PIC24EPXXXGP/MC20X

U-0	R/W-0	U-0	U-0	U-0	R/W-0	U-0	U-0				
_	CVR2OE ⁽¹⁾	—	—	—	VREFSEL	—	—				
bit 15							bit 8				
R/W-0) R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0				
CVRE	N CVR1OE ⁽¹⁾	CVRR	CVRSS ⁽²⁾	CVR3	CVR2	CVR1	CVR0				
bit 7							bit 0				
Legend:											
R = Read	able bit	W = Writable	bit	U = Unimple	mented bit, read	i as '0'					
-n = Value	e at POR	'1' = Bit is set	t	'0' = Bit is cle	eared	x = Bit is unkr	Iown				
bit 15	Unimplemen	ted: Read as '	0'		(1)						
bit 14	CVR2OE: Co	mparator Volta	ige Reference	2 Output Ena	ble bit ⁽¹⁾						
1 = (AVDD - AVSS)/2 is connected to the CVREF20 pin 0 = (AVDD - AVSS)/2 is disconnected from the CVREF20 pin											
bit 13-11	Unimplemen	Unimplemented: Read as '0'									
bit 10	VREFSEL: C	VREFSEL: Comparator Voltage Reference Select bit									
	1 = CVREFIN :	= VREF+	-								
	0 = CVREFIN i	s generated by	y the resistor n	etwork							
bit 9-8	Unimplemen	ted: Read as '	0'								
bit 7	CVREN: Con	nparator Voltag	je Reference E	nable bit							
	1 = Compara	tor voltage refe	erence circuit is	s powered on	wn						
bit 6	CVR1OF: Co	mparator Volta	age Reference	1 Output Ena	ble bit(1)						
bit o	1 = Voltage le	evel is output o	n the CVRFF10								
	0 = Voltage le	evel is disconne	ected from the	n CVREF10 pi	'n						
bit 5	CVRR: Comp	arator Voltage	Reference Ra	inge Selectior	n bit						
	1 = CVRSRC/2	24 step-size									
	0 = CVRSRC/3	32 step-size									
bit 4	CVRSS: Com	parator Voltag	e Reference S	ource Selecti	on bit ⁽²⁾						
	1 = Compara 0 = Compara	tor voltage refe tor voltage refe	erence source,	CVRSRC = (V CVRSRC = A)	(REF+) – (AVSS) /DD – AVSS						
bit 3-0	CVR<3:0> Co	omparator Volt	age Reference	Value Select	ion $0 \leq CVR < 3$:	0> ≤ 15 bits					
	When CVRR = 1:										
	CVREFIN = (C	VR<3:0>/24) •	(CVRSRC)								
	When CVRR	= 0:									
	CVREFIN = (C	VRSRC/4) + (C	VR<3:0>/32) •	(CVRSRC)							
Note 1:	CVRxOE overrides	s the TRISx an	d the ANSELx	bit settinas.							

REGISTER 25-7: CVRCON: COMPARATOR VOLTAGE REFERENCE CONTROL REGISTER

- 2: In order to operate with CVRSS = 1, at least one of the comparator modules must be enabled.

dsPIC33EPXXXGP50X, dsPIC33EPXXXMC20X/50X AND PIC24EPXXXGP/MC20X

REGISTER 26-3: CRCXORH: CRC XOR POLYNOMIAL HIGH REGISTER

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0			
X<31:24>										
bit 15							bit 8			
R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0			
	X<23:16>									
bit 7							bit 0			
Legend:										
R = Readable bit W = Writable bit			U = Unimplemented bit, read as '0'							
-n = Value at POR '1' = Bit is set				'0' = Bit is cleared x = Bit is unknown						

bit 15-0 X<31:16>: XOR of Polynomial Term Xⁿ Enable bits

REGISTER 26-4: CRCXORL: CRC XOR POLYNOMIAL LOW REGISTER

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	
		Х<	15:8>				
						bit 8	
R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	U-0	
		X<7:1>				—	
						bit 0	
R = Readable bit W = Writable		bit	U = Unimplen	nented bit, rea	id as '0'		
-n = Value at POR		'1' = Bit is set		ared	x = Bit is unknown		
· · · · · · · · · · · · · · · · · · ·	R/W-0	R/W-0 R/W-0 t W = Writable 0R '1' = Bit is set	R/W-0 R/W-0 R/W-0 X<7:1> W = Writable bit 0R '1' = Bit is set	R/W-0 R/W-0 R/W-0 R/W-0 X<15:8> X<7:1> U U U U U U U U U U U U U U U U U U U U U U U U U U U U U U U U U U	R/W-0 R/W-0 R/W-0 R/W-0 X<15:8> X<7:1> U	R/W-0 R/W-0 R/W-0 R/W-0 R/W-0 X<15:8> R/W-0 R/W-0 R/W-0 X<7:1> t W = Writable bit U = Unimplemented bit, read as '0' VR '1' = Bit is set '0' = Bit is cleared x = Bit is unkr	

bit 15-1X<15:1>: XOR of Polynomial Term Xⁿ Enable bitsbit 0Unimplemented: Read as '0'

FIGURE 30-17: SPI2 MASTER MODE (FULL-DUPLEX, CKE = 0, CKP = x, SMP = 1) TIMING CHARACTERISTICS



TABLE 30-36:SPI2 MASTER MODE (FULL-DUPLEX, CKE = 0, CKP = x, SMP = 1)TIMING REQUIREMENTS

АС СНА	AC CHARACTERISTICS			Standard Operating Conditions: $3.0V$ to $3.6V$ (unless otherwise stated)Operating temperature $-40^{\circ}C \le TA \le +85^{\circ}C$ for Industrial $1000 \le TA \le +85^{\circ}C$ for Industrial						
	i	<i>"</i>	$-40^{\circ}C \le TA \le +125^{\circ}C$ for Extended							
Param.	Symbol	Characteristic ⁽¹⁾	Min.	Typ. ⁽²⁾	Max.	Units	Conditions			
SP10	FscP	Maximum SCK2 Frequency	—	—	9	MHz	-40°C to +125°C (Note 3)			
SP20	TscF	SCK2 Output Fall Time	_	_		ns	See Parameter DO32 (Note 4)			
SP21	TscR	SCK2 Output Rise Time	—	_	_	ns	See Parameter DO31 (Note 4)			
SP30	TdoF	SDO2 Data Output Fall Time	—	_	_	ns	See Parameter DO32 (Note 4)			
SP31	TdoR	SDO2 Data Output Rise Time	—	_	_	ns	See Parameter DO31 (Note 4)			
SP35	TscH2doV, TscL2doV	SDO2 Data Output Valid after SCK2 Edge	—	6	20	ns				
SP36	TdoV2scH, TdoV2scL	SDO2 Data Output Setup to First SCK2 Edge	30	_	_	ns				
SP40	TdiV2scH, TdiV2scL	Setup Time of SDI2 Data Input to SCK2 Edge	30			ns				
SP41	TscH2diL, TscL2diL	Hold Time of SDI2 Data Input to SCK2 Edge	30			ns				

Note 1: These parameters are characterized, but are not tested in manufacturing.

2: Data in "Typical" column is at 3.3V, +25°C unless otherwise stated.

- **3:** The minimum clock period for SCK2 is 111 ns. The clock generated in Master mode must not violate this specification.
- 4: Assumes 50 pF load on all SPI2 pins.





TABLE 30-44:SPI1 MASTER MODE (FULL-DUPLEX, CKE = 0, CKP = x, SMP = 1)TIMING REQUIREMENTS

AC CHA	RACTERIST	Standard Operating Conditions: 3.0V to 3.6V(unless otherwise stated)Operating temperature $-40^{\circ}C \le TA \le +85^{\circ}C$ for Industrial $-40^{\circ}C \le TA \le +125^{\circ}C$ for Extended					
Param.	Symbol	Characteristic ⁽¹⁾	Min.	Typ. ⁽²⁾	Max.	Units	Conditions
SP10	FscP	Maximum SCK1 Frequency	_	—	10	MHz	-40°C to +125°C (Note 3)
SP20	TscF	SCK1 Output Fall Time	_	—	—	ns	See Parameter DO32 (Note 4)
SP21	TscR	SCK1 Output Rise Time	_	—	—	ns	See Parameter DO31 (Note 4)
SP30	TdoF	SDO1 Data Output Fall Time	_	—	—	ns	See Parameter DO32 (Note 4)
SP31	TdoR	SDO1 Data Output Rise Time	_	—	—	ns	See Parameter DO31 (Note 4)
SP35	TscH2doV, TscL2doV	SDO1 Data Output Valid after SCK1 Edge	_	6	20	ns	
SP36	TdoV2scH, TdoV2scL	SDO1 Data Output Setup to First SCK1 Edge	30	_	_	ns	
SP40	TdiV2scH, TdiV2scL	Setup Time of SDI1 Data Input to SCK1 Edge	30	_	_	ns	
SP41	TscH2diL, TscL2diL	Hold Time of SDI1 Data Input to SCK1 Edge	30	_		ns	

Note 1: These parameters are characterized, but are not tested in manufacturing.

2: Data in "Typical" column is at 3.3V, +25°C unless otherwise stated.

- **3:** The minimum clock period for SCK1 is 100 ns. The clock generated in Master mode must not violate this specification.
- 4: Assumes 50 pF load on all SPI1 pins.

TABLE 30-48:SPI1 SLAVE MODE (FULL-DUPLEX, CKE = 0, CKP = 0, SMP = 0)TIMING REQUIREMENTS

АС СНА	AC CHARACTERISTICS			$\begin{array}{l} \mbox{Standard Operating Conditions: 3.0V to 3.6V} \\ \mbox{(unless otherwise stated)} \\ \mbox{Operating temperature} & -40^{\circ}C \leq TA \leq +85^{\circ}C \mbox{ for Industrial} \\ -40^{\circ}C \leq TA \leq +125^{\circ}C \mbox{ for Extended} \end{array}$				
Param.	Symbol	Characteristic ⁽¹⁾	Min.	Тур. ⁽²⁾	Max.	Units	Conditions	
SP70	FscP	Maximum SCK1 Input Frequency		_	11	MHz	(Note 3)	
SP72	TscF	SCK1 Input Fall Time	_		—	ns	See Parameter DO32 (Note 4)	
SP73	TscR	SCK1 Input Rise Time	—	—	—	ns	See Parameter DO31 (Note 4)	
SP30	TdoF	SDO1 Data Output Fall Time			_	ns	See Parameter DO32 (Note 4)	
SP31	TdoR	SDO1 Data Output Rise Time	—	_	_	ns	See Parameter DO31 (Note 4)	
SP35	TscH2doV, TscL2doV	SDO1 Data Output Valid after SCK1 Edge	—	6	20	ns		
SP36	TdoV2scH, TdoV2scL	SDO1 Data Output Setup to First SCK1 Edge	30	_	_	ns		
SP40	TdiV2scH, TdiV2scL	Setup Time of SDI1 Data Input to SCK1 Edge	30	_	_	ns		
SP41	TscH2diL, TscL2diL	Hold Time of SDI1 Data Input to SCK1 Edge	30	_	_	ns		
SP50	TssL2scH, TssL2scL	$\overline{SS1}$ ↓ to SCK1 ↑ or SCK1 ↓ Input	120	Ι	—	ns		
SP51	TssH2doZ	SS1 ↑ to SDO1 Output High-Impedance	10	—	50	ns	(Note 4)	
SP52	TscH2ssH, TscL2ssH	SS1 ↑ after SCK1 Edge	1.5 Tcy + 40	—	_	ns	(Note 4)	

Note 1: These parameters are characterized, but are not tested in manufacturing.

2: Data in "Typical" column is at 3.3V, +25°C unless otherwise stated.

3: The minimum clock period for SCK1 is 91 ns. Therefore, the SCK1 clock generated by the master must not violate this specification.

4: Assumes 50 pF load on all SPI1 pins.

AC CHARACTERISTICS			Standard Operating Conditions: 3.0V to 3.6V (unless otherwise stated) ⁽¹⁾ Operating temperature $-40^{\circ}C \le TA \le +85^{\circ}C$ for Industrial $-40^{\circ}C \le TA \le +125^{\circ}C$ for Extended					
Param No.	Symbol	Characteristic	Min.	Тур.	Max.	Units	Conditions	
		ADC A	ccuracy (10-Bit N	lode)			
AD20b	Nr	Resolution	10) Data B	its	bits		
AD21b	INL	Integral Nonlinearity	-0.625		0.625	LSb	-40°C ≤ TA ≤ +85°C (Note 2)	
			-1.5		1.5	LSb	+85°C < TA ≤ +125°C (Note 2)	
AD22b	DNL	Differential Nonlinearity	-0.25	_	0.25	LSb	-40°C ≤ TA ≤ +85°C (Note 2)	
			-0.25	_	0.25	LSb	$+85^{\circ}C < TA \le +125^{\circ}C$ (Note 2)	
AD23b	Gerr	Gain Error	-2.5		2.5	LSb	-40°C \leq TA \leq +85°C (Note 2)	
			-2.5		2.5	LSb	+85°C < TA \leq +125°C (Note 2)	
AD24b	EOFF	Offset Error	-1.25		1.25	LSb	-40°C \leq TA \leq +85°C (Note 2)	
			-1.25		1.25	LSb	+85°C < TA \leq +125°C (Note 2)	
AD25b	—	Monotonicity	_	_	_		Guaranteed	
		Dynamic P	erforman	ce (10-E	Bit Mode)			
AD30b	THD	Total Harmonic Distortion ⁽³⁾	—	64	—	dB		
AD31b	SINAD	Signal to Noise and Distortion ⁽³⁾	-	57	_	dB		
AD32b	SFDR	Spurious Free Dynamic Range ⁽³⁾	—	72	—	dB		
AD33b	Fnyq	Input Signal Bandwidth ⁽³⁾	—	550	—	kHz		
AD34b	ENOB	Effective Number of Bits ⁽³⁾	—	9.4	_	bits		

TABLE 30-59: ADC MODULE SPECIFICATIONS (10-BIT MODE)

Note 1: Device is functional at VBORMIN < VDD < VDDMIN, but will have degraded performance. Device functionality is tested, but not characterized. Analog modules (ADC, op amp/comparator and comparator voltage reference) may have degraded performance. Refer to Parameter BO10 in Table 30-13 for the minimum and maximum BOR values.

2: For all accuracy specifications, VINL = AVSS = VREFL = 0V and AVDD = VREFH = 3.6V.

3: Parameters are characterized but not tested in manufacturing.



1:128

70

Section Name	Update Description
Section 16.0 "High-Speed PWM Module (dsPIC33EPXXXMC20X/50X and PIC24EPXXXMC20X Devices Only)"	Updated the High-Speed PWM Module Register Interconnection Diagram (see Figure 16-2). Added the TRGCONx and TRIGx registers (see Register 16-12 and Register 16-14, respectively).
Section 21.0 "Enhanced CAN (ECAN™) Module (dsPIC33EPXXXGP/MC50X Devices Only)"	Updated the CANCKS bit value definitions in CiCTRL1: ECAN Control Register 1 (see Register 21-1).
Section 22.0 "Charge Time Measurement Unit (CTMU)"	Updated the IRNG<1:0> bit value definitions and added Note 2 in the CTMU Current Control Register (see Register 22-3).
Section 25.0 "Op amp/ Comparator Module"	Updated the Op amp/Comparator I/O Operating Modes Diagram (see Figure 25-1). Updated the User-programmable Blanking Function Block Diagram (see Figure 25-3). Updated the Digital Filter Interconnect Block Diagram (see Figure 25-4). Added Section 25.1 "Op amp Application Considerations ". Added Note 2 to the Comparator Control Register (see Register 25-2). Updated the bit definitions in the Comparator Mask Gating Control Register (see Register 25-5).
Section 27.0 "Special Features"	Updated the FICD Configuration Register, updated Note 1, and added Note 3 in the Configuration Byte Register Map (see Table 27-1). Added Section 27.2 " User ID Words ".
Section 30.0 "Electrical Characteristics"	 Updated the following Absolute Maximum Ratings: Maximum current out of Vss pin Maximum current into VDD pin Added Note 1 to the Operating MIPS vs. Voltage (see Table 30-1).
	Updated all Idle Current (IIDLE) Typical and Maximum DC Characteristics values (see Table 30-7).
	Updated all Doze Current (IDOZE) Typical and Maximum DC Characteristics values (see Table 30-9).
	Added Note 2, removed Parameter CM24, updated the Typical values Parameters CM10, CM20, CM21, CM32, CM41, CM44, and CM45, and updated the Minimum values for CM40 and CM41, and the Maximum value for CM40 in the AC/DC Characteristics: Op amp/Comparator (see Table 30-14).
	Updated Note 2 and the Typical value for Parameter VR310 in the Op amp/ Comparator Reference Voltage Settling Time Specifications (see Table 30-15).
	Added Note 1, removed Parameter VRD312, and added Parameter VRD314 to the Op amp/Comparator Voltage Reference DC Specifications (see Table 30-16).
	Updated the Minimum, Typical, and Maximum values for Internal LPRC Accuracy (see Table 30-22).
	Updated the Minimum, Typical, and Maximum values for Parameter SY37 in the Reset, Watchdog Timer, Oscillator Start-up Timer, Power-up Timer Timing Requirements (see Table 30-24).
	The Maximum Data Rate values were updated for the SPI2 Maximum Data/Clock Rate Summary (see Table 30-35)

TABLE A-2: MAJOR SECTION UPDATES (CONTINUED)