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"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "<u>Embedded -</u> <u>Microcontrollers</u>"

Details

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Product Status	Obsolete
Core Processor	PIC
Core Size	16-Bit
Speed	60 MIPs
Connectivity	I ² C, IrDA, LINbus, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, DMA, POR, PWM, WDT
Number of I/O	53
Program Memory Size	128KB (43K x 24)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	8K x 16
Voltage - Supply (Vcc/Vdd)	3V ~ 3.6V
Data Converters	A/D 16x10b/12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 150°C (TA)
Mounting Type	Surface Mount
Package / Case	64-VFQFN Exposed Pad
Supplier Device Package	64-VQFN (9x9)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/pic24ep128gp206-h-mr

Email: info@E-XFL.COM

Address: Room A, 16/F, Full Win Commercial Centre, 573 Nathan Road, Mongkok, Hong Kong



2.2.1 TANK CAPACITORS

On boards with power traces running longer than six inches in length, it is suggested to use a tank capacitor for integrated circuits including DSCs to supply a local power source. The value of the tank capacitor should be determined based on the trace resistance that connects the power supply source to the device and the maximum current drawn by the device in the application. In other words, select the tank capacitor so that it meets the acceptable voltage sag at the device. Typical values range from 4.7 μ F to 47 μ F.

2.3 CPU Logic Filter Capacitor Connection (VCAP)

A low-ESR (< 1 Ohm) capacitor is required on the VCAP pin, which is used to stabilize the voltage regulator output voltage. The VCAP pin must not be connected to VDD and must have a capacitor greater than 4.7 μ F (10 μ F is recommended), 16V connected to ground. The type can be ceramic or tantalum. See **Section 30.0** "**Electrical Characteristics**" for additional information.

The placement of this capacitor should be close to the VCAP pin. It is recommended that the trace length not exceeds one-quarter inch (6 mm). See **Section 27.3 "On-Chip Voltage Regulator"** for details.

2.4 Master Clear (MCLR) Pin

The MCLR pin provides two specific device functions:

- Device Reset
- Device Programming and Debugging.

During device programming and debugging, the resistance and capacitance that can be added to the pin must be considered. Device programmers and debuggers drive the MCLR pin. Consequently, specific voltage levels (VIH and VIL) and fast signal transitions must not be adversely affected. Therefore, specific values of R and C will need to be adjusted based on the application and PCB requirements.

For example, as shown in Figure 2-2, it is recommended that the capacitor, C, be isolated from the $\overline{\text{MCLR}}$ pin during programming and debugging operations.

Place the components as shown in Figure 2-2 within one-quarter inch (6 mm) from the MCLR pin.





3.6 CPU Resources

Many useful resources are provided on the main product page of the Microchip web site for the devices listed in this data sheet. This product page, which can be accessed using this link, contains the latest updates and additional information.

Note:	In the event you are not able to access the
	product page using the link above, enter
	this URL in your browser:
	http://www.microchip.com/wwwproducts/
	Devices.aspx?dDocName=en555464

3.6.1 KEY RESOURCES

- "CPU" (DS70359) in the "dsPIC33/PIC24 Family Reference Manual"
- Code Samples
- Application Notes
- Software Libraries
- Webinars
- All related "dsPIC33/PIC24 Family Reference Manual" Sections
- Development Tools

3.8 Arithmetic Logic Unit (ALU)

The dsPIC33EPXXXGP50X, dsPIC33EPXXXMC20X/ 50X and PIC24EPXXXGP/MC20X ALU is 16 bits wide, and is capable of addition, subtraction, bit shifts and logic operations. Unless otherwise mentioned, arithmetic operations are two's complement in nature. Depending on the operation, the ALU can affect the values of the Carry (C), Zero (Z), Negative (N), Overflow (OV) and Digit Carry (DC) Status bits in the <u>SR register. The C and DC</u> Status bits operate as Borrow and Digit Borrow bits, respectively, for subtraction operations.

The ALU can perform 8-bit or 16-bit operations, depending on the mode of the instruction that is used. Data for the ALU operation can come from the W register array or data memory, depending on the addressing mode of the instruction. Likewise, output data from the ALU can be written to the W register array or a data memory location.

Refer to the *"16-bit MCU and DSC Programmer's Reference Manual"* (DS70157) for information on the SR bits affected by each instruction.

The core CPU incorporates hardware support for both multiplication and division. This includes a dedicated hardware multiplier and support hardware for 16-bit divisor division.

3.8.1 MULTIPLIER

Using the high-speed 17-bit x 17-bit multiplier, the ALU supports unsigned, signed, or mixed-sign operation in several MCU multiplication modes:

- 16-bit x 16-bit signed
- 16-bit x 16-bit unsigned
- 16-bit signed x 5-bit (literal) unsigned
- 16-bit signed x 16-bit unsigned
- 16-bit unsigned x 5-bit (literal) unsigned
- 16-bit unsigned x 16-bit signed
- 8-bit unsigned x 8-bit unsigned

3.8.2 DIVIDER

The divide block supports 32-bit/16-bit and 16-bit/16-bit signed and unsigned integer divide operations with the following data sizes:

- 32-bit signed/16-bit signed divide
- 32-bit unsigned/16-bit unsigned divide
- 16-bit signed/16-bit signed divide
- 16-bit unsigned/16-bit unsigned divide

The quotient for all divide instructions ends up in W0 and the remainder in W1. The 16-bit signed and unsigned DIV instructions can specify any W register for both the 16-bit divisor (Wn) and any W register (aligned) pair (W(m + 1):Wm) for the 32-bit dividend. The divide algorithm takes one cycle per bit of divisor, so both 32-bit/16-bit and 16-bit/16-bit instructions take the same number of cycles to execute.

3.9 DSP Engine (dsPIC33EPXXXMC20X/50X and dsPIC33EPXXXGP50X Devices Only)

The DSP engine consists of a high-speed 17-bit x 17-bit multiplier, a 40-bit barrel shifter and a 40-bit adder/subtracter (with two target accumulators, round and saturation logic).

The DSP engine can also perform inherent accumulatorto-accumulator operations that require no additional data. These instructions are ADD, SUB and NEG.

The DSP engine has options selected through bits in the CPU Core Control register (CORCON), as listed below:

- Fractional or integer DSP multiply (IF)
- · Signed, unsigned or mixed-sign DSP multiply (US)
- · Conventional or convergent rounding (RND)
- · Automatic saturation on/off for ACCA (SATA)
- Automatic saturation on/off for ACCB (SATB)
- Automatic saturation on/off for writes to data memory (SATDW)
- Accumulator Saturation mode selection (ACCSAT)

	SOMMAN	
Instruction	Algebraic Operation	ACC Write Back
CLR	A = 0	Yes
ED	$A = (x - y)^2$	No
EDAC	$A = A + (x - y)^2$	No
MAC	$A = A + (x \bullet y)$	Yes
MAC	$A = A + x^2$	No
MOVSAC	No change in A	Yes
MPY	$A = x \bullet y$	No
MPY	$A = x^2$	No
MPY.N	$A = -x \bullet y$	No
MSC	$A = A - x \bullet y$	Yes

TABLE 3-2: DSP INSTRUCTIONS SUMMARY



FIGURE 4-7: DATA MEMORY MAP FOR dsPIC33EP32MC20X/50X AND dsPIC33EP32GP50X DEVICES

TABLE 4-19: SPI1 AND SPI2 REGISTER MAP

SFR Name	Addr.	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	All Resets
SPI1STAT	0240	SPIEN	—	SPISIDL	—	—	:	SPIBEC<2:0)>	SRMPT	SPIROV	SRXMPT		SISEL<2:0>		SPITBF	SPIRBF	0000
SPI1CON1	0242	_	_	_	DISSCK	DISSDO	MODE16	SMP	CKE	SSEN	CKP	MSTEN		SPRE<2:0>		PPRE	<1:0>	0000
SPI1CON2	0244	FRMEN	SPIFSD	FRMPOL	_	_	_	_	_	_	_	—	_	_	_	FRMDLY	SPIBEN	0000
SPI1BUF	0248							SPI1 Tra	ansmit and F	Receive Buf	fer Registe	r						0000
SPI2STAT	0260	SPIEN	—	SPISIDL	—	—	:	SPIBEC<2:0)>	SRMPT	SPIROV	SRXMPT		SISEL<2:0>		SPITBF	SPIRBF	0000
SPI2CON1	0262	_	—		DISSCK	DISSDO	MODE16	SMP	CKE	SSEN	CKP	MSTEN		SPRE<2:0>		PPRE	<1:0>	0000
SPI2CON2	0264	FRMEN	SPIFSD	FRMPOL	_	_	_	_	_	_	_	—	_	_	_	FRMDLY	SPIBEN	0000
SPI2BUF	0268	3 SPI2 Transmit and Receive Buffer Register 0											0000					

Legend: — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

File Name	Addr	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	All
	0.400								Cas dafini	tion								Resets
	0400- 041E								See defini	tion when wi	IN = x							
C1BUFPNT1	0420		F3B	P<3:0>			F2BI	><3:0>			F1BP	o<3:0>			F0BP	<3:0>		0000
C1BUFPNT2	0422		F7B	P<3:0>			F6BI	><3:0>			F5BP	2 <3:0>			F4BP<3:0>			
C1BUFPNT3	0424		F11B	3P<3:0>			F10B	P<3:0>		F9BP<3:0>				F8BP	<3:0>		0000	
C1BUFPNT4	0426		F15E	3P<3:0>			F14B	P<3:0>			F13B	P<3:0>			F12B	F12BP<3:0>		
C1RXM0SID	0430				SID	:10:3>					SID<2:0>		_	MIDE	_	EID<	17:16>	xxxx
C1RXM0EID	0432				EID≪	:15:8>							EID<	:7:0>				xxxx
C1RXM1SID	0434				SID	:10:3>					SID<2:0>		—	MIDE	—	EID<	17:16>	xxxx
C1RXM1EID	0436				EID<	:15:8>							EID<	:7:0>				xxxx
C1RXM2SID	0438				SID<	:10:3>					SID<2:0>		—	MIDE	—	EID<	17:16>	xxxx
C1RXM2EID	043A		EID<15:8>					EID<7:0>							xxxx			
C1RXF0SID	0440				SID<	:10:3>					SID<2:0>		—	EXIDE	—	EID<	17:16>	xxxx
C1RXF0EID	0442		EID<15:8>					EID<7:0>						xxxx				
C1RXF1SID	0444		SID<10:3>						SID<2:0>		—	EXIDE	—	EID<	17:16>	xxxx		
C1RXF1EID	0446		EID<15:8>						EID<	:7:0>		-		xxxx				
C1RXF2SID	0448		SID<10:3>				SID<2:0>		—	EXIDE	_	EID<	17:16>	xxxx				
C1RXF2EID	044A				EID<	:15:8>							EID<	:7:0>	_	_		xxxx
C1RXF3SID	044C				SID<	:10:3>					SID<2:0>			EXIDE	_	EID<	17:16>	xxxx
C1RXF3EID	044E				EID<	:15:8>				EID<7:0>						xxxx		
C1RXF4SID	0450				SID<	:10:3>				SID<2:0> —			EXIDE — EID<17:16>				xxxx	
C1RXF4EID	0452				EID<	:15:8>				EID<7:0>					_		xxxx	
C1RXF5SID	0454				SID<	:10:3>					SID<2:0>			EXIDE	_	EID<	17:16>	xxxx
C1RXF5EID	0456				EID<	:15:8>							EID<	:7:0>	_	_		xxxx
C1RXF6SID	0458				SID<	:10:3>					SID<2:0>			EXIDE	_	EID<	17:16>	xxxx
C1RXF6EID	045A				EID<	:15:8>							EID<	:7:0>		-		xxxx
C1RXF7SID	045C				SID<	:10:3>				_	SID<2:0>			EXIDE	—	EID<	17:16>	xxxx
C1RXF7EID	045E				EID<	:15:8>							EID<	:7:0>	_	_		xxxx
C1RXF8SID	0460				SID<	:10:3>					SID<2:0>			EXIDE	_	EID<	17:16>	xxxx
C1RXF8EID	0462				EID<	:15:8>							EID<	:7:0>	_	_		xxxx
C1RXF9SID	0464				SID<	:10:3>					SID<2:0>			EXIDE — EID<17:16>			xxxx	
C1RXF9EID	0466				EID<	:15:8>							EID<	:7:0>		-		xxxx
C1RXF10SID	0468				SID<	:10:3>					SID<2:0>		—	EXIDE	—	EID<	17:16>	xxxx
C1RXF10EID	046A				EID	:15:8>							EID<	7:0>		_		xxxx
C1RXF11SID	046C				SID	:10:3>					SID<2:0>		—	EXIDE	_	EID<	17:16>	xxxx

TABLE 4-23: ECAN1 REGISTER MAP WHEN WIN (C1CTRL1<0>) = 1 FOR dsPIC33EPXXXMC/GP50X DEVICES ONLY

Legend: x = unknown value on Reset, — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

dsPIC33EPXXXGP50X, dsPIC33EPXXXMC20X/50X AND PIC24EPXXXGP/MC20X

U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0				
—	—	—		—	—	—					
bit 15							bit 8				
U-0	U-0	U-0	U-0	R-0	R-0	R-0	R-0				
		<u> </u>		RQCOL3	RQCOL2	RQCOL1	RQCOL0				
bit 7							bit 0				
Legend:											
R = Readable	bit	W = Writable	bit	U = Unimplemented bit, read as '0'							
-n = Value at I	-n = Value at POR '1' = Bit is set				ared	x = Bit is unkr	iown				
bit 15-4	Unimplemen	ted: Read as '	י)								
bit 3	RQCOL3: DM	IA Channel 3 T	ransfer Requ	est Collision Fl	lag bit						
	1 = User forc	e and interrupt	-based reques	st collision is d	etected						
	0 = No reque	est collision is d	etected								
bit 2	RQCOL2: DM	IA Channel 2 T	ransfer Requ	est Collision Fl	lag bit						
	1 = User forc	e and interrupt	-based reques	st collision is d	etected						
	0 = No reque	est collision is d	etected								
bit 1	RQCOL1: DM	1A Channel 1 T	ransfer Reque	est Collision Fl	lag bit						
	1 = User forc 0 = No reque	e and interrupt st collision is d	-based reques etected	st collision is d	etected						
bit 0	RQCOL0: DM	1A Channel 0 T	ransfer Requ	est Collision Fl	lag bit						
	1 = User forc	e and interrupt	-based reques	st collision is d	etected						

REGISTER 8-12: DMARQC: DMA REQUEST COLLISION STATUS REGISTER

0 = No request collision is detected

REGISTER 9-2: CLKDIV: CLOCK DIVISOR REGISTER (CONTINUED)

- **Note 1:** The DOZE<2:0> bits can only be written to when the DOZEN bit is clear. If DOZEN = 1, any writes to DOZE<2:0> are ignored.
 - $\label{eq:constraint} \textbf{2:} \quad \text{This bit is cleared when the ROI bit is set and an interrupt occurs.}$
 - **3:** The DOZEN bit cannot be set if DOZE<2:0> = 000. If DOZE<2:0> = 000, any attempt by user software to set the DOZEN bit is ignored.

REGISTER 11-15: RPINR37: PERIPHERAL PIN SELECT INPUT REGISTER 37 (dsPIC33EPXXXMC20X/50X AND PIC24EPXXXMC20X DEVICES ONLY)

	5444.0	D 44/ 0	D 444 0		D 44/ 0	D 444 0			
U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0		
—				SYNCI1R<6:0)>				
bit 15							bit 8		
U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0		
—	—	—		—	—	—	_		
bit 7				-	•		bit 0		
Legend:									
R = Readabl	le bit	W = Writable b	oit	U = Unimplemented bit, read as '0'					
-n = Value at POR		'1' = Bit is set		'0' = Bit is cle	eared	x = Bit is unkn	iown		
bit 15	Unimplemer	nted: Read as '0)'						
bit 14-8	SYNCI1R<6: (see Table 11	• 0>: Assign PWI I-2 for input pin :	VI Synchroniz selection nur	zation Input 1 to nbers)	o the Correspon	ding RPn Pin b	its		
	1111001 = 	nput tied to RPI	121						
	•								
	•								
	0000001 = I	nout tied to CME	21						
	0000000 = 1	nput tied to Vss							
bit 7-0	Unimplemer	nted: Read as '0)'						

REGISTER 15-2: OCxCON2: OUTPUT COMPARE x CONTROL REGISTER 2 (CONTINUED)

bit 4-0	SYNCSE	-<4:0>: Trigger/Synchronization Source Selection bits
	11111 =	OCxRS compare event is used for synchronization
	11110 =	INT2 pin synchronizes or triggers OCx
	11101 =	INT1 pin synchronizes or triggers OCx
	11100 =	CTMU module synchronizes or triggers OCx
	11011 =	ADC1 module synchronizes or triggers OCx
	11010 =	CMP3 module synchronizes or triggers OCx
	11001 =	CMP2 module synchronizes or triggers OCx
	11000 =	CMP1 module synchronizes or triggers OCx
	10111 =	Reserved
	10110 =	Reserved
	10101 =	Reserved
	10100 =	Reserved
	10011 =	IC4 input capture event synchronizes or triggers OCx
	10010 =	IC3 input capture event synchronizes or triggers OCx
	10001 =	IC2 input capture event synchronizes or triggers OCx
	10000 =	IC1 input capture event synchronizes or triggers OCx
	01111 =	Timer5 synchronizes or triggers OCx
	01110 =	Timer4 synchronizes or triggers OCx
	01101 =	Timer3 synchronizes or triggers OCx
	01100 =	Timer2 synchronizes or triggers OCx (default)
	01011 =	Timer1 synchronizes or triggers OCx
	01010 =	PTGOx synchronizes or triggers OCx ⁽³⁾
	01001 =	Reserved
	01000 =	Reserved
	00111 =	Reserved
	00110 =	Reserved
	00101 =	Reserved
	00100 =	OC4 module synchronizes or triggers $OCx^{(1,2)}$
	00011 =	OC3 module synchronizes or triggers $OCx^{(1,2)}$
	00010 =	OC2 module synchronizes or triggers $OCx^{(1,2)}$
	00001 =	OC1 module synchronizes or triggers OCx ^(1,2)
	00000 =	No Sync or Trigger source for OCx

- **Note 1:** Do not use the OCx module as its own Synchronization or Trigger source.
 - 2: When the OCy module is turned OFF, it sends a trigger out signal. If the OCx module uses the OCy module as a Trigger source, the OCy module must be unselected as a Trigger source prior to disabling it.
 - Each Output Compare x module (OCx) has one PTG Trigger/Synchronization source. See Section 24.0 "Peripheral Trigger Generator (PTG) Module" for more information. PTGO0 = OC1

PTGO0 = OC1 PTGO1 = OC2 PTGO2 = OC3PTGO3 = OC4

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
QCAPEN	FLTREN	QFDIV2	QFDIV1	QFDIV0	OUTFNC1	OUTFNC0	SWPAB
bit 15					• •		bit 8
R/W-0	R/W-0	R/W-0	R/W-0	R-x	R-x	R-x	R-x
HOMPOL	IDXPOL	QEBPOL	QEAPOL	HOME	INDEX	QEB	QEA
bit 7							bit 0
Legend:	a hit	\// - \//ritabla	h it	II – Unimploy	monted bit read	4 a.a. (0)	
n - Value at		vv = vvii(able	DIL	$0^{\circ} = 0$	nented bit, read	v – Ritic unkn	
		1 - Dit 13 36t			areu		
bit 15	OCAPEN: OF	-I Position Cou	nter Input Cap	ture Enable bit			
	1 = Index ma	tch event trigge	ers a position c	apture event			
	0 = Index ma	tch event does	not trigger a p	osition capture	event		
bit 14	FLTREN: QE	Ax/QEBx/INDX	x/HOMEx Digi	ital Filter Enabl	e bit		
	1 = Input pin	digital filter is e digital filter is d	nabled isabled (bypas	eed)			
hit 13_11			NDXv/HOMEv	Digital Input Fi	ilter Clock Divid	a Salact hits	
511 15-11	111 = 1:128 (clock divide		Digital Input I			
	110 = 1:64 cl	ock divide					
	101 = 1:32 cl	ock divide					
	100 = 1.16 cm 011 = 1:8 clo	ck divide					
	010 = 1:4 clo	ck divide					
	001 = 1:2 clo	ck divide ck divide					
hit 10-9			Output Functi	ion Mode Sele	rt hits		
bit 10 5	11 = The CTN	VCMPx pin ace	s high when C	$EI1LEC \ge POS$	$S1CNT \ge QEI10$	GEC	
	10 = The CTM	NCMPx pin goe	s high when P	$OS1CNT \leq QE$	EIILEC		
	01 = The CT	NCMPx pin goe	s high when P	$OS1CNT \ge QE$	EI1GEC		
hit 8	SWPAB: Swa	s uisabled an OEA and OE	B Inputs hit				
bit 0	1 = QEAx and	d QEBx are swa	apped prior to	quadrature de	coder logic		
	0 = QEAx and	d QEBx are not	swapped	1			
bit 7	HOMPOL: HO	OMEx Input Po	larity Select bit	t			
	1 = Input is in	iverted					
hit 6		ot inverted Vy Input Dolori	ty Soloot bit				
DILO	1 = Input is in	verted	ly Select bit				
	0 = Input is no	ot inverted					
bit 5	QEBPOL: QE	EBx Input Polar	ity Select bit				
	1 = Input is ir	nverted					
L:1 4		ot inverted	:				
DIT 4		EAX Input Polar	ity Select bit				
	1 = 10000000000000000000000000000000000	not inverted					
bit 3	HOME: Statu	s of HOMEx In	out Pin After P	olarity Control			
	1 = Pin is at I	logic '1'		-			
	0 = Pin is at	logic '0'					

REGISTER 17-2: QEI1IOC: QEI1 I/O CONTROL REGISTER

dsPIC33EPXXXGP50X, dsPIC33EPXXXMC20X/50X AND PIC24EPXXXGP/MC20X

R/W-0	U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0			
ADRC	—	—	SAMC4 ⁽¹⁾	SAMC3 ⁽¹⁾	SAMC2 ⁽¹⁾	SAMC1 ⁽¹⁾	SAMC0 ⁽¹⁾			
bit 15							bit 8			
R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0			
ADCS7(2	²⁾ ADCS6 ⁽²⁾	ADCS5 ⁽²⁾	ADCS4 ⁽²⁾	ADCS3 ⁽²⁾	ADCS2 ⁽²⁾	ADCS1 ⁽²⁾	ADCS0 ⁽²⁾			
bit 7							bit 0			
Legend:										
R = Reada		vv = vvritable t	DIT		nented bit, read					
-n = value	at POR	"1" = Bit is set		$0^{\circ} = Bit is cle$	ared	x = Bit is unkr	nown			
bit 15	15 ADRC: ADC1 Conversion Clock Source bit 1 = ADC internal RC clock 0 = Clock derived from system clock									
bit 14-13	Unimplement	ted: Read as '0	3							
bit 12-8	SAMC<4:0>:	Auto-Sample T	ime bits ⁽¹⁾							
	11111 = 31 T. • • • • • •	AD								
hit 7 0	00000 = 0 IA		ion Clock Colo	at hita(2)						
Dit 7-0	ADC3<7.051 11111111 = -	TP • (ADCS<7: TP • (ADCS<7: TP • (ADCS<7: TP • (ADCS<7: TP • (ADCS<7:	0> + 1) = TP • 0> + 1) = TP • 0> + 1) = TP • 0> + 1) = TP •	256 = TAD 3 = TAD 2 = TAD 1 = TAD						
Note 1: 2:	This bit is only use This bit is not used	d if SSRC<2:0> if ADRC (AD10	· (AD1CON1< CON3<15>) =	7:5>) = 111 ar 1.	nd SSRCG (AD	1CON1<4>) =	0.			

REGISTER 23-3: AD1CON3: ADC1 CONTROL REGISTER 3

28.0 INSTRUCTION SET SUMMARY

Note: This data sheet summarizes the features of the dsPIC33EPXXXGP50X. dsPIC33EPXXXMC20X/50X and PIC24EPXXXGP/MC20X families of devices. It is not intended to be a comprehensive reference source. То complement the information in this data sheet, refer to the related section of the "dsPIC33/PIC24 Familv Reference Manual', which is available from the Microchip web site (www.microchip.com).

The dsPIC33EP instruction set is almost identical to that of the dsPIC30F and dsPIC33F. The PIC24EP instruction set is almost identical to that of the PIC24F and PIC24H.

Most instructions are a single program memory word (24 bits). Only three instructions require two program memory locations.

Each single-word instruction is a 24-bit word, divided into an 8-bit opcode, which specifies the instruction type and one or more operands, which further specify the operation of the instruction.

The instruction set is highly orthogonal and is grouped into five basic categories:

- · Word or byte-oriented operations
- · Bit-oriented operations
- · Literal operations
- DSP operations
- · Control operations

Table 28-1 lists the general symbols used in describing the instructions.

The dsPIC33E instruction set summary in Table 28-2 lists all the instructions, along with the status flags affected by each instruction.

Most word or byte-oriented W register instructions (including barrel shift instructions) have three operands:

- The first source operand, which is typically a register 'Wb' without any address modifier
- The second source operand, which is typically a register 'Ws' with or without an address modifier
- The destination of the result, which is typically a register 'Wd' with or without an address modifier

However, word or byte-oriented file register instructions have two operands:

- · The file register specified by the value 'f'
- The destination, which could be either the file register 'f' or the W0 register, which is denoted as 'WREG'

Most bit-oriented instructions (including simple rotate/ shift instructions) have two operands:

- The W register (with or without an address modifier) or file register (specified by the value of 'Ws' or 'f')
- The bit in the W register or file register (specified by a literal value or indirectly by the contents of register 'Wb')

The literal instructions that involve data movement can use some of the following operands:

- A literal value to be loaded into a W register or file register (specified by 'k')
- The W register or file register where the literal value is to be loaded (specified by 'Wb' or 'f')

However, literal instructions that involve arithmetic or logical operations use some of the following operands:

- The first source operand, which is a register 'Wb' without any address modifier
- The second source operand, which is a literal value
- The destination of the result (only if not the same as the first source operand), which is typically a register 'Wd' with or without an address modifier

The MAC class of DSP instructions can use some of the following operands:

- The accumulator (A or B) to be used (required operand)
- The W registers to be used as the two operands
- · The X and Y address space prefetch operations
- The X and Y address space prefetch destinations
- The accumulator write back destination

The other DSP instructions do not involve any multiplication and can include:

- The accumulator to be used (required)
- The source or destination operand (designated as Wso or Wdo, respectively) with or without an address modifier
- The amount of shift specified by a W register 'Wn' or a literal value

The control instructions can use some of the following operands:

- A program memory address
- The mode of the Table Read and Table Write instructions

Most instructions are a single word. Certain double-word instructions are designed to provide all the required information in these 48 bits. In the second word, the 8 MSbs are '0's. If this second word is executed as an instruction (by itself), it executes as a NOP.

The double-word instructions execute in two instruction cycles.

Most single-word instructions are executed in a single instruction cycle, unless a conditional test is true, or the Program Counter is changed as a result of the instruction, or a PSV or Table Read is performed, or an SFR register is read. In these cases, the execution takes multiple instruction cycles with the additional instruction cycle(s) executed as a NOP. Certain instructions that involve skipping over the subsequent instruction require either two or three cycles if the skip is performed, depending on whether the instruction being skipped is a single-word or two-word instruction. Moreover, double-word moves require two cycles.

Note: For more details on the instruction set, refer to the *"16-bit MCU and DSC Programmer's Reference Manual"* (DS70157). For more information on instructions that take more than one instruction cycle to execute, refer to **"CPU"** (DS70359) in the *"dsPIC33/PIC24 Family Reference Manual"*, particularly the **"Instruction Flow Types"** section.

Field	Description
#text	Means literal defined by "text"
(text)	Means "content of text"
[text]	Means "the location addressed by text"
{}	Optional field or operation
$a\in\{b,c,d\}$	a is selected from the set of values b, c, d
<n:m></n:m>	Register bit field
.b	Byte mode selection
.d	Double-Word mode selection
.S	Shadow register select
.w	Word mode selection (default)
Acc	One of two accumulators {A, B}
AWB	Accumulator write back destination address register \in {W13, [W13]+ = 2}
bit4	4-bit bit selection field (used in word addressed instructions) $\in \{015\}$
C, DC, N, OV, Z	MCU Status bits: Carry, Digit Carry, Negative, Overflow, Sticky Zero
Expr	Absolute address, label or expression (resolved by the linker)
f	File register address ∈ {0x00000x1FFF}
lit1	1-bit unsigned literal $\in \{0,1\}$
lit4	4-bit unsigned literal ∈ {015}
lit5	5-bit unsigned literal $\in \{031\}$
lit8	8-bit unsigned literal \in {0255}
lit10	10-bit unsigned literal \in {0255} for Byte mode, {0:1023} for Word mode
lit14	14-bit unsigned literal $\in \{016384\}$
lit16	16-bit unsigned literal $\in \{065535\}$
lit23	23-bit unsigned literal \in {08388608}; LSb must be '0'
None	Field does not require an entry, can be blank
OA, OB, SA, SB	DSP Status bits: ACCA Overflow, ACCB Overflow, ACCA Saturate, ACCB Saturate
PC	Program Counter
Slit10	10-bit signed literal \in {-512511}
Slit16	16-bit signed literal ∈ {-3276832767}
Slit6	6-bit signed literal \in {-1616}
Wb	Base W register ∈ {W0W15}
Wd	Destination W register \in { Wd, [Wd], [Wd++], [Wd], [++Wd], [Wd] }
Wdo	Destination W register ∈ { Wnd, [Wnd], [Wnd++], [Wnd], [++Wnd], [Wnd], [Wnd+Wb] }

TABLE 28-1: SYMBOLS USED IN OPCODE DESCRIPTIONS

Base Instr #	Assembly Mnemonic		Assembly Syntax	Description	# of Words	# of Cycles ⁽²⁾	Status Flags Affected
25	DAW	DAW	Wn	Wn = decimal adjust Wn	1	1	С
26	DEC	DEC	f	f = f - 1	1	1	C,DC,N,OV,Z
		DEC	f,WREG	WREG = f – 1	1	1	C,DC,N,OV,Z
		DEC	Ws,Wd	Wd = Ws - 1	1	1	C,DC,N,OV,Z
27	DEC2	DEC2	f	f = f – 2	1	1	C,DC,N,OV,Z
		DEC2	f,WREG	WREG = f – 2	1	1	C,DC,N,OV,Z
		DEC2	Ws,Wd	Wd = Ws - 2	1	1	C,DC,N,OV,Z
28	DISI	DISI	#lit14	Disable Interrupts for k instruction cycles	1	1	None
29	DIV	DIV.S	Wm,Wn	Signed 16/16-bit Integer Divide	1	18	N,Z,C,OV
		DIV.SD	Wm,Wn	Signed 32/16-bit Integer Divide	1	18	N,Z,C,OV
		DIV.U	Wm,Wn	Unsigned 16/16-bit Integer Divide	1	18	N,Z,C,OV
		DIV.UD	Wm,Wn	Unsigned 32/16-bit Integer Divide	1	18	N,Z,C,OV
30	DIVF	DIVF	Wm, Wn ⁽¹⁾	Signed 16/16-bit Fractional Divide	1	18	N,Z,C,OV
31	DO	DO	#lit15,Expr ⁽¹⁾	Do code to PC + Expr, lit15 + 1 times	2	2	None
		DO	Wn, Expr ⁽¹⁾	Do code to PC + Expr, (Wn) + 1 times	2	2	None
32	ED	ED	Wm*Wm,Acc,Wx,Wy,Wxd ⁽¹⁾	Euclidean Distance (no accumulate)	1	1	OA,OB,OAB, SA,SB,SAB
33	EDAC	EDAC	Wm*Wm,Acc,Wx,Wy,Wxd ⁽¹⁾	Euclidean Distance	1	1	OA,OB,OAB, SA,SB,SAB
34	EXCH	EXCH	Wns,Wnd	Swap Wns with Wnd	1	1	None
35	FBCL	FBCL	Ws,Wnd	Find Bit Change from Left (MSb) Side	1	1	С
36	FF1L	FF1L	Ws,Wnd	Find First One from Left (MSb) Side	1	1	С
37	FF1R	FF1R	Ws,Wnd	Find First One from Right (LSb) Side	1	1	С
38	GOTO	GOTO	Expr	Go to address	2	4	None
		GOTO	Wn	Go to indirect	1	4	None
		GOTO.L	Wn	Go to indirect (long address)	1	4	None
39	INC	INC	f	f = f + 1	1	1	C,DC,N,OV,Z
		INC	f,WREG	WREG = f + 1	1	1	C,DC,N,OV,Z
		INC	Ws,Wd	Wd = Ws + 1	1	1	C,DC,N,OV,Z
40	INC2	INC2	f	f = f + 2	1	1	C,DC,N,OV,Z
		INC2	f,WREG	WREG = f + 2	1	1	C,DC,N,OV,Z
		INC2	Ws,Wd	Wd = Ws + 2	1	1	C,DC,N,OV,Z
41	IOR	IOR	f	f = f .IOR. WREG	1	1	N,Z
		IOR	f,WREG	WREG = f.IOR. WREG	1	1	N,Z
		IOR	#lit10,Wn	Wd = lit10 .IOR. Wd	1	1	N,Z
		IOR	Wb,Ws,Wd	Wd = Wb .IOR. Ws	1	1	N,Z
		IOR	Wb,#lit5,Wd	Wd = Wb .IOR. lit5	1	1	N,Z
42	LAC	LAC	Wso,#Slit4,Acc	Load Accumulator	1	1	OA,OB,OAB, SA,SB,SAB
43	LNK	LNK	#lit14	Link Frame Pointer	1	1	SFA
44	LSR	LSR	f	f = Logical Right Shift f	1	1	C,N,OV,Z
		LSR	f,WREG	WREG = Logical Right Shift f	1	1	C,N,OV,Z
		LSR	Ws,Wd	Wd = Logical Right Shift Ws	1	1	C,N,OV,Z
		LSR	Wb,Wns,Wnd	Wnd = Logical Right Shift Wb by Wns	1	1	N,Z
		LSR	Wb,#lit5,Wnd	Wnd = Logical Right Shift Wb by lit5	1	1	N,Z
45	MAC	MAC	Wm*Wn,Acc,Wx,Wxd,Wy,Wyd,AWB ⁽¹⁾	Multiply and Accumulate	1	1	OA,OB,OAB, SA,SB,SAB
		MAC	Wm*Wm,Acc,Wx,Wxd,Wy,Wyd ⁽¹⁾	Square and Accumulate	1	1	OA,OB,OAB, SA,SB,SAB

TABLE 28-2: INSTRUCTION SET OVERVIEW (CONTINUED)

Note 1: These instructions are available in dsPIC33EPXXXMC20X/50X and PIC24EPXXXMC20X devices only.

2: Read and Read-Modify-Write (e.g., bit operations and logical operations) on non-CPU SFRs incur an additional instruction cycle.

DC CHARACTERISTICS			$\begin{array}{llllllllllllllllllllllllllllllllllll$					
Parameter No.	Тур.	Max.	Units	Conditions				
Idle Current (IDLE) ⁽¹⁾								
DC40d	3	8	mA	-40°C		10 MIPS		
DC40a	3	8	mA	+25°C	2 21/			
DC40b	3	8	mA	+85°C	3.3V			
DC40c	3	8	mA	+125°C				
DC42d	6	12	mA	-40°C		20 MIPS		
DC42a	6	12	mA	+25°C	3 3\/			
DC42b	6	12	mA	+85°C	5.5 V			
DC42c	6	12	mA	+125°C				
DC44d	11	18	mA	-40°C		40 MIPS		
DC44a	11	18	mA	+25°C	3 3\/			
DC44b	11	18	mA	+85°C	5.5 V			
DC44c	11	18	mA	+125°C				
DC45d	17	27	mA	-40°C		60 MIPS		
DC45a	17	27	mA	+25°C	3 3\/			
DC45b	17	27	mA	+85°C	5.5V			
DC45c	17	27	mA	+125°C				
DC46d	20	35	mA	-40°C				
DC46a	20	35	mA	+25°C	3.3V	70 MIPS		
DC46b	20	35	mA	+85°C				

TABLE 30-7: DC CHARACTERISTICS: IDLE CURRENT (lidle)

Note 1: Base Idle current (IIDLE) is measured as follows:

• CPU core is off, oscillator is configured in EC mode and external clock is active; OSC1 is driven with external square wave from rail-to-rail (EC clock overshoot/undershoot < 250 mV required)

- · CLKO is configured as an I/O input pin in the Configuration Word
- All I/O pins are configured as inputs and pulled to Vss
- $\overline{\text{MCLR}}$ = VDD, WDT and FSCM are disabled
- No peripheral modules are operating; however, every peripheral is being clocked (all PMDx bits are zeroed)
- The NVMSIDL bit (NVMCON<12>) = 1 (i.e., Flash regulator is set to standby while the device is in Idle mode)
- The VREGSF bit (RCON<11>) = 0 (i.e., Flash regulator is set to standby while the device is in Sleep mode)
- JTAG is disabled

TABLE 30-37:SPI2 SLAVE MODE (FULL-DUPLEX, CKE = 1, CKP = 0, SMP = 0)TIMING REQUIREMENTS

AC CHARACTERISTICS			$\begin{tabular}{lllllllllllllllllllllllllllllllllll$				
Param.	Symbol	Characteristic ⁽¹⁾	Min.	Typ. ⁽²⁾	Max.	Units	Conditions
SP70	FscP	Maximum SCK2 Input Frequency	-	—	Lesser of FP or 15	MHz	(Note 3)
SP72	TscF	SCK2 Input Fall Time	—	_	_	ns	See Parameter DO32 (Note 4)
SP73	TscR	SCK2 Input Rise Time	—	—	—	ns	See Parameter DO31 (Note 4)
SP30	TdoF	SDO2 Data Output Fall Time	—	—	—	ns	See Parameter DO32 (Note 4)
SP31	TdoR	SDO2 Data Output Rise Time	—	—	—	ns	See Parameter DO31 (Note 4)
SP35	TscH2doV, TscL2doV	SDO2 Data Output Valid after SCK2 Edge	—	6	20	ns	
SP36	TdoV2scH, TdoV2scL	SDO2 Data Output Setup to First SCK2 Edge	30	—	—	ns	
SP40	TdiV2scH, TdiV2scL	Setup Time of SDI2 Data Input to SCK2 Edge	30	—	—	ns	
SP41	TscH2diL, TscL2diL	Hold Time of SDI2 Data Input to SCK2 Edge	30	_	_	ns	
SP50	TssL2scH, TssL2scL	$\overline{SS2}$ ↓ to SCK2 ↑ or SCK2 ↓ Input	120	—	—	ns	
SP51	TssH2doZ	SS2 ↑ to SDO2 Output High-Impedance	10	—	50	ns	(Note 4)
SP52	TscH2ssH TscL2ssH	SS2 ↑ after SCK2 Edge	1.5 Tcy + 40	_	_	ns	(Note 4)
SP60	TssL2doV	SDO2 Data Output Valid after SS2 Edge	-	—	50	ns	

Note 1: These parameters are characterized, but are not tested in manufacturing.

2: Data in "Typical" column is at 3.3V, +25°C unless otherwise stated.

3: The minimum clock period for SCK2 is 66.7 ns. Therefore, the SCK2 clock generated by the master must not violate this specification.

4: Assumes 50 pF load on all SPI2 pins.





TABLE 30-44:SPI1 MASTER MODE (FULL-DUPLEX, CKE = 0, CKP = x, SMP = 1)TIMING REQUIREMENTS

AC CHARACTERISTICS			Standard Operating Conditions: 3.0V to 3.6V(unless otherwise stated)Operating temperature $-40^{\circ}C \le TA \le +85^{\circ}C$ for Industrial $-40^{\circ}C \le TA \le +125^{\circ}C$ for Extended				
Param.	Symbol	Characteristic ⁽¹⁾	Min.	Typ. ⁽²⁾	Max.	Units	Conditions
SP10	FscP	Maximum SCK1 Frequency	_	—	10	MHz	-40°C to +125°C (Note 3)
SP20	TscF	SCK1 Output Fall Time	_	—	—	ns	See Parameter DO32 (Note 4)
SP21	TscR	SCK1 Output Rise Time	_	—	—	ns	See Parameter DO31 (Note 4)
SP30	TdoF	SDO1 Data Output Fall Time	_	—	—	ns	See Parameter DO32 (Note 4)
SP31	TdoR	SDO1 Data Output Rise Time	_	—	—	ns	See Parameter DO31 (Note 4)
SP35	TscH2doV, TscL2doV	SDO1 Data Output Valid after SCK1 Edge	_	6	20	ns	
SP36	TdoV2scH, TdoV2scL	SDO1 Data Output Setup to First SCK1 Edge	30	_	_	ns	
SP40	TdiV2scH, TdiV2scL	Setup Time of SDI1 Data Input to SCK1 Edge	30	_	_	ns	
SP41	TscH2diL, TscL2diL	Hold Time of SDI1 Data Input to SCK1 Edge	30			ns	

Note 1: These parameters are characterized, but are not tested in manufacturing.

2: Data in "Typical" column is at 3.3V, +25°C unless otherwise stated.

- **3:** The minimum clock period for SCK1 is 100 ns. The clock generated in Master mode must not violate this specification.
- 4: Assumes 50 pF load on all SPI1 pins.

33.1 Package Marking Information (Continued)



28-Lead Plastic Small Outline (SO) - Wide, 7.50 mm Body [SOIC]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging





	MILLIMETERS					
Dimension	MIN	NOM	MAX			
Number of Pins	N	28				
Pitch	е	1.27 BSC				
Overall Height	Α	-	-	2.65		
Molded Package Thickness	A2	2.05	-	-		
Standoff §	A1	0.10	-	0.30		
Overall Width	E	10.30 BSC				
Molded Package Width	E1	7.50 BSC				
Overall Length	D	17.90 BSC				
Chamfer (Optional)	h	0.25	-	0.75		
Foot Length	L	0.40	-	1.27		
Footprint	L1	1.40 REF				
Lead Angle	Θ	0°	-	-		
Foot Angle	φ	0°	-	8°		
Lead Thickness	С	0.18	-	0.33		
Lead Width	b	0.31	-	0.51		
Mold Draft Angle Top	α	5°	-	15°		
Mold Draft Angle Bottom	β	5°	-	15°		

Notes:

- 1. Pin 1 visual index feature may vary, but must be located within the hatched area.
- 2. § Significant Characteristic
- 3. Dimension D does not include mold flash, protrusions or gate burrs, which shall not exceed 0.15 mm per end. Dimension E1 does not include interlead flash or protrusion, which shall not exceed 0.25 mm per side.
- 4. Dimensioning and tolerancing per ASME Y14.5M
 - BSC: Basic Dimension. Theoretically exact value shown without tolerances. REF: Reference Dimension, usually without tolerance, for information purposes only.
- 5. Datums A & B to be determined at Datum H.

Microchip Technology Drawing C04-052C Sheet 2 of 2