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Details

Product Status	Active
Core Processor	PIC
Core Size	16-Bit
Speed	70 MIPS
Connectivity	I ² C, IrDA, LINbus, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, DMA, POR, PWM, WDT
Number of I/O	53
Program Memory Size	128KB (43K x 24)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	8K x 16
Voltage - Supply (Vcc/Vdd)	3V ~ 3.6V
Data Converters	A/D 16x10b/12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	64-TQFP
Supplier Device Package	64-TQFP (10x10)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/pic24ep128gp206-i-pt

3.0 CPU

Note 1: This data sheet summarizes the features of the dsPIC33EPXXXGP50X, dsPIC33EPXXXMC20X/50X and PIC24EPXXXGP/MC20X families of devices. It is not intended to be a comprehensive reference source. To complement the information in this data sheet, refer to “**CPU**” (DS70359) in the “*dsPIC33/PIC24 Family Reference Manual*”, which is available from the Microchip web site (www.microchip.com).

2: Some registers and associated bits described in this section may not be available on all devices. Refer to **Section 4.0 “Memory Organization”** in this data sheet for device-specific register and bit information.

The dsPIC33EPXXXGP50X, dsPIC33EPXXXMC20X/50X and PIC24EPXXXGP/MC20X CPU has a 16-bit (data) modified Harvard architecture with an enhanced instruction set, including significant support for digital signal processing. The CPU has a 24-bit instruction word with a variable length opcode field. The Program Counter (PC) is 23 bits wide and addresses up to 4M x 24 bits of user program memory space.

An instruction prefetch mechanism helps maintain throughput and provides predictable execution. Most instructions execute in a single-cycle effective execution rate, with the exception of instructions that change the program flow, the double-word move (MOV.D) instruction, PSV accesses and the table instructions. Overhead-free program loop constructs are supported using the DO and REPEAT instructions, both of which are interruptible at any point.

3.1 Registers

The dsPIC33EPXXXGP50X, dsPIC33EPXXXMC20X/50X and PIC24EPXXXGP/MC20X devices have sixteen, 16-bit working registers in the programmer's model. Each of the working registers can act as a data, address or address offset register. The 16th working register (W15) operates as a Software Stack Pointer for interrupts and calls.

3.2 Instruction Set

The instruction set for dsPIC33EPXXXGP50X and dsPIC33EPXXXMC20X/50X devices has two classes of instructions: the MCU class of instructions and the DSP class of instructions. The instruction set for PIC24EPXXXGP/MC20X devices has the MCU class of instructions only and does not support DSP instructions. These two instruction classes are seamlessly integrated into the architecture and execute from a single execution unit. The instruction set includes many addressing modes and was designed for optimum C compiler efficiency.

3.3 Data Space Addressing

The base Data Space can be addressed as 64 Kbytes (32K words).

The Data Space includes two ranges of memory, referred to as X and Y data memory. Each memory range is accessible through its own independent Address Generation Unit (AGU). The MCU class of instructions operates solely through the X memory AGU, which accesses the entire memory map as one linear Data Space. On dsPIC33EPXXXMC20X/50X and dsPIC33EPXXXGP50X devices, certain DSP instructions operate through the X and Y AGUs to support dual operand reads, which splits the data address space into two parts. The X and Y Data Spaces have memory locations that are device-specific, and are described further in the data memory maps in **Section 4.2 “Data Address Space”**.

The upper 32 Kbytes of the Data Space memory map can optionally be mapped into Program Space (PS) at any 32-Kbyte aligned program word boundary. The Program-to-Data Space mapping feature, known as Program Space Visibility (PSV), lets any instruction access Program Space as if it were Data Space. Moreover, the Base Data Space address is used in conjunction with a Read or Write Page register (DSRPAG or DSWPAG) to form an Extended Data Space (EDS) address. The EDS can be addressed as 8M words or 16 Mbytes. Refer to the “**Data Memory**” (DS70595) and “**Program Memory**” (DS70613) sections in the “*dsPIC33/PIC24 Family Reference Manual*” for more details on EDS, PSV and table accesses.

On the dsPIC33EPXXXMC20X/50X and dsPIC33EPXXXGP50X devices, overhead-free circular buffers (Modulo Addressing) are supported in both X and Y address spaces. The Modulo Addressing removes the software boundary checking overhead for DSP algorithms. The X AGU Circular Addressing can be used with any of the MCU class of instructions. The X AGU also supports Bit-Reversed Addressing to greatly simplify input or output data re-ordering for radix-2 FFT algorithms. PIC24EPXXXGP/MC20X devices do not support Modulo and Bit-Reversed Addressing.

3.4 Addressing Modes

The CPU supports these addressing modes:

- Inherent (no operand)
- Relative
- Literal
- Memory Direct
- Register Direct
- Register Indirect

Each instruction is associated with a predefined addressing mode group, depending upon its functional requirements. As many as six addressing modes are supported for each instruction.

3.7 CPU Control Registers

REGISTER 3-1: SR: CPU STATUS REGISTER

R/W-0	R/W-0	R/W-0	R/W-0	R/C-0	R/C-0	R-0	R/W-0
OA ⁽¹⁾	OB ⁽¹⁾	SA ^(1,4)	SB ^(1,4)	OAB ⁽¹⁾	SAB ⁽¹⁾	DA ⁽¹⁾	DC
bit 15							bit 8

R/W-0 ^(2,3)	R/W-0 ^(2,3)	R/W-0 ^(2,3)	R-0	R/W-0	R/W-0	R/W-0	R/W-0
IPL2	IPL1	IPL0	RA	N	OV	Z	C
bit 7							bit 0

Legend:	C = Clearable bit		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

- bit 15 **OA:** Accumulator A Overflow Status bit⁽¹⁾
 1 = Accumulator A has overflowed
 0 = Accumulator A has not overflowed
- bit 14 **OB:** Accumulator B Overflow Status bit⁽¹⁾
 1 = Accumulator B has overflowed
 0 = Accumulator B has not overflowed
- bit 13 **SA:** Accumulator A Saturation 'Sticky' Status bit^(1,4)
 1 = Accumulator A is saturated or has been saturated at some time
 0 = Accumulator A is not saturated
- bit 12 **SB:** Accumulator B Saturation 'Sticky' Status bit^(1,4)
 1 = Accumulator B is saturated or has been saturated at some time
 0 = Accumulator B is not saturated
- bit 11 **OAB:** OA || OB Combined Accumulator Overflow Status bit⁽¹⁾
 1 = Accumulators A or B have overflowed
 0 = Neither Accumulators A or B have overflowed
- bit 10 **SAB:** SA || SB Combined Accumulator 'Sticky' Status bit⁽¹⁾
 1 = Accumulators A or B are saturated or have been saturated at some time
 0 = Neither Accumulators A or B are saturated
- bit 9 **DA:** DO Loop Active bit⁽¹⁾
 1 = DO loop is in progress
 0 = DO loop is not in progress
- bit 8 **DC:** MCU ALU Half Carry/Borrow bit
 1 = A carry-out from the 4th low-order bit (for byte-sized data) or 8th low-order bit (for word-sized data) of the result occurred
 0 = No carry-out from the 4th low-order bit (for byte-sized data) or 8th low-order bit (for word-sized data) of the result occurred

- Note 1:** This bit is available on dsPIC33EPXXXMC20X/50X and dsPIC33EPXXXGP50X devices only.
- Note 2:** The IPL<2:0> bits are concatenated with the IPL<3> bit (CORCON<3>) to form the CPU Interrupt Priority Level. The value in parentheses indicates the IPL, if IPL<3> = 1. User interrupts are disabled when IPL<3> = 1.
- Note 3:** The IPL<2:0> Status bits are read-only when the NSTDIS bit (INTCON1<15>) = 1.
- Note 4:** A data write to the SR register can modify the SA and SB bits by either a data write to SA and SB or by clearing the SAB bit. To avoid a possible SA or SB bit write race condition, the SA and SB bits should not be modified using bit operations.

4.1.1 PROGRAM MEMORY ORGANIZATION

The program memory space is organized in word-addressable blocks. Although it is treated as 24 bits wide, it is more appropriate to think of each address of the program memory as a lower and upper word, with the upper byte of the upper word being unimplemented. The lower word always has an even address, while the upper word has an odd address (Figure 4-6).

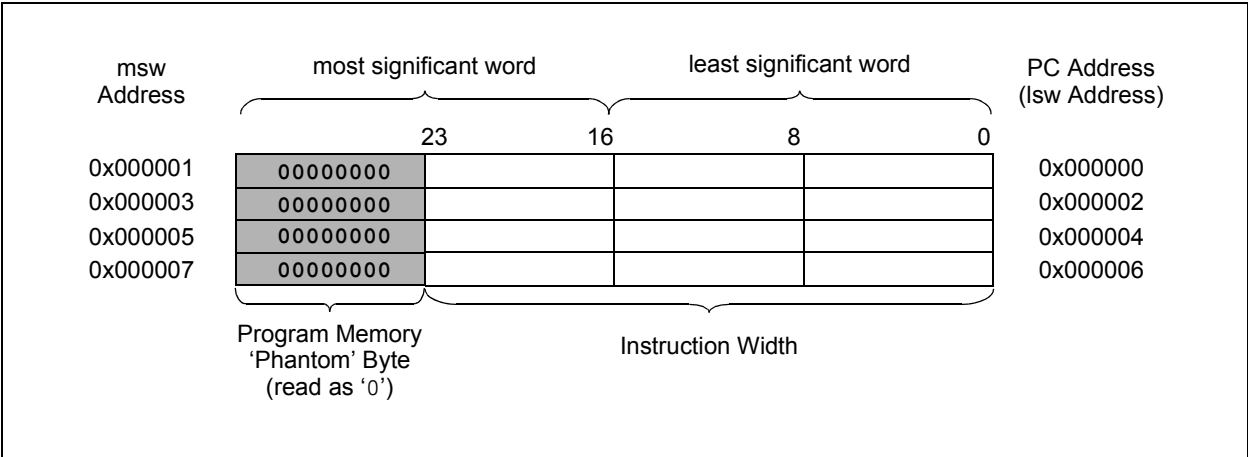
Program memory addresses are always word-aligned on the lower word and addresses are incremented, or decremented by two, during code execution. This arrangement provides compatibility with data memory space addressing and makes data in the program memory space accessible.

4.1.2 INTERRUPT AND TRAP VECTORS

All dsPIC33EPXXXGP50X, dsPIC33EPXXXMC20X/50X and PIC24EPXXXGP/MC20X devices reserve the addresses between 0x000000 and 0x000200 for hard-coded program execution vectors. A hardware Reset vector is provided to redirect code execution from the default value of the PC on device Reset to the actual start of code. A GOTO instruction is programmed by the user application at address, 0x000000, of Flash memory, with the actual address for the start of code at address, 0x000002, of Flash memory.

A more detailed discussion of the Interrupt Vector Tables (IVTs) is provided in Section 7.1 “Interrupt Vector Table”.

FIGURE 4-6: PROGRAM MEMORY ORGANIZATION



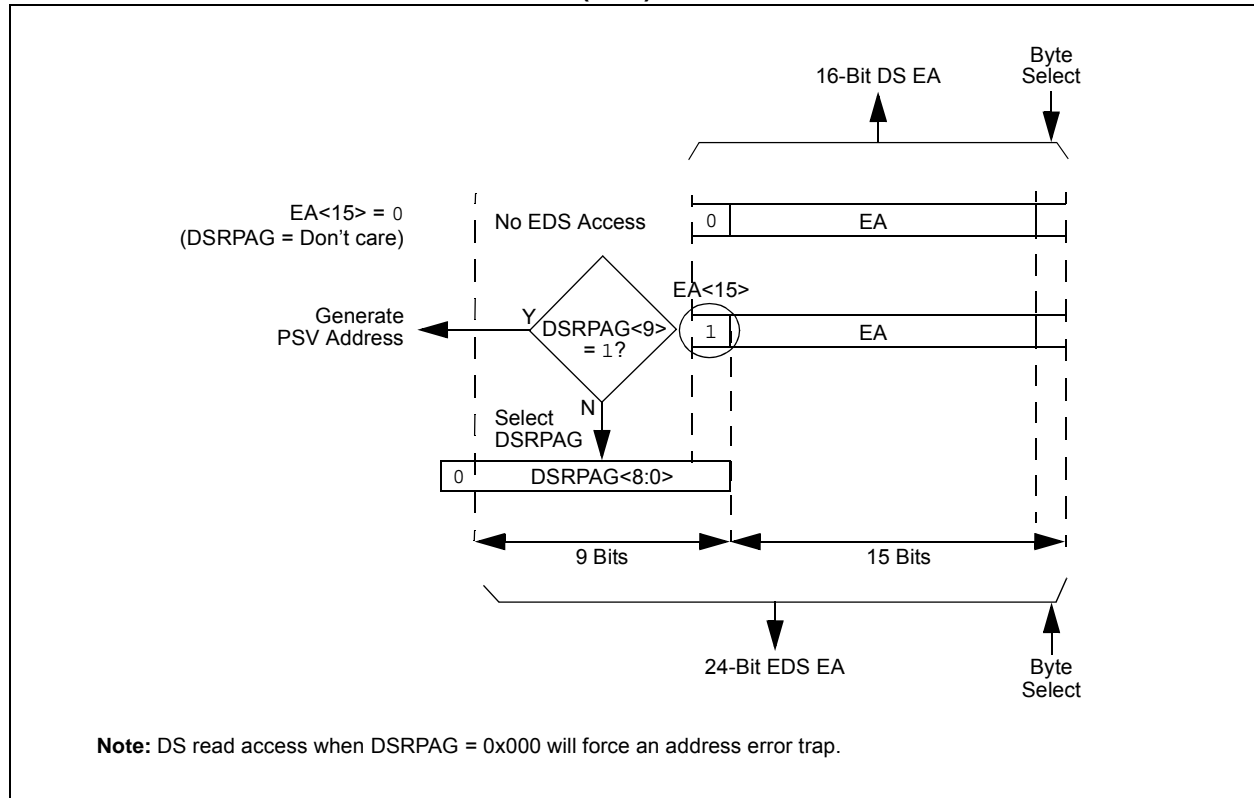
4.4.1 PAGED MEMORY SCHEME

The dsPIC33EPXXXGP50X, dsPIC33EPXXXMC20X/50X and PIC24EPXXXGP/MC20X architecture extends the available Data Space through a paging scheme, which allows the available Data Space to be accessed using MOV instructions in a linear fashion for pre-modified and post-modified Effective Addresses (EA). The upper half of the base Data Space address is used in conjunction with the Data Space Page registers, the 10-bit Read Page register (DSRPAG) or the 9-bit Write Page register (DSWPAG), to form an Extended Data Space (EDS)

address or Program Space Visibility (PSV) address. The Data Space Page registers are located in the SFR space.

Construction of the EDS address is shown in Example 4-1. When DSRPAG<9> = 0 and the base address bit, EA<15> = 1, the DSRPAG<8:0> bits are concatenated onto EA<14:0> to form the 24-bit EDS read address. Similarly, when base address bit, EA<15> = 1, DSWPAG<8:0> are concatenated onto EA<14:0> to form the 24-bit EDS write address.

EXAMPLE 4-1: EXTENDED DATA SPACE (EDS) READ ADDRESS GENERATION



REGISTER 8-12: DMARQC: DMA REQUEST COLLISION STATUS REGISTER

U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
—	—	—	—	—	—	—	—
bit 15				bit 8			

U-0	U-0	U-0	U-0	R-0	R-0	R-0	R-0
—	—	—	—	RQCOL3	RQCOL2	RQCOL1	RQCOL0
bit 7				bit 0			

Legend:

R = Readable bit

W = Writable bit

U = Unimplemented bit, read as '0'

-n = Value at POR

'1' = Bit is set

'0' = Bit is cleared

x = Bit is unknown

bit 15-4 **Unimplemented:** Read as '0'

bit 3 **RQCOL3:** DMA Channel 3 Transfer Request Collision Flag bit
 1 = User force and interrupt-based request collision is detected
 0 = No request collision is detected

bit 2 **RQCOL2:** DMA Channel 2 Transfer Request Collision Flag bit
 1 = User force and interrupt-based request collision is detected
 0 = No request collision is detected

bit 1 **RQCOL1:** DMA Channel 1 Transfer Request Collision Flag bit
 1 = User force and interrupt-based request collision is detected
 0 = No request collision is detected

bit 0 **RQCOL0:** DMA Channel 0 Transfer Request Collision Flag bit
 1 = User force and interrupt-based request collision is detected
 0 = No request collision is detected

12.0 TIMER1

Note 1: This data sheet summarizes the features of the dsPIC33EPXXXGP50X, dsPIC33EPXXXMC20X/50X and PIC24EPXXXGP/MC20X families of devices. It is not intended to be a comprehensive reference source. To complement the information in this data sheet, refer to “Timers” (DS70362) in the “dsPIC33/PIC24 Family Reference Manual”, which is available from the Microchip web site (www.microchip.com).

2: Some registers and associated bits described in this section may not be available on all devices. Refer to **Section 4.0 “Memory Organization”** in this data sheet for device-specific register and bit information.

The Timer1 module is a 16-bit timer that can operate as a free-running interval timer/counter.

The Timer1 module has the following unique features over other timers:

- Can be operated in Asynchronous Counter mode from an external clock source
- The external clock input (T1CK) can optionally be synchronized to the internal device clock and the clock synchronization is performed after the prescaler

A block diagram of Timer1 is shown in Figure 12-1.

The Timer1 module can operate in one of the following modes:

- Timer mode
- Gated Timer mode
- Synchronous Counter mode
- Asynchronous Counter mode

In Timer and Gated Timer modes, the input clock is derived from the internal instruction cycle clock (Fcy). In Synchronous and Asynchronous Counter modes, the input clock is derived from the external clock input at the T1CK pin.

The Timer modes are determined by the following bits:

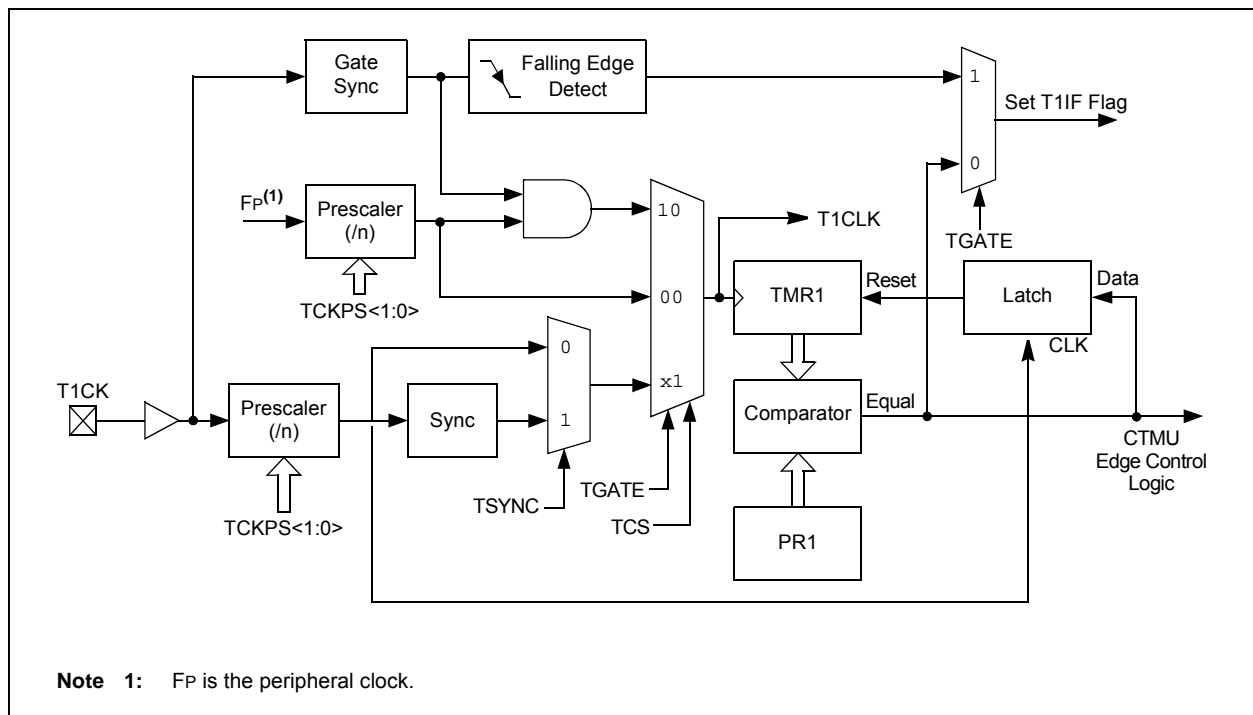
- Timer Clock Source Control bit (TCS): T1CON<1>
- Timer Synchronization Control bit (TSYNC): T1CON<2>
- Timer Gate Control bit (TGATE): T1CON<6>

Timer control bit setting for different operating modes are given in the Table 12-1.

TABLE 12-1: TIMER MODE SETTINGS

Mode	TCS	TGATE	TSYNC
Timer	0	0	x
Gated Timer	0	1	x
Synchronous Counter	1	x	1
Asynchronous Counter	1	x	0

FIGURE 12-1: 16-BIT TIMER1 MODULE BLOCK DIAGRAM



16.1.2 WRITE-PROTECTED REGISTERS

On dsPIC33EPXXXMC20X/50X and PIC24EPXXXMC20X devices, write protection is implemented for the IOCONx and FCLCONx registers. The write protection feature prevents any inadvertent writes to these registers. This protection feature can be controlled by the PWMLOCK Configuration bit (FOSCSEL<6>). The default state of the write protection feature is enabled (PWMLOCK = 1). The write protection feature can be disabled by configuring, PWMLOCK = 0.

To gain write access to these locked registers, the user application must write two consecutive values of (0xABCD and 0x4321) to the PWMKEY register to perform the unlock operation. The write access to the IOCONx or FCLCONx registers must be the next SFR access following the unlock process. There can be no other SFR accesses during the unlock process and subsequent write access. To write to both the IOCONx and FCLCONx registers requires two unlock operations.

The correct unlocking sequence is described in Example 16-1.

EXAMPLE 16-1: PWMx WRITE-PROTECTED REGISTER UNLOCK SEQUENCE

```
; FLT32 pin must be pulled low externally in order to clear and disable the fault
; Writing to FCLCON1 register requires unlock sequence

mov #0xabcd,w10      ; Load first unlock key to w10 register
mov #0x4321,w11      ; Load second unlock key to w11 register
mov #0x0000,w0       ; Load desired value of FCLCON1 register in w0
mov w10, PWMKEY      ; Write first unlock key to PWMKEY register
mov w11, PWMKEY      ; Write second unlock key to PWMKEY register
mov w0,FCLCON1       ; Write desired value to FCLCON1 register

; Set PWM ownership and polarity using the IOCON1 register
; Writing to IOCON1 register requires unlock sequence

mov #0xabcd,w10      ; Load first unlock key to w10 register
mov #0x4321,w11      ; Load second unlock key to w11 register
mov #0xF000,w0       ; Load desired value of IOCON1 register in w0
mov w10, PWMKEY      ; Write first unlock key to PWMKEY register
mov w11, PWMKEY      ; Write second unlock key to PWMKEY register
mov w0,IOCON1        ; Write desired value to IOCON1 register
```


REGISTER 16-10: DTRx: PWMx DEAD-TIME REGISTER

U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
—	—	DTRx<13:8>					
bit 15							bit 8

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
DTRx<7:0>							
bit 7							bit 0

Legend:

R = Readable bit W = Writable bit U = Unimplemented bit, read as '0'
-n = Value at POR '1' = Bit is set '0' = Bit is cleared x = Bit is unknown

bit 15-14 **Unimplemented:** Read as '0'

bit 13-0 **DTRx<13:0>:** Unsigned 14-Bit Dead-Time Value for PWMx Dead-Time Unit bits

REGISTER 16-11: ALTDTRx: PWMx ALTERNATE DEAD-TIME REGISTER

U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
—	—	ALTDTRx<13:8>					
bit 15							bit 8

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
ALTDTRx<7:0>							
bit 7							bit 0

Legend:

R = Readable bit W = Writable bit U = Unimplemented bit, read as '0'
-n = Value at POR '1' = Bit is set '0' = Bit is cleared x = Bit is unknown

bit 15-14 **Unimplemented:** Read as '0'

bit 13-0 **ALTDTRx<13:0>:** Unsigned 14-Bit Dead-Time Value for PWMx Dead-Time Unit bits

REGISTER 16-15: FCLCONx: PWMx FAULT CURRENT-LIMIT CONTROL REGISTER⁽¹⁾

- bit 7-3 **FLTSRC<4:0>**: Fault Control Signal Source Select for PWM Generator # bits
- 11111 = Fault 32 (**default**)
 - 11110 = Reserved
 - .
 - .
 - .
 - 01100 = Reserved
 - 01011 = Comparator 4
 - 01010 = Op Amp/Comparator 3
 - 01001 = Op Amp/Comparator 2
 - 01000 = Op Amp/Comparator 1
 - 00111 = Reserved
 - 00110 = Reserved
 - 00101 = Reserved
 - 00100 = Reserved
 - 00011 = Fault 4
 - 00010 = Fault 3
 - 00001 = Fault 2
 - 00000 = Fault 1
- bit 2 **FLTPOL**: Fault Polarity for PWM Generator # bit⁽²⁾
- 1 = The selected Fault source is active-low
 - 0 = The selected Fault source is active-high
- bit 1-0 **FLTMOD<1:0>**: Fault Mode for PWM Generator # bits
- 11 = Fault input is disabled
 - 10 = Reserved
 - 01 = The selected Fault source forces PWMxH, PWMxL pins to FLTDAT values (cycle)
 - 00 = The selected Fault source forces PWMxH, PWMxL pins to FLTDAT values (latched condition)

- Note 1:** If the PWMLOCK Configuration bit (FOSCSEL<6>) is a '1', the IOCONx register can only be written after the unlock sequence has been executed.
- 2:** These bits should be changed only when PTEN = 0. Changing the clock selection during operation will yield unpredictable results.

REGISTER 18-2: SPIxCON1: SPIx CONTROL REGISTER 1

U-0	U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
—	—	—	DISSCK	DISSDO	MODE16	SMP	CKE ⁽¹⁾
bit 15							bit 8

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
SSEN ⁽²⁾	CKP	MSTEN	SPRE2 ⁽³⁾	SPRE1 ⁽³⁾	SPRE0 ⁽³⁾	PPRE1 ⁽³⁾	PPRE0 ⁽³⁾
bit 7							bit 0

Legend:

R = Readable bit W = Writable bit U = Unimplemented bit, read as '0'
 -n = Value at POR '1' = Bit is set '0' = Bit is cleared x = Bit is unknown

- bit 15-13 **Unimplemented:** Read as '0'
- bit 12 **DISSCK:** Disable SCKx Pin bit (SPIx Master modes only)
 1 = Internal SPIx clock is disabled, pin functions as I/O
 0 = Internal SPIx clock is enabled
- bit 11 **DISSDO:** Disable SDOx Pin bit
 1 = SDOx pin is not used by the module; pin functions as I/O
 0 = SDOx pin is controlled by the module
- bit 10 **MODE16:** Word/Byte Communication Select bit
 1 = Communication is word-wide (16 bits)
 0 = Communication is byte-wide (8 bits)
- bit 9 **SMP:** SPIx Data Input Sample Phase bit
Master mode:
 1 = Input data is sampled at end of data output time
 0 = Input data is sampled at middle of data output time
Slave mode:
 SMP must be cleared when SPIx is used in Slave mode.
- bit 8 **CKE:** SPIx Clock Edge Select bit⁽¹⁾
 1 = Serial output data changes on transition from active clock state to Idle clock state (refer to bit 6)
 0 = Serial output data changes on transition from Idle clock state to active clock state (refer to bit 6)
- bit 7 **SSEN:** Slave Select Enable bit (Slave mode)⁽²⁾
 1 = \overline{SSx} pin is used for Slave mode
 0 = \overline{SSx} pin is not used by the module; pin is controlled by port function
- bit 6 **CKP:** Clock Polarity Select bit
 1 = Idle state for clock is a high level; active state is a low level
 0 = Idle state for clock is a low level; active state is a high level
- bit 5 **MSTEN:** Master Mode Enable bit
 1 = Master mode
 0 = Slave mode

- Note 1:** The CKE bit is not used in Framed SPI modes. Program this bit to '0' for Framed SPI modes (FRMEN = 1).
Note 2: This bit must be cleared when FRMEN = 1.
Note 3: Do not set both primary and secondary prescalers to the value of 1:1.

REGISTER 19-1: I2CxCON: I2Cx CONTROL REGISTER (CONTINUED)

- bit 6 **STREN:** SCLx Clock Stretch Enable bit (when operating as I²C slave)
Used in conjunction with the SCLREL bit.
1 = Enables software or receives clock stretching
0 = Disables software or receives clock stretching
- bit 5 **ACKDT:** Acknowledge Data bit (when operating as I²C master, applicable during master receive)
Value that is transmitted when the software initiates an Acknowledge sequence.
1 = Sends NACK during Acknowledge
0 = Sends ACK during Acknowledge
- bit 4 **ACKEN:** Acknowledge Sequence Enable bit
(when operating as I²C master, applicable during master receive)
1 = Initiates Acknowledge sequence on SDAx and SCLx pins and transmits ACKDT data bit. Hardware is clear at the end of the master Acknowledge sequence.
0 = Acknowledge sequence is not in progress
- bit 3 **RCEN:** Receive Enable bit (when operating as I²C master)
1 = Enables Receive mode for I²C. Hardware is clear at the end of the eighth bit of the master receive data byte.
0 = Receive sequence is not in progress
- bit 2 **PEN:** Stop Condition Enable bit (when operating as I²C master)
1 = Initiates Stop condition on SDAx and SCLx pins. Hardware is clear at the end of the master Stop sequence.
0 = Stop condition is not in progress
- bit 1 **RSEN:** Repeated Start Condition Enable bit (when operating as I²C master)
1 = Initiates Repeated Start condition on SDAx and SCLx pins. Hardware is clear at the end of the master Repeated Start sequence.
0 = Repeated Start condition is not in progress
- bit 0 **SEN:** Start Condition Enable bit (when operating as I²C master)
1 = Initiates Start condition on SDAx and SCLx pins. Hardware is clear at the end of the master Start sequence.
0 = Start condition is not in progress

Note 1: When performing master operations, ensure that the IPMIEN bit is set to '0'.

REGISTER 20-1: UxMODE: UARTx MODE REGISTER (CONTINUED)

- bit 5 **ABAUD:** Auto-Baud Enable bit
1 = Enables baud rate measurement on the next character – requires reception of a Sync field (55h) before other data; cleared in hardware upon completion
0 = Baud rate measurement is disabled or completed
- bit 4 **URXINV:** UARTx Receive Polarity Inversion bit
1 = UxRX Idle state is '0'
0 = UxRX Idle state is '1'
- bit 3 **BRGH:** High Baud Rate Enable bit
1 = BRG generates 4 clocks per bit period (4x baud clock, High-Speed mode)
0 = BRG generates 16 clocks per bit period (16x baud clock, Standard mode)
- bit 2-1 **PDSEL<1:0>:** Parity and Data Selection bits
11 = 9-bit data, no parity
10 = 8-bit data, odd parity
01 = 8-bit data, even parity
00 = 8-bit data, no parity
- bit 0 **STSEL:** Stop Bit Selection bit
1 = Two Stop bits
0 = One Stop bit

- Note 1:** Refer to the “**UART**” (DS70582) section in the “*dsPIC33/PIC24 Family Reference Manual*” for information on enabling the UARTx module for receive or transmit operation.
- 2:** This feature is only available for the 16x BRG mode (BRGH = 0).
- 3:** This feature is only available on 44-pin and 64-pin devices.
- 4:** This feature is only available on 64-pin devices.

REGISTER 21-11: CxFEN1: ECANx ACCEPTANCE FILTER ENABLE REGISTER 1

R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1
FLTEN15	FLTEN14	FLTEN13	FLTEN12	FLTEN11	FLTEN10	FLTEN9	FLTEN8
bit 15							bit 8

R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1
FLTEN7	FLTEN6	FLTEN5	FLTEN4	FLTEN3	FLTEN2	FLTEN1	FLTEN0
bit 7							bit 0

Legend:

R = Readable bit W = Writable bit U = Unimplemented bit, read as '0'
-n = Value at POR '1' = Bit is set '0' = Bit is cleared x = Bit is unknown

bit 15-0 **FLTEN<15:0>**: Enable Filter n to Accept Messages bits
1 = Enables Filter n
0 = Disables Filter n

REGISTER 21-12: CxBUFNT1: ECANx FILTER 0-3 BUFFER POINTER REGISTER 1

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
F3BP<3:0>				F2BP<3:0>			
bit 15							bit 8

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
F1BP<3:0>				F0BP<3:0>			
bit 7							bit 0

Legend:

R = Readable bit W = Writable bit U = Unimplemented bit, read as '0'
-n = Value at POR '1' = Bit is set '0' = Bit is cleared x = Bit is unknown

bit 15-12 **F3BP<3:0>**: RX Buffer Mask for Filter 3 bits
1111 = Filter hits received in RX FIFO buffer
1110 = Filter hits received in RX Buffer 14
.
.
.
0001 = Filter hits received in RX Buffer 1
0000 = Filter hits received in RX Buffer 0

bit 11-8 **F2BP<3:0>**: RX Buffer Mask for Filter 2 bits (same values as bits<15:12>)

bit 7-4 **F1BP<3:0>**: RX Buffer Mask for Filter 1 bits (same values as bits<15:12>)

bit 3-0 **F0BP<3:0>**: RX Buffer Mask for Filter 0 bits (same values as bits<15:12>)

REGISTER 24-4: PTGT0LIM: PTG TIMER0 LIMIT REGISTER⁽¹⁾

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
PTGT0LIM<15:8>							
bit 15				bit 8			

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
PTGT0LIM<7:0>							
bit 7				bit 0			

Legend:

R = Readable bit

W = Writable bit

U = Unimplemented bit, read as '0'

-n = Value at POR

'1' = Bit is set

'0' = Bit is cleared

x = Bit is unknown

bit 15-0 **PTGT0LIM<15:0>**: PTG Timer0 Limit Register bits
General Purpose Timer0 Limit register (effective only with a PTGT0 Step command).

Note 1: This register is read-only when the PTG module is executing Step commands (PTGEN = 1 and PTGSTRT = 1).

REGISTER 24-5: PTGT1LIM: PTG TIMER1 LIMIT REGISTER⁽¹⁾

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
PTGT1LIM<15:8>							
bit 15				bit 8			

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
PTGT1LIM<7:0>							
bit 7				bit 0			

Legend:

R = Readable bit

W = Writable bit

U = Unimplemented bit, read as '0'

-n = Value at POR

'1' = Bit is set

'0' = Bit is cleared

x = Bit is unknown

bit 15-0 **PTGT1LIM<15:0>**: PTG Timer1 Limit Register bits
General Purpose Timer1 Limit register (effective only with a PTGT1 Step command).

Note 1: This register is read-only when the PTG module is executing Step commands (PTGEN = 1 and PTGSTRT = 1).

REGISTER 25-2: CMxCON: COMPARATOR x CONTROL REGISTER (x = 1, 2 OR 3) (CONTINUED)

- bit 7-6 **EVPOL<1:0>**: Trigger/Event/Interrupt Polarity Select bits
- 11 = Trigger/event/interrupt generated on any change of the comparator output (while CEVT = 0)
 - 10 = Trigger/event/interrupt generated only on high-to-low transition of the polarity selected comparator output (while CEVT = 0)
 - If CPOL = 1 (inverted polarity):
Low-to-high transition of the comparator output.
 - If CPOL = 0 (non-inverted polarity):
High-to-low transition of the comparator output.
 - 01 = Trigger/event/interrupt generated only on low-to-high transition of the polarity-selected comparator output (while CEVT = 0)
 - If CPOL = 1 (inverted polarity):
High-to-low transition of the comparator output.
 - If CPOL = 0 (non-inverted polarity):
Low-to-high transition of the comparator output
 - 00 = Trigger/event/interrupt generation is disabled
- bit 5 **Unimplemented**: Read as '0'
- bit 4 **CREF**: Comparator Reference Select bit (VIN+ input)⁽¹⁾
- 1 = VIN+ input connects to internal CVREFIN voltage⁽²⁾
 - 0 = VIN+ input connects to CxIN1+ pin
- bit 3-2 **Unimplemented**: Read as '0'
- bit 1-0 **CCH<1:0>**: Op Amp/Comparator Channel Select bits⁽¹⁾
- 11 = Unimplemented
 - 10 = Unimplemented
 - 01 = Inverting input of the comparator connects to the CxIN2- pin⁽²⁾
 - 00 = Inverting input of the op amp/comparator connects to the CxIN1- pin

Note 1: Inputs that are selected and not available will be tied to Vss. See the “Pin Diagrams” section for available inputs for each package.

2: This output is not available when OPMODE (CMxCON<10>) = 1.

TABLE 28-2: INSTRUCTION SET OVERVIEW (CONTINUED)

Base Instr #	Assembly Mnemonic	Assembly Syntax	Description	# of Words	# of Cycles ⁽²⁾	Status Flags Affected
46	MOV	MOV <i>f</i> , <i>Wn</i>	Move <i>f</i> to <i>Wn</i>	1	1	None
		MOV <i>f</i>	Move <i>f</i> to <i>f</i>	1	1	None
		MOV <i>f</i> , WREG	Move <i>f</i> to WREG	1	1	None
		MOV #lit16, <i>Wn</i>	Move 16-bit literal to <i>Wn</i>	1	1	None
		MOV.b #lit8, <i>Wn</i>	Move 8-bit literal to <i>Wn</i>	1	1	None
		MOV <i>Wn</i> , <i>f</i>	Move <i>Wn</i> to <i>f</i>	1	1	None
		MOV <i>Wso</i> , <i>Wdo</i>	Move <i>Ws</i> to <i>Wd</i>	1	1	None
		MOV WREG, <i>f</i>	Move WREG to <i>f</i>	1	1	None
		MOV.D <i>Wns</i> , <i>Wd</i>	Move Double from <i>W(ns):W(ns + 1)</i> to <i>Wd</i>	1	2	None
		MOV.D <i>Ws</i> , <i>Wnd</i>	Move Double from <i>Ws</i> to <i>W(nd + 1):W(nd)</i>	1	2	None
47	MOVPG	MOVPG #lit10, DSRPAG	Move 10-bit literal to DSRPAG	1	1	None
		MOVPG #lit9, DSWPAG	Move 9-bit literal to DSWPAG	1	1	None
		MOVPG #lit8, TBLPAG	Move 8-bit literal to TBLPAG	1	1	None
		MOVPG <i>Ws</i> , DSRPAG	Move <i>Ws</i> <9:0> to DSRPAG	1	1	None
		MOVPG <i>Ws</i> , DSWPAG	Move <i>Ws</i> <8:0> to DSWPAG	1	1	None
		MOVPG <i>Ws</i> , TBLPAG	Move <i>Ws</i> <7:0> to TBLPAG	1	1	None
48	MOVSAC	MOVSAC <i>Acc</i> , <i>Wx</i> , <i>Wxd</i> , <i>Wy</i> , <i>Wyd</i> , AWB ⁽¹⁾	Prefetch and store accumulator	1	1	None
49	MPY	MPY <i>Wm</i> * <i>Wn</i> , <i>Acc</i> , <i>Wx</i> , <i>Wxd</i> , <i>Wy</i> , <i>Wyd</i> ⁽¹⁾	Multiply <i>Wm</i> by <i>Wn</i> to Accumulator	1	1	OA,OB,OAB,SA,SB,SAB
		MPY <i>Wm</i> * <i>Wm</i> , <i>Acc</i> , <i>Wx</i> , <i>Wxd</i> , <i>Wy</i> , <i>Wyd</i> ⁽¹⁾	Square <i>Wm</i> to Accumulator	1	1	OA,OB,OAB,SA,SB,SAB
50	MPY.N	MPY.N <i>Wm</i> * <i>Wn</i> , <i>Acc</i> , <i>Wx</i> , <i>Wxd</i> , <i>Wy</i> , <i>Wyd</i> ⁽¹⁾	-(Multiply <i>Wm</i> by <i>Wn</i>) to Accumulator	1	1	None
51	MSC	MSC <i>Wm</i> * <i>Wm</i> , <i>Acc</i> , <i>Wx</i> , <i>Wxd</i> , <i>Wy</i> , <i>Wyd</i> , AWB ⁽¹⁾	Multiply and Subtract from Accumulator	1	1	OA,OB,OAB,SA,SB,SAB

Note 1: These instructions are available in dsPIC33EPXXXMC20X/50X and PIC24EPXXXMC20X devices only.

2: Read and Read-Modify-Write (e.g., bit operations and logical operations) on non-CPU SFRs incur an additional instruction cycle.

TABLE 30-49: I2Cx BUS DATA TIMING REQUIREMENTS (MASTER MODE)

AC CHARACTERISTICS				Standard Operating Conditions: 3.0V to 3.6V (unless otherwise stated) Operating temperature $-40^{\circ}\text{C} \leq T_A \leq +85^{\circ}\text{C}$ for Industrial $-40^{\circ}\text{C} \leq T_A \leq +125^{\circ}\text{C}$ for Extended			
Param No.	Symbol	Characteristic ⁽⁴⁾		Min. ⁽¹⁾	Max.	Units	Conditions
IM10	TLO:SCL	Clock Low Time	100 kHz mode	$T_{CY}/2$ (BRG + 2)	—	μs	
			400 kHz mode	$T_{CY}/2$ (BRG + 2)	—	μs	
			1 MHz mode ⁽²⁾	$T_{CY}/2$ (BRG + 2)	—	μs	
IM11	THI:SCL	Clock High Time	100 kHz mode	$T_{CY}/2$ (BRG + 2)	—	μs	
			400 kHz mode	$T_{CY}/2$ (BRG + 2)	—	μs	
			1 MHz mode ⁽²⁾	$T_{CY}/2$ (BRG + 2)	—	μs	
IM20	TF:SCL	SDAx and SCLx Fall Time	100 kHz mode	—	300	ns	Cb is specified to be from 10 to 400 pF
			400 kHz mode	$20 + 0.1 C_b$	300	ns	
			1 MHz mode ⁽²⁾	—	100	ns	
IM21	TR:SCL	SDAx and SCLx Rise Time	100 kHz mode	—	1000	ns	Cb is specified to be from 10 to 400 pF
			400 kHz mode	$20 + 0.1 C_b$	300	ns	
			1 MHz mode ⁽²⁾	—	300	ns	
IM25	TSU:DAT	Data Input Setup Time	100 kHz mode	250	—	ns	
			400 kHz mode	100	—	ns	
			1 MHz mode ⁽²⁾	40	—	ns	
IM26	THD:DAT	Data Input Hold Time	100 kHz mode	0	—	μs	
			400 kHz mode	0	0.9	μs	
			1 MHz mode ⁽²⁾	0.2	—	μs	
IM30	TSU:STA	Start Condition Setup Time	100 kHz mode	$T_{CY}/2$ (BRG + 2)	—	μs	Only relevant for Repeated Start condition
			400 kHz mode	$T_{CY}/2$ (BRG + 2)	—	μs	
			1 MHz mode ⁽²⁾	$T_{CY}/2$ (BRG + 2)	—	μs	
IM31	THD:STA	Start Condition Hold Time	100 kHz mode	$T_{CY}/2$ (BRG + 2)	—	μs	After this period, the first clock pulse is generated
			400 kHz mode	$T_{CY}/2$ (BRG + 2)	—	μs	
			1 MHz mode ⁽²⁾	$T_{CY}/2$ (BRG + 2)	—	μs	
IM33	TSU:STO	Stop Condition Setup Time	100 kHz mode	$T_{CY}/2$ (BRG + 2)	—	μs	
			400 kHz mode	$T_{CY}/2$ (BRG + 2)	—	μs	
			1 MHz mode ⁽²⁾	$T_{CY}/2$ (BRG + 2)	—	μs	
IM34	THD:STO	Stop Condition Hold Time	100 kHz mode	$T_{CY}/2$ (BRG + 2)	—	μs	
			400 kHz mode	$T_{CY}/2$ (BRG + 2)	—	μs	
			1 MHz mode ⁽²⁾	$T_{CY}/2$ (BRG + 2)	—	μs	
IM40	TAA:SCL	Output Valid From Clock	100 kHz mode	—	3500	ns	
			400 kHz mode	—	1000	ns	
			1 MHz mode ⁽²⁾	—	400	ns	
IM45	TBF:SDA	Bus Free Time	100 kHz mode	4.7	—	μs	Time the bus must be free before a new transmission can start
			400 kHz mode	1.3	—	μs	
			1 MHz mode ⁽²⁾	0.5	—	μs	
IM50	CB	Bus Capacitive Loading		—	400	pF	
IM51	TPGD	Pulse Gobbler Delay		65	390	ns	(Note 3)

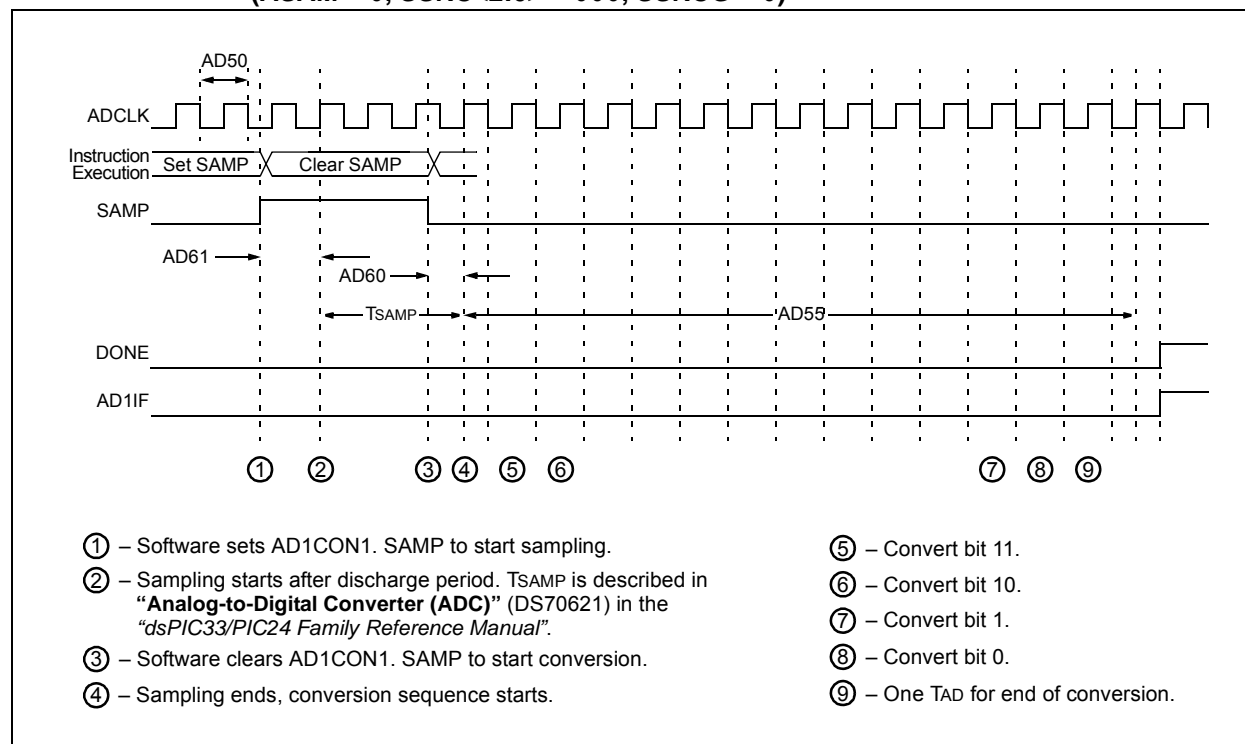
Note 1: BRG is the value of the I²C™ Baud Rate Generator. Refer to “Inter-Integrated Circuit (I²C™)” (DS70330) in the “dsPIC33/PIC24 Family Reference Manual”. Please see the Microchip web site for the latest family reference manual sections.

2: Maximum pin capacitance = 10 pF for all I2Cx pins (for 1 MHz mode only).

3: Typical value for this parameter is 130 ns.

4: These parameters are characterized, but not tested in manufacturing.

FIGURE 30-36: ADC CONVERSION (12-BIT MODE) TIMING CHARACTERISTICS
(ASAM = 0, SSRC<2:0> = 000, SSRCG = 0)



Revision F (November 2012)

Removed “Preliminary” from data sheet footer.

Revision G (March 2013)

This revision includes the following global changes:

- changes “ $\overline{\text{FLT}}\text{x}$ ” pin function to “FLT_x” on all occurrences
- adds **Section 31.0 “High-Temperature Electrical Characteristics”** for high-temperature (+150°C) data

This revision also includes minor typographical and formatting changes throughout the text.

Other major changes are referenced by their respective section in Table A-5.

TABLE A-5: MAJOR SECTION UPDATES

Section Name	Update Description
Cover Section	<ul style="list-style-type: none"> • Changes internal oscillator specification to 1.0% • Changes I/O sink/source values to 12 mA or 6 mA • Corrects 44-pin VTLA pin diagram (pin 32 now shows as 5V tolerant)
Section 4.0 “Memory Organization”	<ul style="list-style-type: none"> • Deletes references to Configuration Shadow registers • Corrects the spelling of the JTAGIP and PTGWDTIP bits throughout • Corrects the Reset value of all IOCON registers as C000h • Adds footnote to Table 4-42 to indicate the absence of Comparator 3 in 28-pin devices
Section 6.0 “Resets”	<ul style="list-style-type: none"> • Removes references to cold and warm Resets, and clarifies the initial configuration of the device clock source on all Resets
Section 7.0 “Interrupt Controller”	<ul style="list-style-type: none"> • Corrects the definition of GIE as “Global Interrupt Enable” (not “General”)
Section 9.0 “Oscillator Configuration”	<ul style="list-style-type: none"> • Clarifies the behavior of the CF bit when cleared in software • Removes POR behavior footnotes from all control registers • Corrects the tuning range of the TUN<5:0> bits in Register 9-4 to an overall range $\pm 1.5\%$
Section 13.0 “Timer2/3 and Timer4/5”	<ul style="list-style-type: none"> • Clarifies the presence of the ADC Trigger in 16-bit Timer3 and Timer5, as well as the 32-bit timers
Section 15.0 “Output Compare”	<ul style="list-style-type: none"> • Corrects the first trigger source for SYNCSEL<4:0> (OCxCON2<4:0>) as OCxRS match
Section 16.0 “High-Speed PWM Module”	<ul style="list-style-type: none"> • Clarifies the source of the PWM interrupts in Figure 16-1 • Corrects the Reset states of IOCONx<15:14> in Register 16-13 as ‘11’
Section 17.0 “Quadrature Encoder Interface (QEI) Module”	<ul style="list-style-type: none"> • Clarifies the operation of the IMV<1:0> bits (QEICON<9:8>) with updated text and additional notes • Corrects the first prescaler value for QFVDIV<2:0> (QE1IOC<13:11>), now 1:128
Section 23.0 “10-Bit/12-Bit Analog-to-Digital Converter (ADC)”	<ul style="list-style-type: none"> • Adds note to Figure 23-1 that Op Amp 3 is not available in 28-pin devices • Changes “sample clock” to “sample trigger” in AD1CON1 (Register 23-1) • Clarifies footnotes on op amp usage in Registers 23-5 and 23-6
Section 25.0 “Op Amp/Comparator Module”	<ul style="list-style-type: none"> • Adds Note text to indicate that Comparator 3 is unavailable in 28-pin devices • Splits Figure 25-1 into two figures for clearer presentation (Figure 25-1 for Op amp/Comparators 1 through 3, Figure 25-2 for Comparator 4). Subsequent figures are renumbered accordingly. • Corrects reference description in xxxxx (now (AVDD+AVSS)/2) • Changes CMSTAT<15> in Register 25-1 to “PSIDL”
Section 27.0 “Special Features”	<ul style="list-style-type: none"> • Corrects the addresses of all Configuration bytes for 512 Kbyte devices

NOTES: