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#### What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

## Applications of "<u>Embedded -</u> <u>Microcontrollers</u>"

#### Details

E·XFI

Product Status	Active
Core Processor	PIC
Core Size	16-Bit
Speed	70 MIPs
Connectivity	I <sup>2</sup> C, IrDA, LINbus, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, DMA, POR, PWM, WDT
Number of I/O	53
Program Memory Size	128KB (43K x 24)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	8K x 16
Voltage - Supply (Vcc/Vdd)	3V ~ 3.6V
Data Converters	A/D 16x10b/12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	64-VFQFN Exposed Pad
Supplier Device Package	64-VQFN (9x9)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/pic24ep128gp206t-i-mr

Email: info@E-XFL.COM

Address: Room A, 16/F, Full Win Commercial Centre, 573 Nathan Road, Mongkok, Hong Kong

#### FIGURE 4-2: PROGRAM MEMORY MAP FOR dsPIC33EP64GP50X, dsPIC33EP64MC20X/50X AND PIC24EP64GP/MC20X DEVICES



Note: Memory areas are not shown to scale.

## TABLE 4-20: ADC1 REGISTER MAP

File Name	Addr.	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	All Resets
ADC1BUF0	0300		ADC1 Data Buffer 0 xx:									xxxx						
ADC1BUF1	0302								ADC1 Data B	uffer 1								xxxx
ADC1BUF2	0304								ADC1 Data B	uffer 2								xxxx
ADC1BUF3	0306								ADC1 Data B	uffer 3								xxxx
ADC1BUF4	0308								ADC1 Data B	uffer 4								xxxx
ADC1BUF5	030A								ADC1 Data B	uffer 5								xxxx
ADC1BUF6	030C								ADC1 Data B	uffer 6								xxxx
ADC1BUF7	030E								ADC1 Data B	uffer 7								xxxx
ADC1BUF8	0310								ADC1 Data B	uffer 8								xxxx
ADC1BUF9	0312								ADC1 Data B	uffer 9								xxxx
ADC1BUFA	0314								ADC1 Data Bu	uffer 10								xxxx
ADC1BUFB	0316								ADC1 Data Bu	uffer 11								xxxx
ADC1BUFC	0318								ADC1 Data Bu	uffer 12								xxxx
ADC1BUFD	031A								ADC1 Data Bu	uffer 13								xxxx
ADC1BUFE	031C								ADC1 Data Bu	uffer 14								xxxx
ADC1BUFF	031E								ADC1 Data Bu	uffer 15								xxxx
AD1CON1	0320	ADON	—	ADSIDL	ADDMABM	_	AD12B	FOR	M<1:0>		SSRC<2:0	>	SSRCG	SIMSAM	ASAM	SAMP	DONE	0000
AD1CON2	0322	,	VCFG<2:0	>	—		CSCNA	CHP	S<1:0>	BUFS			SMPI<4:0>	>		BUFM	ALTS	0000
AD1CON3	0324	ADRC	—	—		-	SAMC<4:0	>	_		-		ADCS	<7:0>				0000
AD1CHS123	0326	_	—	—	—		CH123N	NB<1:0>	CH123SB	—	—		—	—	CH123N	A<1:0>	CH123SA	0000
AD1CHS0	0328	CH0NB	—	—		-	CH0SB<4:0	>	_	CH0NA	—			C	H0SA<4:0	>		0000
AD1CSSH	032E	CSS31	CSS30	—	—		CSS26	CSS25	CSS24	—			—	—	—	—	—	0000
AD1CSSL	0330	CSS15	CSS14	CSS13	CSS12	CSS11	CSS10	CSS9	CSS8	CSS7	CSS6	CSS5	CSS4	CSS3	CSS2	CSS1	CSS0	0000
AD1CON4	0332	_	-	-	-	—	—	_	ADDMAEN	—	—	—	—	—	D	MABL<2:	0>	0000

Legend: x = unknown value on Reset, - = unimplemented, read as '0'. Reset values are shown in hexadecimal.



## EXAMPLE 4-3: PAGED DATA MEMORY SPACE

dsPIC33EPXXXGP50X, dsPIC33EPXXXMC20X/50X AND PIC24EPXXXGP/MC20X

## 4.5 Instruction Addressing Modes

The addressing modes shown in Table 4-63 form the basis of the addressing modes optimized to support the specific features of individual instructions. The addressing modes provided in the MAC class of instructions differ from those in the other instruction types.

## 4.5.1 FILE REGISTER INSTRUCTIONS

Most file register instructions use a 13-bit address field (f) to directly address data present in the first 8192 bytes of data memory (Near Data Space). Most file register instructions employ a working register, W0, which is denoted as WREG in these instructions. The destination is typically either the same file register or WREG (with the exception of the MUL instruction), which writes the result to a register or register pair. The MOV instruction allows additional flexibility and can access the entire Data Space.

## 4.5.2 MCU INSTRUCTIONS

The three-operand MCU instructions are of the form:

Operand 3 = Operand 1 <function> Operand 2

where Operand 1 is always a working register (that is, the addressing mode can only be Register Direct), which is referred to as Wb. Operand 2 can be a W register fetched from data memory or a 5-bit literal. The result location can either be a W register or a data memory location. The following addressing modes are supported by MCU instructions:

- Register Direct
- · Register Indirect
- · Register Indirect Post-Modified
- Register Indirect Pre-Modified
- 5-Bit or 10-Bit Literal
- Note: Not all instructions support all the addressing modes given above. Individual instructions can support different subsets of these addressing modes.

## TABLE 4-63: FUNDAMENTAL ADDRESSING MODES SUPPORTED

Addressing Mode	Description
File Register Direct	The address of the file register is specified explicitly.
Register Direct	The contents of a register are accessed directly.
Register Indirect	The contents of Wn form the Effective Address (EA).
Register Indirect Post-Modified	The contents of Wn form the EA. Wn is post-modified (incremented or decremented) by a constant value.
Register Indirect Pre-Modified	Wn is pre-modified (incremented or decremented) by a signed constant value to form the EA.
Register Indirect with Register Offset (Register Indexed)	The sum of Wn and Wb forms the EA.
Register Indirect with Literal Offset	The sum of Wn and a literal forms the EA.

## 5.0 FLASH PROGRAM MEMORY

- Note 1: This data sheet summarizes the features of the dsPIC33EPXXXGP50X, dsPIC33EPXXXGP/MC20X/50X and PIC24EPXXXGP/MC20X families of devices. It is not intended to be a comprehensive reference source. To complement the information in this data sheet, refer to "Flash Programming" (DS70609) in the "dsPIC33/PIC24 Family Reference Manual", which is available from the Microchip web site (www.microchip.com).
  - 2: Some registers and associated bits described in this section may not be available on all devices. Refer to Section 4.0 "Memory Organization" in this data sheet for device-specific register and bit information.

The dsPIC33EPXXXGP50X, dsPIC33EPXXXMC20X/ 50X and PIC24EPXXXGP/MC20X devices contain internal Flash program memory for storing and executing application code. The memory is readable, writable and erasable during normal operation over the entire VDD range.

Flash memory can be programmed in two ways:

- In-Circuit Serial Programming™ (ICSP™) programming capability
- Run-Time Self-Programming (RTSP)

ICSP allows for a dsPIC33EPXXXGP50X, dsPIC33EPXXXMC20X/50X and PIC24EPXXXGP/ MC20X device to be serially programmed while in the end application circuit. This is done with two lines for programming clock and programming data (one of the alternate programming pin pairs: PGECx/PGEDx), and three other lines for power (VDD), ground (VSS) and Master Clear (MCLR). This allows customers to manufacture boards with unprogrammed devices and then program the device just before shipping the product. This also allows the most recent firmware or a custom firmware to be programmed.

RTSP is accomplished using TBLRD (Table Read) and TBLWT (Table Write) instructions. With RTSP, the user application can write program memory data a single program memory word, and erase program memory in blocks or 'pages' of 1024 instructions (3072 bytes) at a time.

## 5.1 Table Instructions and Flash Programming

Regardless of the method used, all programming of Flash memory is done with the Table Read and Table Write instructions. These allow direct read and write access to the program memory space from the data memory while the device is in normal operating mode. The 24-bit target address in the program memory is formed using bits<7:0> of the TBLPAG register and the Effective Address (EA) from a W register, specified in the table instruction, as shown in Figure 5-1.

The TBLRDL and the TBLWTL instructions are used to read or write to bits<15:0> of program memory. TBLRDL and TBLWTL can access program memory in both Word and Byte modes.

The TBLRDH and TBLWTH instructions are used to read or write to bits<23:16> of program memory. TBLRDH and TBLWTH can also access program memory in Word or Byte mode.

## FIGURE 5-1: ADDRESSING FOR TABLE REGISTERS



## **10.0 POWER-SAVING FEATURES**

- Note 1: This data sheet summarizes the features of the dsPIC33EPXXXGP50X, dsPIC33EPXXXMC20X/50X and PIC24EPXXXGP/MC20X families of devices. It is not intended to be a comprehensive reference source. To complement the information in this data sheet, refer to "Watchdog Timer and Power-Saving Modes" (DS70615) in the "dsPIC33/ PIC24 Family Reference Manual", which is available from the Microchip web site (www.microchip.com).
  - Some registers and associated bits described in this section may not be available on all devices. Refer to Section 4.0 "Memory Organization" in this data sheet for device-specific register and bit information.

The dsPIC33EPXXXGP50X, dsPIC33EPXXXMC20X/ 50X and PIC24EPXXXGP/MC20X devices provide the ability to manage power consumption by selectively managing clocking to the CPU and the peripherals. In general, a lower clock frequency and a reduction in the number of peripherals being clocked constitutes lower consumed power.

dsPIC33EPXXXGP50X, dsPIC33EPXXXMC20X/50X and PIC24EPXXXGP/MC20X devices can manage power consumption in four ways:

- Clock Frequency
- Instruction-Based Sleep and Idle modes
- Software-Controlled Doze mode
- · Selective Peripheral Control in Software

Combinations of these methods can be used to selectively tailor an application's power consumption while still maintaining critical application features, such as timing-sensitive communications.

## EXAMPLE 10-1: PWRSAV INSTRUCTION SYNTAX

PWRSAV	#SLEEP_MODE	;	Put	the	device	into	Sleep mode
PWRSAV	#IDLE_MODE	;	Put	the	device	into	Idle mode

## 10.1 Clock Frequency and Clock Switching

The dsPIC33EPXXXGP50X, dsPIC33EPXXXMC20X/ 50X and PIC24EPXXXGP/MC20X devices allow a wide range of clock frequencies to be selected under application control. If the system clock configuration is not locked, users can choose low-power or highprecision oscillators by simply changing the NOSCx bits (OSCCON<10:8>). The process of changing a system clock during operation, as well as limitations to the process, are discussed in more detail in **Section 9.0 "Oscillator Configuration"**.

## 10.2 Instruction-Based Power-Saving Modes

The dsPIC33EPXXXGP50X, dsPIC33EPXXXMC20X/ 50X and PIC24EPXXXGP/MC20X devices have two special power-saving modes that are entered through the execution of a special PWRSAV instruction. Sleep mode stops clock operation and halts all code execution. Idle mode halts the CPU and code execution, but allows peripheral modules to continue operation. The assembler syntax of the PWRSAV instruction is shown in Example 10-1.

**Note:** SLEEP\_MODE and IDLE\_MODE are constants defined in the assembler include file for the selected device.

Sleep and Idle modes can be exited as a result of an enabled interrupt, WDT time-out or a device Reset. When the device exits these modes, it is said to "wake-up".

## REGISTER 10-1: PMD1: PERIPHERAL MODULE DISABLE CONTROL REGISTER 1 (CONTINUED)

- bit 3 SPI1MD: SPI1 Module Disable bit 1 = SPI1 module is disabled
  - 0 = SPI1 module is enabled
- bit 2 Unimplemented: Read as '0'
- bit 1 C1MD: ECAN1 Module Disable bit<sup>(2)</sup> 1 = ECAN1 module is disabled 0 = ECAN1 module is enabled
- bit 0 AD1MD: ADC1 Module Disable bit 1 = ADC1 module is disabled 0 = ADC1 module is enabled
- Note 1: This bit is available on dsPIC33EPXXXMC20X/50X and PIC24EPXXXMC20X devices only.
  - 2: This bit is available on dsPIC33EPXXXGP50X and dsPIC33EPXXXMC50X devices only.

U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	_	_	—	_	_	_	—
bit 15		L	I	4			bit 8
U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
—				INT2R<6:0>			
bit 7							bit 0
Legend:							
R = Readable	bit	W = Writable	bit	U = Unimpler	mented bit, read	l as '0'	
-n = Value at POR							
-n = Value at F	POR	'1' = Bit is set		'0' = Bit is cle	ared	x = Bit is unkr	nown
-n = Value at F	POR	'1' = Bit is set		'0' = Bit is cle	ared	x = Bit is unkr	iown
-n = Value at F bit 15-7	POR Unimplemen	<pre>'1' = Bit is set ted: Read as '0</pre>	0'	ʻ0' = Bit is cle	ared	x = Bit is unkr	iown
-n = Value at F bit 15-7 bit 6-0	Unimplement INT2R<6:0>: (see Table 11-	'1' = Bit is set ted: Read as '0 Assign Externa -2 for input pin	)' al Interrupt 2 ( selection nun	'0' = Bit is cle (INT2) to the C nbers)	orresponding R	x = Bit is unkr Pn Pin bits	iown
-n = Value at F bit 15-7 bit 6-0	POR Unimplement INT2R<6:0>: (see Table 11- 1111001 = In	'1' = Bit is set ted: Read as '0 Assign Externa -2 for input pin uput tied to RPI	o' al Interrupt 2 ( selection nun 121	'0' = Bit is cle (INT2) to the C nbers)	ared	x = Bit is unkr Pn Pin bits	iown
-n = Value at F bit 15-7 bit 6-0	OR Unimplemen INT2R<6:0>: (see Table 11- 1111001 = In	'1' = Bit is set ted: Read as '( Assign Externa -2 for input pin put tied to RPI	o' al Interrupt 2 ( selection nun 121	'0' = Bit is cle (INT2) to the C nbers)	orresponding R	x = Bit is unkr Pn Pin bits	iown
-n = Value at F bit 15-7 bit 6-0	POR Unimplement INT2R<6:0>: (see Table 11- 1111001 = In	'1' = Bit is set ted: Read as '0 Assign Externa 2 for input pin uput tied to RPI	o' al Interrupt 2 ( selection nun 121	'0' = Bit is cle (INT2) to the C nbers)	orresponding R	x = Bit is unkr Pn Pin bits	iown
-n = Value at F bit 15-7 bit 6-0	POR Unimplement INT2R<6:0>: (see Table 11- 1111001 = In	'1' = Bit is set ted: Read as '0 Assign Externa 2 for input pin put tied to RPI	o' al Interrupt 2 ( selection nun 121 P1	'0' = Bit is cle (INT2) to the C nbers)	orresponding R	x = Bit is unkr Pn Pin bits	iown
-n = Value at F bit 15-7 bit 6-0	Unimplement INT2R<6:0>: (see Table 11- 1111001 = In 0000001 = In 0000000 = In	'1' = Bit is set ted: Read as '0 Assign Externa 2 for input pin put tied to RPI put tied to CMI put tied to Vss	o' al Interrupt 2 ( selection nun 121 P1	'0' = Bit is cle (INT2) to the C nbers)	orresponding R	x = Bit is unkr	iown

## REGISTER 11-2: RPINR1: PERIPHERAL PIN SELECT INPUT REGISTER 1

## REGISTER 11-3: RPINR3: PERIPHERAL PIN SELECT INPUT REGISTER 3

U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
—	_		_				_
bit 15							bit 8
U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
—				T2CKR<6:0>			
bit 7							bit 0
Legend:							
R = Readabl	le bit	W = Writable I	bit	U = Unimplem	nented bit, read	as '0'	
-n = Value at	t POR	'1' = Bit is set		'0' = Bit is clea	ared	x = Bit is unkn	own
bit 15-7	Unimplemen	ted: Read as 'o	)'				
bit 15-7 bit 6-0	Unimplemen T2CKR<6:0> (see Table 11	ted: Read as '( : Assign Timer2 -2 for input pin	)' 2 External Clo selection nur	ock (T2CK) to th nbers)	e Correspondi	ng RPn pin bits	
bit 15-7 bit 6-0	Unimplemen T2CKR<6:0> (see Table 11 1111001 = Ir	ted: Read as '( : Assign Timer2 -2 for input pin nput tied to RPI	) <sup>;</sup> 2 External Clo selection nur 121	ock (T2CK) to th nbers)	ie Correspondii	ng RPn pin bits	
bit 15-7 bit 6-0	Unimplemen T2CKR<6:0> (see Table 11 1111001 = Ir	ted: Read as '( : Assign Timer2 -2 for input pin nput tied to RPI	) <sup>;</sup> 2 External Clo selection nur 121	ock (T2CK) to th nbers)	e Correspondi	ng RPn pin bits	
bit 15-7 bit 6-0	Unimplemen T2CKR<6:0> (see Table 11 1111001 = Ir	ted: Read as ' : Assign Timer2 -2 for input pin nput tied to RPI	)' 2 External Cle selection nur 121	ock (T2CK) to th nbers)	e Correspondi	ng RPn pin bits	
bit 15-7 bit 6-0	Unimplemen T2CKR<6:0> (see Table 11 1111001 = Ir	ted: Read as 'c : Assign Timer2 -2 for input pin nput tied to RPI	)' 2 External Clo selection nur 121 P1	ock (T2CK) to th nbers)	le Correspondi	ng RPn pin bits	
bit 15-7 bit 6-0	Unimplemen T2CKR<6:0> (see Table 11 1111001 = Ir 0000001 = Ir 0000000 = Ir	ted: Read as '( : Assign Timer2 -2 for input pin nput tied to RPI nput tied to CMI nput tied to Vss	)' 2 External Clo selection nur 121 P1	ock (T2CK) to th nbers)	e Correspondi	ng RPn pin bits	

## 14.2 Input Capture Registers

## REGISTER 14-1: ICxCON1: INPUT CAPTURE x CONTROL REGISTER 1

U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	U-0	U-0
—	—	ICSIDL	ICTSEL2	ICTSEL1	ICTSEL0	_	—
bit 15							bit 8

U-0	R/W-0	R/W-0	R/HC/HS-0	R/HC/HS-0	R/W-0	R/W-0	R/W-0
—	ICI1	ICI0	ICOV	ICBNE	ICM2	ICM1	ICM0
bit 7							bit 0

Legend:	HC = Hardware Clearable bit	HS = Hardware Settable bit	
R = Readable bit	W = Writable bit	U = Unimplemented bit, rea	d as '0'
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15-14	Unimplemented: Read as '0'
bit 13	ICSIDL: Input Capture Stop in Idle Control bit
	1 = Input capture will Halt in CPU Idle mode
	0 = Input capture will continue to operate in CPU Idle mode
bit 12-10	ICTSEL<2:0>: Input Capture Timer Select bits
	111 = Peripheral clock (FP) is the clock source of the ICx
	110 = Reserved
	101 = Reserved
	100 - 11 CLR is the clock source of the ICx (only the synchronous clock is supported) 011 = T5CLK is the clock source of the ICx
	010 = T4CLK is the clock source of the ICx
	001 = T2CLK is the clock source of the ICx
	000 = T3CLK is the clock source of the ICx
bit 9-7	Unimplemented: Read as '0'
bit 6-5	ICI<1:0>: Number of Captures per Interrupt Select bits (this field is not used if ICM<2:0> = 001 or 111)
	11 = Interrupt on every fourth capture event
	10 = Interrupt on every third capture event
	01 = Interrupt on every second capture event
hit 4	ICOV: Input Capture Overflow Status Flag bit (read-only)
Dit 4	1 = Input capture buffer overflow occurred
	0 = No input capture buffer overflow occurred
bit 3	ICBNE: Input Capture Buffer Not Empty Status bit (read-only)
	1 = Input capture buffer is not empty, at least one more capture value can be read
	0 = Input capture buffer is empty
bit 2-0	ICM<2:0>: Input Capture Mode Select bits
	111 = Input capture functions as interrupt pin only in CPU Sleep and Idle modes (rising edge detect only, all other control bits are not applicable)
	110 = Unused (module is disabled)
	101 = Capture mode, every 16th rising edge (Prescaler Capture mode)
	100 = Capture mode, every 4th rising edge (Prescaler Capture mode)
	011 = Capture mode, every falling edge (Simple Capture mode)
	001 = Capture mode, every edge rising and falling (Edge Detect mode (ICI<1:0>) is not used in this mode)
	000 = Input capture module is turned off

## 24.2 PTG Resources

Many useful resources are provided on the main product page of the Microchip web site for the devices listed in this data sheet. This product page, which can be accessed using this link, contains the latest updates and additional information.

Note:	In the event you are not able to access the
	product page using the link above, enter
	this URL in your browser:
	http://www.microchip.com/wwwproducts/
	Devices.aspx?dDocName=en555464

## 24.2.1 KEY RESOURCES

- "Peripheral Trigger Generator" (DS70669) in the "dsPIC33/PIC24 Family Reference Manual"
- Code Samples
- Application Notes
- · Software Libraries
- Webinars
- All Related "dsPIC33/PIC24 Family Reference Manual" Sections
- Development Tools

bit 3-0	Step Command	OPTION<3:0>	Option Description
	PTGCTRL(1)	0000	Reserved.
		0001	Reserved.
		0010	Disable Step Delay Timer (PTGSD).
		0011	Reserved.
		0100	Reserved.
		0101	Reserved.
		0110	Enable Step Delay Timer (PTGSD).
		0111	Reserved.
		1000	Start and wait for the PTG Timer0 to match the Timer0 Limit Register.
		1001	Start and wait for the PTG Timer1 to match the Timer1 Limit Register.
		1010	Reserved.
		1011	Wait for the software trigger bit transition from low-to-high before continuing (PTGSWT = 0 to 1).
		1100	Copy contents of the Counter 0 register to the AD1CHS0 register.
		1101	Copy contents of the Counter 1 register to the AD1CHS0 register.
		1110	Copy contents of the Literal 0 register to the AD1CHS0 register.
		1111	Generate triggers indicated in the Broadcast Trigger Enable register (PTGBTE).
	PTGADD(1)	0000	Add contents of the PTGADJ register to the Counter 0 Limit register (PTGC0LIM).
		0001	Add contents of the PTGADJ register to the Counter 1 Limit register (PTGC1LIM).
		0010	Add contents of the PTGADJ register to the Timer0 Limit register (PTGT0LIM).
		0011	Add contents of the PTGADJ register to the Timer1 Limit register (PTGT1LIM).
		0100	Add contents of the PTGADJ register to the Step Delay Limit register (PTGSDLIM).
		0101	Add contents of the PTGADJ register to the Literal 0 register (PTGL0).
		0110	Reserved.
		0111	Reserved.
	PTGCOPY(1)	1000	Copy contents of the PTGHOLD register to the Counter 0 Limit register (PTGC0LIM).
		1001	Copy contents of the PTGHOLD register to the Counter 1 Limit register (PTGC1LIM).
		1010	Copy contents of the PTGHOLD register to the Timer0 Limit register (PTGT0LIM).
		1011	Copy contents of the PTGHOLD register to the Timer1 Limit register (PTGT1LIM).
		1100	Copy contents of the PTGHOLD register to the Step Delay Limit register (PTGSDLIM).
		1101	Copy contents of the PTGHOLD register to the Literal 0 register (PTGL0).
		1110	Reserved.
		1111	Reserved.

TABLE 24-1: PTG STEP COMMAND FORMAT (CONTINUED)

Note 1: All reserved commands or options will execute but have no effect (i.e., execute as a NOP instruction).

2: Refer to Table 24-2 for the trigger output descriptions.

3: This feature is only available on dsPIC33EPXXXMC20X/50X and PIC24EPXXXMC20X devices.

NOTES:

## **30.1 DC Characteristics**

|--|

			Maximum MIPS		
Characteristic	VDD Range (in Volts)	Temp Range (in °C)	dsPIC33EPXXXGP50X, dsPIC33EPXXXMC20X/50X and PIC24EPXXXGP/MC20X		
	3.0V to 3.6V <sup>(1)</sup>	-40°C to +85°C	70		
—	3.0V to 3.6V <sup>(1)</sup>	-40°C to +125°C	60		

**Note 1:** Device is functional at VBORMIN < VDD < VDDMIN. Analog modules (ADC, op amp/comparator and comparator voltage reference) may have degraded performance. Device functionality is tested but not characterized. Refer to Parameter BO10 in Table 30-13 for the minimum and maximum BOR values.

## TABLE 30-2: THERMAL OPERATING CONDITIONS

Rating	Symbol	Min.	Тур.	Max.	Unit	
Industrial Temperature Devices						
Operating Junction Temperature Range	TJ	-40		+125	°C	
Operating Ambient Temperature Range	TA	-40		+85	°C	
Extended Temperature Devices						
Operating Junction Temperature Range	TJ	-40		+140	°C	
Operating Ambient Temperature Range	TA	-40		+125	°C	
Power Dissipation: Internal chip power dissipation: $PINT = VDD \times (IDD - \Sigma IOH)$ I/O Pin Power Dissipation:	PD		Pint + Pi/c	D	W	
$I/O = \Sigma (\{VDD - VOH\} \times IOH) + \Sigma (VOL \times IOL)$						
Maximum Allowed Power Dissipation	PDMAX	(	TJ — TA)/θJ	IA	W	

## TABLE 30-3: THERMAL PACKAGING CHARACTERISTICS

Characteristic	Symbol	Тур.	Max.	Unit	Notes
Package Thermal Resistance, 64-Pin QFN	θJA	28.0	_	°C/W	1
Package Thermal Resistance, 64-Pin TQFP 10x10 mm	θја	48.3		°C/W	1
Package Thermal Resistance, 48-Pin UQFN 6x6 mm	θја	41	-	°C/W	1
Package Thermal Resistance, 44-Pin QFN	θJA	29.0		°C/W	1
Package Thermal Resistance, 44-Pin TQFP 10x10 mm	θја	49.8		°C/W	1
Package Thermal Resistance, 44-Pin VTLA 6x6 mm	θја	25.2	_	°C/W	1
Package Thermal Resistance, 36-Pin VTLA 5x5 mm	θJA	28.5		°C/W	1
Package Thermal Resistance, 28-Pin QFN-S	θја	30.0		°C/W	1
Package Thermal Resistance, 28-Pin SSOP	θја	71.0	_	°C/W	1
Package Thermal Resistance, 28-Pin SOIC	θJA	69.7	_	°C/W	1
Package Thermal Resistance, 28-Pin SPDIP	θJA	60.0	_	°C/W	1

**Note 1:** Junction to ambient thermal resistance, Theta-JA ( $\theta$ JA) numbers are achieved by package simulations.

DC CH	ARACTE	RISTICS	Standard (unless of Operating	d Operatin otherwise g temperat	<b>g Conditic stated)</b> ure -40°( -40°(	o <b>ns: 3.0\</b> C ≤ Ta ≤ C ≤ Ta ≤	<b>/ to 3.6V</b> +85°C for Industrial +125°C for Extended			
Param No.	Symbol	Characteristic	Min. Typ. Max. Units Conditions							
	VIL	Input Low Voltage								
DI10		Any I/O Pin and MCLR	Vss	—	0.2 VDD	V				
DI18		I/O Pins with SDAx, SCLx	Vss	_	0.3 VDD	V	SMBus disabled			
DI19		I/O Pins with SDAx, SCLx	Vss	—	0.8	V	SMBus enabled			
	Vih	Input High Voltage								
DI20		I/O Pins Not 5V Tolerant	0.8 VDD	—	Vdd	V	(Note 3)			
		I/O Pins 5V Tolerant and MCLR	0.8 VDD	—	5.5	V	(Note 3)			
		I/O Pins with SDAx, SCLx	0.8 VDD	—	5.5	V	SMBus disabled			
		I/O Pins with SDAx, SCLx	2.1	—	5.5	V	SMBus enabled			
	ICNPU	Change Notification Pull-up Current								
DI30			150	250	550	μA	VDD = 3.3V, VPIN = VSS			
	ICNPD	Change Notification Pull-Down Current <sup>(4)</sup>								
DI31			20	50	100	μA	VDD = 3.3V, VPIN = VDD			

## TABLE 30-11: DC CHARACTERISTICS: I/O PIN INPUT SPECIFICATIONS

**Note 1:** The leakage current on the MCLR pin is strongly dependent on the applied voltage level. The specified levels represent normal operating conditions. Higher leakage current can be measured at different input voltages.

- 2: Negative current is defined as current sourced by the pin.
- 3: See the "Pin Diagrams" section for the 5V tolerant I/O pins.
- 4: VIL source < (VSS 0.3). Characterized but not tested.

**5:** Non-5V tolerant pins VIH source > (VDD + 0.3), 5V tolerant pins VIH source > 5.5V. Characterized but not tested.

- 6: Digital 5V tolerant pins cannot tolerate any "positive" input injection current from input sources > 5.5V.
- 7: Non-zero injection currents can affect the ADC results by approximately 4-6 counts.
- 8: Any number and/or combination of I/O pins not excluded under IICL or IICH conditions are permitted provided the mathematical "absolute instantaneous" sum of the input injection currents from all pins do not exceed the specified limit. Characterized but not tested.





## FIGURE 30-10: HIGH-SPEED PWMx MODULE TIMING CHARACTERISTICS (dsPIC33EPXXXMC20X/50X and PIC24EPXXXMC20X DEVICES ONLY)



## TABLE 30-29: HIGH-SPEED PWMx MODULE TIMING REQUIREMENTS (dsPIC33EPXXXMC20X/50X and PIC24EPXXXMC20X DEVICES ONLY)

AC CHARACTERISTICS				rd Opera otherwis ng tempe	ting Con se stated rature	ditions: 3 ) -40°C ≤ T -40°C ≤ T	<b>3.0V to 3.6V</b> $A \le +85^{\circ}C$ for Industrial $A \le +125^{\circ}C$ for Extended
Param No.	Symbol	Characteristic <sup>(1)</sup>	Min.	Тур.	Conditions		
MP10	TFPWM	PWMx Output Fall Time	—			ns	See Parameter DO32
MP11	TRPWM	PWMx Output Rise Time	_	_		ns	See Parameter DO31
MP20	TFD	Fault Input ↓ to PWMx I/O Change	_	_	15	ns	
MP30	Tfh	Fault Input Pulse Width	15	_		ns	

**Note 1:** These parameters are characterized but not tested in manufacturing.

# FIGURE 30-11: TIMERQ (QEI MODULE) EXTERNAL CLOCK TIMING CHARACTERISTICS (dsPIC33EPXXXMC20X/50X AND PIC24EPXXXMC20X DEVICES ONLY)



## TABLE 30-30: QEI MODULE EXTERNAL CLOCK TIMING REQUIREMENTS (dsPIC33EPXXXMC20X/50X AND PIC24EPXXXMC20X DEVICES ONLY)

AC CHARACTERISTICS			$\begin{array}{l} \mbox{Standard Operating Conditions: 3.0V to 3.6V} \\ \mbox{(unless otherwise stated)} \\ \mbox{Operating temperature} & -40^{\circ}C \leq TA \leq +85^{\circ}C \mbox{ for Industrial} \\ & -40^{\circ}C \leq TA \leq +125^{\circ}C \mbox{ for Extended} \end{array}$					
Param No.	Symbol	Chara	cteristic <sup>(1)</sup>	Min.	Тур.	Max.	Units	Conditions
TQ10	TtQH	TQCK High Time	Synchronous, with prescaler	Greater of 12.5 + 25 or (0.5 TCY/N) + 25			ns	Must also meet Parameter TQ15
TQ11	TtQL	TQCK Low Time	Synchronous, with prescaler	Greater of 12.5 + 25 or (0.5 Tcy/N) + 25	_	_	ns	Must also meet Parameter TQ15
TQ15	TtQP	TQCP Input Period	Synchronous, with prescaler	Greater of 25 + 50 or (1 Tcy/N) + 50	_	_	ns	
TQ20	TCKEXTMRL	Delay from External TQCK Clock Edge to Timer Increment		_	1	Тсү	—	

Note 1: These parameters are characterized but not tested in manufacturing.



## FIGURE 30-13: QEI MODULE INDEX PULSE TIMING CHARACTERISTICS (dsPIC33EPXXXMC20X/50X and PIC24EPXXXMC20X DEVICES ONLY)

## TABLE 30-32: QEI INDEX PULSE TIMING REQUIREMENTS (dsPIC33EPXXXMC20X/50X and PIC24EPXXXMC20X DEVICES ONLY)

AC CHA	RACTERI	STICS	$\begin{array}{l} \mbox{Standard Operating Conditions: 3.0V to 3.6V} \\ \mbox{(unless otherwise stated)} \\ \mbox{Operating temperature} & -40^{\circ}C \leq TA \leq +85^{\circ}C \mbox{ for Industrial} \\ -40^{\circ}C \leq TA \leq +125^{\circ}C \mbox{ for Extended} \end{array}$				
Param No.	Symbol	Characteristic <sup>(1)</sup>	Min.	Max.	Units	Conditions	
TQ50	TqiL	Filter Time to Recognize Low, with Digital Filter	3 * N * Tcy	_	ns	N = 1, 2, 4, 16, 32, 64, 128 and 256 <b>(Note 2)</b>	
TQ51	TqiH	Filter Time to Recognize High, with Digital Filter	3 * N * Tcy	—	ns	N = 1, 2, 4, 16, 32, 64, 128 and 256 <b>(Note 2)</b>	
TQ55	Tqidxr	Index Pulse Recognized to Position Counter Reset (ungated index)	3 TCY	—	ns		

**Note 1:** These parameters are characterized but not tested in manufacturing.

2: Alignment of index pulses to QEA and QEB is shown for position counter Reset timing only. Shown for forward direction only (QEA leads QEB). Same timing applies for reverse direction (QEA lags QEB) but index pulse recognition occurs on the falling edge.



## FIGURE 30-18: SPI2 SLAVE MODE (FULL-DUPLEX, CKE = 1, CKP = 0, SMP = 0) TIMING CHARACTERISTICS

# TABLE 30-40:SPI2 SLAVE MODE (FULL-DUPLEX, CKE = 0, CKP = 0, SMP = 0)TIMING REQUIREMENTS

АС СНА	ARACTERIS	$\label{eq:standard operating Conditions: 3.0V to 3.6V} \end{tabular} \begin{tabular}{lllllllllllllllllllllllllllllllllll$					
Param.	Symbol	Characteristic <sup>(1)</sup>	Min.	Typ. <sup>(2)</sup>	Max.	Units	Conditions
SP70	FscP	Maximum SCK2 Input Frequency	—	—	11	MHz	(Note 3)
SP72	TscF	SCK2 Input Fall Time	—	-	_	ns	See Parameter DO32 (Note 4)
SP73	TscR	SCK2 Input Rise Time	_	—	—	ns	See Parameter DO31 (Note 4)
SP30	TdoF	SDO2 Data Output Fall Time			_	ns	See Parameter DO31 (Note 4)
SP31	TdoR	SDO2 Data Output Rise Time	—	_	_	ns	See Parameter DO31 (Note 4)
SP35	TscH2doV, TscL2doV	SDO2 Data Output Valid after SCK2 Edge	—	6	20	ns	
SP36	TdoV2scH, TdoV2scL	SDO2 Data Output Setup to First SCK2 Edge	30	_	_	ns	
SP40	TdiV2scH, TdiV2scL	Setup Time of SDI2 Data Input to SCK2 Edge	30	_	_	ns	
SP41	TscH2diL, TscL2diL	Hold Time of SDI2 Data Input to SCK2 Edge	30	—	_	ns	
SP50	TssL2scH, TssL2scL	$\overline{SS2}$ ↓ to SCK2 ↑ or SCK2 ↓ Input	120		—	ns	
SP51	TssH2doZ	SS2 ↑ to SDO2 Output High-Impedance	10	—	50	ns	(Note 4)
SP52	TscH2ssH TscL2ssH	SS2 ↑ after SCK2 Edge	1.5 Tcy + 40	—		ns	(Note 4)

Note 1: These parameters are characterized, but are not tested in manufacturing.

2: Data in "Typical" column is at 3.3V, +25°C unless otherwise stated.

**3:** The minimum clock period for SCK2 is 91 ns. Therefore, the SCK2 clock generated by the master must not violate this specification.

4: Assumes 50 pF load on all SPI2 pins.

## 44-Lead Plastic Quad Flat, No Lead Package (ML) - 8x8 mm Body [QFN]

**Note:** For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



	MILLIMETERS				
Dimension	MIN	NOM	MAX		
Contact Pitch	E	0.65 BSC			
Optional Center Pad Width	W2	6.			
Optional Center Pad Length	T2			6.60	
Contact Pad Spacing	C1		8.00		
Contact Pad Spacing	C2		8.00		
Contact Pad Width (X44)	X1			0.35	
Contact Pad Length (X44)	Y1			0.85	
Distance Between Pads	G	0.25			

Notes:

1. Dimensioning and tolerancing per ASME Y14.5M

BSC: Basic Dimension. Theoretically exact value shown without tolerances.

Microchip Technology Drawing No. C04-2103B