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#### Details

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Product Status	Active
Core Processor	PIC
Core Size	16-Bit
Speed	60 MIPs
Connectivity	I <sup>2</sup> C, IrDA, LINbus, QEI, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, DMA, Motor Control PWM, POR, PWM, WDT
Number of I/O	21
Program Memory Size	128KB (43K x 24)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	8K x 16
Voltage - Supply (Vcc/Vdd)	3V ~ 3.6V
Data Converters	A/D 6x10b/12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 125°C (TA)
Mounting Type	Surface Mount
Package / Case	28-SOIC (0.295", 7.50mm Width)
Supplier Device Package	28-SOIC
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/pic24ep128mc202-e-so

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#### Pin Diagrams (Continued)



### TABLE 4-17: I2C1 AND I2C2 REGISTER MAP

File Name	Addr.	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	All Resets
I2C1RCV	0200	—	—	—	_	—	_	_	—				I2C1 Recei	ve Register				0000
I2C1TRN	0202	_	_	_	_	_	_	_	_				I2C1 Trans	mit Register				00FF
I2C1BRG	0204	_	_	_	_	_	_	_	Baud Rate Generator							0000		
I2C1CON	0206	I2CEN	_	I2CSIDL	SCLREL	IPMIEN	A10M	DISSLW	SMEN	GCEN	STREN	ACKDT	ACKEN	RCEN	PEN	RSEN	SEN	1000
I2C1STAT	0208	ACKSTAT	TRSTAT	_	_	_	BCL	GCSTAT	ADD10	IWCOL	I2COV	D_A	Р	S	R_W	RBF	TBF	0000
I2C1ADD	020A	—	_	—	_	—			I2C1 Address Register						0000			
I2C1MSK	020C	—	_	—	_	—						I2C1 Ad	dress Mask					0000
I2C2RCV	0210	_	_	_	_	_	_	_	_				I2C2 Recei	ve Register				0000
I2C2TRN	0212	_	_		—	—		_	—				I2C2 Trans	mit Register				00FF
I2C2BRG	0214	—	_	—	_	—		_				Bau	d Rate Gen	erator				0000
I2C2CON	0216	I2CEN	_	I2CSIDL	SCLREL	IPMIEN	A10M	DISSLW	SMEN	GCEN	STREN	ACKDT	ACKEN	RCEN	PEN	RSEN	SEN	1000
I2C2STAT	0218	ACKSTAT	TRSTAT		—	—	BCL	GCSTAT	ADD10	IWCOL	I2COV	D_A	Р	S	R_W	RBF	TBF	0000
I2C2ADD	021A	_		_	_	_	_		I2C2 Address Register 00							0000		
I2C2MSK	021C	_		_	_	_	_					I2C2 Ad	dress Mask					0000

Legend: — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

### TABLE 4-18: UART1 AND UART2 REGISTER MAP

SFR Name	Addr.	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	All Resets
U1MODE	0220	UARTEN	—	USIDL	IREN	RTSMD	—	UEN<	<1:0>	WAKE	LPBACK	ABAUD	URXINV	BRGH	PDSE	L<1:0>	STSEL	0000
U1STA	0222	UTXISEL1	UTXINV	UTXISEL0	_	UTXBRK	UTXEN	UTXBF	TRMT URXISEL<1:0> ADDEN RIDLE PERR FERR OERR URXDA						URXDA	0110		
U1TXREG	0224	_	_	-	_	_	_	_				UART	1 Transmit F	Register				xxxx
U1RXREG	0226	_	_	—	_	_	_	_	UART1 Receive Register						0000			
U1BRG	0228							Baud	Rate Gen	erator Pre	scaler							0000
U2MODE	0230	UARTEN	_	USIDL	IREN	RTSMD	_	UEN<	<1:0>	WAKE	LPBACK	ABAUD	URXINV	BRGH	PDSE	L<1:0>	STSEL	0000
U2STA	0232	UTXISEL1	UTXINV	UTXISEL0	_	UTXBRK	UTXEN	UTXBF	TRMT	URXI	SEL<1:0>	ADDEN	RIDLE	PERR	FERR	OERR	URXDA	0110
U2TXREG	0234	_	_	—	_	_	_	_				UART	2 Transmit F	Register				xxxx
U2RXREG	0236	_	_	—	_	_	_	_				UART	2 Receive F	Register				0000
U2BRG	0238							Baud	d Rate Generator Prescaler 0							0000		
			Less Bard de la checke de la Bard de condecte de la checke de la che															

Legend: x = unknown value on Reset, — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

### 4.8 Interfacing Program and Data Memory Spaces

The dsPIC33EPXXXGP50X, dsPIC33EPXXXMC20X/ 50X and PIC24EPXXXGP/MC20X architecture uses a 24-bit-wide Program Space (PS) and a 16-bit-wide Data Space (DS). The architecture is also a modified Harvard scheme, meaning that data can also be present in the Program Space. To use this data successfully, it must be accessed in a way that preserves the alignment of information in both spaces.

Aside from normal execution, the architecture of the dsPIC33EPXXXGP50X, dsPIC33EPXXXMC20X/50X and PIC24EPXXXGP/MC20X devices provides two methods by which Program Space can be accessed during operation:

- Using table instructions to access individual bytes or words anywhere in the Program Space
- Remapping a portion of the Program Space into the Data Space (Program Space Visibility)

Table instructions allow an application to read or write to small areas of the program memory. This capability makes the method ideal for accessing data tables that need to be updated periodically. It also allows access to all bytes of the program word. The remapping method allows an application to access a large block of data on a read-only basis, which is ideal for look-ups from a large table of static data. The application can only access the least significant word of the program word.

#### TABLE 4-65: PROGRAM SPACE ADDRESS CONSTRUCTION

	Access	Program Space Address								
Access Type	Space	<23>	<22:16>	<15>	<14:1>	<0>				
Instruction Access	User	0		PC<22:1>		0				
(Code Execution)			0xx xxxx xx	xx xxxx	xxxx xxx0					
TBLRD/TBLWT	User	TB	LPAG<7:0>		Data EA<15:0>					
(Byte/Word Read/Write)		0	xxx xxxx	xxxx xxx	x xxxx xxxx					
	Configuration	TBLPAG<7:0> Data EA<15:0>								
		1	XXX XXXX	XXXX XX	xx xxxx xxxx					

#### FIGURE 4-22: DATA ACCESS FROM PROGRAM SPACE ADDRESS GENERATION



Internut Course	Vector	IRQ		Inte	errupt Bit L	ocation
Interrupt Source	#	#	IVI Address	Flag	Enable	Priority
	Highe	est Natura	al Order Priority			
INT0 – External Interrupt 0	8	0	0x000014	IFS0<0>	IEC0<0>	IPC0<2:0>
IC1 – Input Capture 1	9	1	0x000016	IFS0<1>	IEC0<1>	IPC0<6:4>
OC1 – Output Compare 1	10	2	0x000018	IFS0<2>	IEC0<2>	IPC0<10:8>
T1 – Timer1	11	3	0x00001A	IFS0<3>	IEC0<3>	IPC0<14:12>
DMA0 – DMA Channel 0	12	4	0x00001C	IFS0<4>	IEC0<4>	IPC1<2:0>
IC2 – Input Capture 2	13	5	0x00001E	IFS0<5>	IEC0<5>	IPC1<6:4>
OC2 – Output Compare 2	14	6	0x000020	IFS0<6>	IEC0<6>	IPC1<10:8>
T2 – Timer2	15	7	0x000022	IFS0<7>	IEC0<7>	IPC1<14:12>
T3 – Timer3	16	8	0x000024	IFS0<8>	IEC0<8>	IPC2<2:0>
SPI1E – SPI1 Error	17	9	0x000026	IFS0<9>	IEC0<9>	IPC2<6:4>
SPI1 – SPI1 Transfer Done	18	10	0x000028	IFS0<10>	IEC0<10>	IPC2<10:8>
U1RX – UART1 Receiver	19	11	0x00002A	IFS0<11>	IEC0<11>	IPC2<14:12>
U1TX – UART1 Transmitter	20	12	0x00002C	IFS0<12>	IEC0<12>	IPC3<2:0>
AD1 – ADC1 Convert Done	21	13	0x00002E	IFS0<13>	IEC0<13>	IPC3<6:4>
DMA1 – DMA Channel 1	22	14	0x000030	IFS0<14>	IEC0<14>	IPC3<10:8>
Reserved	23	15	0x000032	_	_	_
SI2C1 – I2C1 Slave Event	24	16	0x000034	IFS1<0>	IEC1<0>	IPC4<2:0>
MI2C1 – I2C1 Master Event	25	17	0x000036	IFS1<1>	IEC1<1>	IPC4<6:4>
CM – Comparator Combined Event	26	18	0x000038	IFS1<2>	IEC1<2>	IPC4<10:8>
CN – Input Change Interrupt	27	19	0x00003A	IFS1<3>	IEC1<3>	IPC4<14:12>
INT1 – External Interrupt 1	28	20	0x00003C	IFS1<4>	IEC1<4>	IPC5<2:0>
Reserved	29-31	21-23	0x00003E-0x000042	_	_	_
DMA2 – DMA Channel 2	32	24	0x000044	IFS1<8>	IEC1<8>	IPC6<2:0>
OC3 – Output Compare 3	33	25	0x000046	IFS1<9>	IEC1<9>	IPC6<6:4>
OC4 – Output Compare 4	34	26	0x000048	IFS1<10>	IEC1<10>	IPC6<10:8>
T4 – Timer4	35	27	0x00004A	IFS1<11>	IEC1<11>	IPC6<14:12>
T5 – Timer5	36	28	0x00004C	IFS1<12>	IEC1<12>	IPC7<2:0>
INT2 – External Interrupt 2	37	29	0x00004E	IFS1<13>	IEC1<13>	IPC7<6:4>
U2RX – UART2 Receiver	38	30	0x000050	IFS1<14>	IEC1<14>	IPC7<10:8>
U2TX – UART2 Transmitter	39	31	0x000052	IFS1<15>	IEC1<15>	IPC7<14:12>
SPI2E – SPI2 Error	40	32	0x000054	IFS2<0>	IEC2<0>	IPC8<2:0>
SPI2 – SPI2 Transfer Done	41	33	0x000056	IFS2<1>	IEC2<1>	IPC8<6:4>
C1RX – CAN1 RX Data Ready <sup>(1)</sup>	42	34	0x000058	IFS2<2>	IEC2<2>	IPC8<10:8>
C1 – CAN1 Event <sup>(1)</sup>	43	35	0x00005A	IFS2<3>	IEC2<3>	IPC8<14:12>
DMA3 – DMA Channel 3	44	36	0x00005C	IFS2<4>	IEC2<4>	IPC9<2:0>
IC3 – Input Capture 3	45	37	0x00005E	IFS2<5>	IEC2<5>	IPC9<6:4>
IC4 – Input Capture 4	46	38	0x000060	IFS2<6>	IEC2<6>	IPC9<10:8>
Reserved	47-56	39-48	0x000062-0x000074	—	—	_
SI2C2 – I2C2 Slave Event	57	49	0x000076	IFS3<1>	IEC3<1>	IPC12<6:4>
MI2C2 – I2C2 Master Event	58	50	0x000078	IFS3<2>	IEC3<2>	IPC12<10:8>
Reserved	59-64	51-56	0x00007A-0x000084			
PSEM – PWM Special Event Match <sup>(2)</sup>	65	57	0x000086	IFS3<9>	IEC3<9>	IPC14<6:4>

#### TABLE 7-1: INTERRUPT VECTOR DETAILS

Note 1: This interrupt source is available on dsPIC33EPXXXGP50X and dsPIC33EPXXXMC50X devices only.

2: This interrupt source is available on dsPIC33EPXXXMC20X/50X and PIC24EPXXXMC20X devices only.

NOTES:

U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
				SCK2INR<6:0	>		
bit 15	·						bit 8
U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
—				SDI2R<6:0>			
bit 7							bit 0
Legend:							
R = Readab	le bit	W = Writable	bit	U = Unimplen	nented bit, rea	ad as '0'	
-n = Value a	t POR	'1' = Bit is set		'0' = Bit is cle	ared	x = Bit is unkı	nown
1.1.45			- <sup>1</sup>				
DIT 15	Unimpleme	nted: Read as	0.				
bit 14-8	SCK2INR<6 (see Table 1	5:0>: Assign SPI 1-2 for input pin	2 Clock Input selection nur	t (SCK2) to the mbers)	Correspondin	g RPn Pin bits	
	1111001 =	Input tied to RPI	121				
	•						
	0000001 =	Input tied to CM	P1				
	0000000 =	Input fied to Vss					
bit 7	Unimpleme	nted: Read as	0'				
bit 6-0	SDI2R<6:0> (see Table 1	<ul> <li>Assign SPI2 D</li> <li>1-2 for input pin</li> </ul>	ata Input (SE selection nur	012) to the Corre nbers)	esponding RP	n Pin bits	
	1111001 =	Input tied to RPI	121				
	•						
	0000001 =	Input tied to CM	P1				
	0000000 =	Input tied to Vss					

### REGISTER 11-12: RPINR22: PERIPHERAL PIN SELECT INPUT REGISTER 22

## 14.0 INPUT CAPTURE

- Note 1: This data sheet summarizes the features of the dsPIC33EPXXXGP50X, dsPIC33EPXXXMC20X/50X and PIC24EPXXXGP/MC20X families of devices. It is not intended to be a comprehensive reference source. To complement the information in this data sheet, refer to "Input Capture" (DS70352) in the "dsPIC33/dsPIC24 Family Reference Manual', which is available from the Microchip web site (www.microchip.com).
  - Some registers and associated bits described in this section may not be available on all devices. Refer to Section 4.0 "Memory Organization" in this data sheet for device-specific register and bit information.

The input capture module is useful in applications requiring frequency (period) and pulse measurement. The dsPIC33EPXXXGP50X, dsPIC33EPXXXMC20X/ 50X and PIC24EPXXXGP/MC20X devices support four input capture channels.

Key features of the input capture module include:

- Hardware-configurable for 32-bit operation in all modes by cascading two adjacent modules
- Synchronous and Trigger modes of output compare operation, with up to 19 user-selectable Trigger/Sync sources available
- A 4-level FIFO buffer for capturing and holding timer values for several events
- Configurable interrupt generation
- Up to six clock sources available for each module, driving a separate internal 16-bit counter





# 14.2 Input Capture Registers

#### REGISTER 14-1: ICxCON1: INPUT CAPTURE x CONTROL REGISTER 1

U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	U-0	U-0
—	—	ICSIDL	ICTSEL2	ICTSEL1	ICTSEL0	_	—
bit 15							bit 8

U-0	R/W-0	R/W-0	R/HC/HS-0	R/HC/HS-0	R/W-0	R/W-0	R/W-0
—	ICI1	ICI0	ICOV	ICBNE	ICM2	ICM1	ICM0
bit 7							bit 0

Legend:	HC = Hardware Clearable bit	IC = Hardware Clearable bit HS = Hardware Settable bit				
R = Readable bit	W = Writable bit	U = Unimplemented bit, rea	d as '0'			
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown			

bit 15-14	Unimplemented: Read as '0'
bit 13	ICSIDL: Input Capture Stop in Idle Control bit
	1 = Input capture will Halt in CPU Idle mode
	0 = Input capture will continue to operate in CPU Idle mode
bit 12-10	ICTSEL<2:0>: Input Capture Timer Select bits
	111 = Peripheral clock (FP) is the clock source of the ICx
	110 = Reserved
	101 = Reserved
	100 - 11 CLR is the clock source of the ICx (only the synchronous clock is supported) 011 = T5CLK is the clock source of the ICx
	010 = T4CLK is the clock source of the ICx
	001 = T2CLK is the clock source of the ICx
	000 = T3CLK is the clock source of the ICx
bit 9-7	Unimplemented: Read as '0'
bit 6-5	ICI<1:0>: Number of Captures per Interrupt Select bits (this field is not used if ICM<2:0> = 001 or 111)
	11 = Interrupt on every fourth capture event
	10 = Interrupt on every third capture event
	01 = Interrupt on every second capture event
hit 4	ICOV: Input Capture Overflow Status Flag bit (read-only)
Dit 4	1 = Input capture buffer overflow occurred
	0 = No input capture buffer overflow occurred
bit 3	ICBNE: Input Capture Buffer Not Empty Status bit (read-only)
	1 = Input capture buffer is not empty, at least one more capture value can be read
	0 = Input capture buffer is empty
bit 2-0	ICM<2:0>: Input Capture Mode Select bits
	111 = Input capture functions as interrupt pin only in CPU Sleep and Idle modes (rising edge detect only, all other control bits are not applicable)
	110 = Unused (module is disabled)
	101 = Capture mode, every 16th rising edge (Prescaler Capture mode)
	100 = Capture mode, every 4th rising edge (Prescaler Capture mode)
	011 = Capture mode, every falling edge (Simple Capture mode)
	001 = Capture mode, every edge rising and falling (Edge Detect mode (ICI<1:0>) is not used in this mode)
	000 = Input capture module is turned off

·							
R/W-1	R/W-1	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
PENH	PENL	POLH	POLL	PMOD1 <sup>(1)</sup>	PMOD0 <sup>(1)</sup>	OVRENH	OVRENL
bit 15							bit 8
R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
OVRDAT1	OVRDAT0	FLTDAT1	FLTDAT0	CLDAT1	CLDAT0	SWAP	OSYNC
bit 7							bit 0
Legend:							
R = Readable	bit	W = Writable	bit	U = Unimplei	mented bit, read	l as '0'	
-n = Value at F	POR	'1' = Bit is set		'0' = Bit is cle	eared	x = Bit is unkr	nown
bit 15	PENH: PWM	(H Output Pin (	Ownership bit				
	1 = PWMx mc	dule controls I	PWMxH pin WMx⊟ pin				
hit 11							
DIL 14	1 = DM/Mx mc	a Output Pin C					
	1 = PWWX IIIC 0 = GPIO model	dule controls P	WMxL pin				
hit 13		H Output Pin I	Polarity bit				
	1 = PWMxH r	in is active-low	/				
	0 = PWMxH p	oin is active-hig	h				
bit 12	POLL: PWMx	L Output Pin F	olarity bit				
	1 = PWMxL p	in is active-low	,				
	0 = PWMxL p	in is active-hig	h				
bit 11-10	PMOD<1:0>:	PWMx # I/O P	in Mode bits <sup>(1</sup>	)			
	11 = Reserve	d; do not use					
	10 = PWMx I/	O pin pair is in	the Push-Pul	I Output mode			
	01 = PWWx I/ 00 = PWMx I/	O pin pair is in O pin pair is in	the Complem	nt Output mod entary Output	mode		
hit 9	OVRENH: Ov	erride Enable i	for PWMxH P	in bit	mouo		
bit o	1 = OVRDAT	<1> controls or	itput on PWM	xH nin			
	0 = PWMx ge	nerator control	s PWMxH pin				
bit 8	OVRENL: Ov	erride Enable f	or PWMxL Pi	n bit			
	1 = OVRDAT	<0> controls ou	Itput on PWM	xL pin			
	0 = PWMx ge	nerator control	s PWMxL pin				
bit 7-6	OVRDAT<1:0	>: Data for PW	/MxH, PWMxl	L Pins if Overr	ide is Enabled b	its	
	If OVERENH	= 1, PWMxH is	s driven to the	state specifie	d by OVRDAT<	1>.	
	If OVERENL :	= 1, PWMxL is	driven to the	state specified	l by OVRDAT<0	>.	
bit 5-4	FLTDAT<1:0>	Data for PW	MxH and PWI	MxL Pins if FL	TMOD is Enable	ed bits	
	If Fault is activ	ve, PWMxH is	driven to the s	state specified	by FLTDAT<1>		
hit 2 0		VE, FVVIVIXL IS (			UY FLIDAISUS.	hita	
UIL 3-2	LUAI <1:0>			IXL PILIS IT ULN			
	If current-limit	is active. PWN	/IxL is driven t	the state sp	ecified by CLDA	T<0>.	
Note 1: The	ese bits should i	not be changed	d after the PW	Mx module is	enabled (PTEN	= 1).	

# REGISTER 16-13: IOCONx: PWMx I/O CONTROL REGISTER<sup>(2)</sup>

2: If the PWMLOCK Configuration bit (FOSCSEL<6>) is a '1', the IOCONx register can only be written after the unlock sequence has been executed.

# dsPIC33EPXXXGP50X, dsPIC33EPXXXMC20X/50X AND PIC24EPXXXGP/MC20X

U-0	U-0	U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0
—	—	—	_		LEB	<11:8>	
bit 15							bit 8
R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
			LEE	3<7:0>			
bit 7							bit 0
Legend:							
R = Readable	bit	W = Writable	bit	U = Unimpler	nented bit, rea	d as '0'	
-n = Value at F	POR	'1' = Bit is set		'0' = Bit is cle	ared	x = Bit is unkr	nown

### REGISTER 16-17: LEBDLYx: PWMx LEADING-EDGE BLANKING DELAY REGISTER

bit 15-12 Unimplemented: Read as '0'

bit 11-0 LEB<11:0>: Leading-Edge Blanking Delay for Current-Limit and Fault Inputs bits

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0				
QCAPEN	FLTREN	QFDIV2	QFDIV1	QFDIV0	OUTFNC1	OUTFNC0	SWPAB				
bit 15					• •		bit 8				
R/W-0	R/W-0	R/W-0	R/W-0	R-x	R-x	R-x	R-x				
HOMPOL	IDXPOL	QEBPOL	QEAPOL	HOME	INDEX	QEB	QEA				
bit 7							bit 0				
Legend:	a hit	\// - \//ritabla	h it	II – Unimploy	monted bit read	4 a.a. (0)					
n - Value at		vv = vvii(able	DIL	$0^{\circ} = 0$	nented bit, read	v – Ritic unkn					
		1 - Dit 13 36t			areu						
bit 15	OCAPEN: OF	-I Position Cou	nter Input Cap	ture Enable bit							
	1 = Index ma	tch event trigge	ers a position c	apture event							
	0 = Index ma	tch event does	not trigger a p	osition capture	event						
bit 14	FLTREN: QE	Ax/QEBx/INDX	x/HOMEx Digi	ital Filter Enabl	e bit						
	1 = Input pin	digital filter is e digital filter is d	nabled isabled (bypas	eed)							
hit 13_11			NDXv/HOMEv	Digital Input Fi	ilter Clock Divid	a Salact hits					
511 15-11	111 = 1:128 (	<b>QFDIV&lt;2:U&gt;:</b> QEAX/QEBX/INDXX/HOMEX Digital Input Filter Clock Divide Select bits									
	110 <b>= 1:64 cl</b>	110 = 1:64 clock divide									
	101 = 1:32 clock divide										
	011 = 1:8 clock divide										
	010 = 1:4 clock divide										
	001 = 1:2 clo	ck divide ck divide									
hit 10₋9			Output Functi	ion Mode Sele	rt hits						
bit 10 5	11 = The CTN	VCMPx pin ace	s high when C	$EI1LEC \ge POS$	$S1CNT \ge QEI10$	GEC					
	10 = The CTM	NCMPx pin goe	s high when P	$OS1CNT \leq QE$	EIILEC						
	01 = The CT	NCMPx pin goe	s high when P	$OS1CNT \ge QE$	EI1GEC						
hit 8	SWPAB: Swa	OFA and OFA	B Innuts hit								
bit 0	1 = QEAx and	d QEBx are swa	apped prior to	quadrature de	coder logic						
	0 = QEAx and	d QEBx are not	swapped	1							
bit 7	HOMPOL: HO	OMEx Input Po	larity Select bit	t							
	1 = Input is in	1 = Input is inverted									
hit 6		ot inverted Vy Input Dolori	ty Soloot bit								
DILO	1 = Input is in	verted	ly Select bit								
	0 = Input is no	ot inverted									
bit 5	QEBPOL: QE	EBx Input Polar	ity Select bit								
	1 = Input is ir	nverted									
L:1 4		ot inverted	:								
DIT 4		EAX Input Polar	ity Select bit								
	1 = 10000000000000000000000000000000000	not inverted									
bit 3	HOME: Statu	s of HOMEx In	out Pin After P	olarity Control							
	1 = Pin is at I	logic '1'		-							
	0 = Pin is at	logic '0'									

## REGISTER 17-2: QEI1IOC: QEI1 I/O CONTROL REGISTER

#### REGISTER 17-2: QEI1IOC: QEI1 I/O CONTROL REGISTER (CONTINUED)

- bit 2 INDEX: Status of INDXx Input Pin After Polarity Control
  - 1 = Pin is at logic '1'
  - 0 = Pin is at logic '0'
- bit 1 QEB: Status of QEBx Input Pin After Polarity Control And SWPAB Pin Swapping 1 = Pin is at logic '1' 0 = Pin is at logic '0'
- bit 0 **QEA:** Status of QEAx Input Pin After Polarity Control And SWPAB Pin Swapping 1 = Pin is at logic '1'
  - 0 = Pin is at logic '0'

R-0, HSC	R-0, HSC	U-0	U-0	U-0	R/C-0, HS	R-0, HSC	R-0, HSC	
ACKSTAT	TRSTAT	—	—	—	BCL	GCSTAT	ADD10	
bit 15							bit 8	
R/C-0, HS	R/C-0, HS	R-0, HSC	R/C-0, HSC	R/C-0, HSC	R-0, HSC	R-0, HSC	R-0, HSC	
IWCOL	I2COV	D_A	Р	S	R_W	RBF	TBF	
bit 7							bit 0	
Legend: C = Clearable bit		HS = Hardware Settable bit HSC = Hardware Settable/Clear			ettable/Clearable bit			
R = Readable bit W = Writable bit		U = Unimplen	nented bit, read	as '0'				
-n = Value at POR '1' =		'1' = Bit is se	et	'0' = Bit is cleared		x = Bit is unknown		

#### REGISTER 19-2: I2CxSTAT: I2Cx STATUS REGISTER

bit 15	<b>ACKSTAT:</b> Acknowledge Status bit (when operating as $I^2C^{TM}$ master, applicable to master transmit operation)
	1 = NACK received from slave 0 = ACK received from slave
	Hardware is set or clear at the end of slave Acknowledge.
bit 14	<b>TRSTAT:</b> Transmit Status bit (when operating as $I^2C$ master, applicable to master transmit operation) 1 = Master transmit is in progress (8 bits + ACK)
	0 = Master transmit is not in progress Hardware is set at the beginning of master transmission. Hardware is clear at the end of slave Acknowledge.
bit 13-11	Unimplemented: Read as '0'
bit 10	BCL: Master Bus Collision Detect bit
	<ul><li>1 = A bus collision has been detected during a master operation</li><li>0 = No bus collision detected</li></ul>
	Hardware is set at detection of a bus collision.
bit 9	GCSTAT: General Call Status bit
	1 = General call address was received
	0 = General call address was not received
1.11.0	Hardware is set when address matches general call address. Hardware is clear at Stop detection.
DIT 8	ADD10: 10-Bit Address Status bit
	I = 10-bit address was matched 0 = 10-bit address was not matched
	Hardware is set at the match of the 2nd byte of the matched 10-bit address. Hardware is clear at Stop detection.
bit 7	IWCOL: I2Cx Write Collision Detect bit
	1 = An attempt to write to the I2CxTRN register failed because the $I^2$ C module is busy 0 = No collision
	Hardware is set at the occurrence of a write to I2CxTRN while busy (cleared by software).
bit 6	I2COV: I2Cx Receive Overflow Flag bit
	<ul> <li>1 = A byte was received while the I2CxRCV register was still holding the previous byte</li> <li>0 = No overflow</li> </ul>
	Hardware is set at an attempt to transfer I2CxRSR to I2CxRCV (cleared by software).
bit 5	<b>D_A:</b> Data/Address bit (when operating as I <sup>2</sup> C slave)
	1 = Indicates that the last byte received was data
	<ul> <li>Indicates that the last byte received was a device address</li> <li>Hardware is clear at a device address match. Hardware is set by reception of a slave byte.</li> </ul>
bit 4	P: Stop bit
	1 = Indicates that a Stop bit has been detected last
	0 = Stop bit was not detected last
	Hardware is set or clear when a Start, Repeated Start or Stop is detected.

## 22.0 CHARGE TIME MEASUREMENT UNIT (CTMU)

- Note 1: This data sheet summarizes the features of the dsPIC33EPXXXGP50X, dsPIC33EPXXXMC20X/50X and PIC24EPXXXGP/MC20X family of devices. It is not intended to be a comprehensive reference source. To complement the information in this data sheet, refer to "Charge Time Measurement Unit (CTMU)" (DS70661) in the "dsPIC33/PIC24 Family Reference Manual", which is available on the Microchip web site (www.microchip.com).
  - Some registers and associated bits described in this section may not be available on all devices. Refer to Section 4.0 "Memory Organization" in this data sheet for device-specific register and bit information.

The Charge Time Measurement Unit is a flexible analog module that provides accurate differential time measurement between pulse sources, as well as asynchronous pulse generation. Its key features include:

- Four Edge Input Trigger Sources
- Polarity Control for Each Edge Source
- Control of Edge Sequence
- Control of Response to Edges
- · Precise Time Measurement Resolution of 1 ns
- Accurate Current Source Suitable for Capacitive Measurement
- On-Chip Temperature Measurement using a Built-in Diode

Together with other on-chip analog modules, the CTMU can be used to precisely measure time, measure capacitance, measure relative changes in capacitance or generate output pulses that are independent of the system clock.

The CTMU module is ideal for interfacing with capacitive-based sensors. The CTMU is controlled through three registers: CTMUCON1, CTMUCON2 and CTMUICON. CTMUCON1 and CTMUCON2 enable the module and control edge source selection, edge source polarity selection and edge sequencing. The CTMUICON register controls the selection and trim of the current source.

# dsPIC33EPXXXGP50X, dsPIC33EPXXXMC20X/50X AND PIC24EPXXXGP/MC20X

R/W-0	U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	
ADRC	—	—	SAMC4 <sup>(1)</sup>	SAMC3 <sup>(1)</sup>	SAMC2 <sup>(1)</sup>	SAMC1 <sup>(1)</sup>	SAMC0 <sup>(1)</sup>	
bit 15							bit 8	
R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	
ADCS7(2	<sup>2)</sup> ADCS6 <sup>(2)</sup>	ADCS5 <sup>(2)</sup>	ADCS4 <sup>(2)</sup>	ADCS3 <sup>(2)</sup>	ADCS2 <sup>(2)</sup>	ADCS1 <sup>(2)</sup>	ADCS0 <sup>(2)</sup>	
bit 7							bit 0	
Legend:								
R = Reada		vv = vvritable t	DIT		nented bit, read			
-n = value	at POR	"1" = Bit is set		$0^{\circ} = Bit is cle$	ared	x = Bit is unkr	nown	
bit 15	<ul> <li>ADRC: ADC1 Conversion Clock Source bit</li> <li>1 = ADC internal RC clock</li> <li>0 = Clock derived from system clock</li> </ul>							
bit 14-13	Unimplement	ted: Read as '0	3					
bit 12-8	SAMC<4:0>:	Auto-Sample T	ime bits <sup>(1)</sup>					
	11111 = 31 T. • • • • • •	AD						
hit 7 0	00000 = 0 IA		ion Clock Colo	at hita(2)				
bit 7-0 ADCS<7:0>: ADC1 Conversion Clock Select bits <sup>(2)</sup> 1111111 = TP • (ADCS<7:0> + 1) = TP • 256 = TAD • • • • • • • • • • • • • • • • • • •								
Note 1: 2:	<ul> <li>This bit is only used if SSRC&lt;2:0&gt; (AD1CON1&lt;7:5&gt;) = 111 and SSRCG (AD1CON1&lt;4&gt;) = 0.</li> <li>This bit is not used if ADRC (AD1CON3&lt;15&gt;) = 1.</li> </ul>							

#### REGISTER 23-3: AD1CON3: ADC1 CONTROL REGISTER 3

### REGISTER 24-8: PTGC1LIM: PTG COUNTER 1 LIMIT REGISTER<sup>(1)</sup>

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0			
	PTGC1LIM<15:8>									
bit 15							bit 8			
R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0			
	PTGC1LIM<7:0>									
bit 7							bit 0			
Logond										

Legenu.				
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'		
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown	

bit 15-0 **PTGC1LIM<15:0>:** PTG Counter 1 Limit Register bits May be used to specify the loop count for the PTGJMPC1 Step command or as a limit register for the General Purpose Counter 1.

## REGISTER 24-9: PTGHOLD: PTG HOLD REGISTER<sup>(1)</sup>

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	
PTGHOLD<15:8>								
bit 15							bit 8	

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	
PTGHOLD<7:0>								
bit 7 bit 0								

Legend:					
R = Readable bit	R = Readable bit W = Writable bit U = Unimplemented bit, read as '0'				
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown		

bit 15-0 **PTGHOLD<15:0>:** PTG General Purpose Hold Register bits Holds user-supplied data to be copied to the PTGTxLIM, PTGCxLIM, PTGSDLIM or PTGL0 registers with the PTGCOPY command.

**Note 1:** This register is read-only when the PTG module is executing Step commands (PTGEN = 1 and PTGSTRT = 1).

**Note 1:** This register is read-only when the PTG module is executing Step commands (PTGEN = 1 and PTGSTRT = 1).

#### REGISTER 25-2: CMxCON: COMPARATOR x CONTROL REGISTER (x = 1, 2 OR 3) (CONTINUED)

bit 7-6	EVPOL<1:0>: Trigger/Event/Interrupt Polarity Select bits
	<ul> <li>11 = Trigger/event/interrupt generated on any change of the comparator output (while CEVT = 0)</li> <li>10 = Trigger/event/interrupt generated only on high-to-low transition of the polarity selected comparator output (while CEVT = 0)</li> </ul>
	If CPOL = 1 (inverted polarity): Low-to-high transition of the comparator output.
	If CPOL = 0 (non-inverted polarity): High-to-low transition of the comparator output.
	01 = Trigger/event/interrupt generated only on low-to-high transition of the polarity-selected comparator output (while CEVT = 0)
	If CPOL = 1 (inverted polarity): High-to-low transition of the comparator output.
	If CPOL = 0 (non-inverted polarity): Low-to-high transition of the comparator output
	00 = Trigger/event/interrupt generation is disabled
bit 5	Unimplemented: Read as '0'
bit 4	<b>CREF:</b> Comparator Reference Select bit (VIN+ input) <sup>(1)</sup>
	<ul> <li>1 = VIN+ input connects to internal CVREFIN voltage<sup>(2)</sup></li> <li>0 = VIN+ input connects to CxIN1+ pin</li> </ul>
bit 3-2	Unimplemented: Read as '0'
bit 1-0	CCH<1:0>: Op Amp/Comparator Channel Select bits <sup>(1)</sup>
	<ul> <li>11 = Unimplemented</li> <li>10 = Unimplemented</li> <li>01 = Inverting input of the comparator connects to the CxIN2- pin<sup>(2)</sup></li> <li>00 = Inverting input of the op amp/comparator connects to the CxIN1- pin</li> </ul>

- **Note 1:** Inputs that are selected and not available will be tied to Vss. See the "**Pin Diagrams**" section for available inputs for each package.
  - 2: This output is not available when OPMODE (CMxCON<10>) = 1.

#### 27.2 User ID Words

dsPIC33EPXXXGP50X, dsPIC33EPXXXMC20X/50X and PIC24EPXXXGP/MC20X devices contain four User ID Words, located at addresses, 0x800FF8 through 0x800FFE. The User ID Words can be used for storing product information such as serial numbers, system manufacturing dates, manufacturing lot numbers and other application-specific information.

The User ID Words register map is shown in Table 27-3.

TABLE 27-3:USER ID WORDS REGISTER<br/>MAP

File Name	ile Name Address		Bits 15-0	
FUID0	0x800FF8	—	UID0	
FUID1	0x800FFA	—	UID1	
FUID2	0x800FFC	—	UID2	
FUID3	0x800FFE	—	UID3	

**Legend:** — = unimplemented, read as '1'.

### 27.3 On-Chip Voltage Regulator

All of the dsPIC33EPXXXGP50X, dsPIC33EPXXXMC20X/50X and PIC24EPXXXGP/ MC20X devices power their core digital logic at a nominal 1.8V. This can create a conflict for designs that are required to operate at a higher typical voltage, such as 3.3V. To simplify system design, all devices in the dsPIC33EPXXXGP50X, dsPIC33EPXXXMC20X/50X and PIC24EPXXXGP/MC20X family incorporate an onchip regulator that allows the device to run its core logic from VDD.

The regulator provides power to the core from the other VDD pins. A low-ESR (less than 1 Ohm) capacitor (such as tantalum or ceramic) must be connected to the VCAP pin (Figure 27-1). This helps to maintain the stability of the regulator. The recommended value for the filter capacitor is provided in Table 30-5 located in **Section 30.0 "Electrical Characteristics"**.

Note: It is important for the low-ESR capacitor to be placed as close as possible to the VCAP pin.

#### FIGURE 27-1: CONNECTIONS FOR THE ON-CHIP VOLTAGE

REGULATOR<sup>(1,2,3)</sup>



### 27.4 Brown-out Reset (BOR)

The Brown-out Reset (BOR) module is based on an internal voltage reference circuit that monitors the regulated supply voltage, VCAP. The main purpose of the BOR module is to generate a device Reset when a brown-out condition occurs. Brown-out conditions are generally caused by glitches on the AC mains (for example, missing portions of the AC cycle waveform due to bad power transmission lines or voltage sags due to excessive current draw when a large inductive load is turned on).

A BOR generates a Reset pulse, which resets the device. The BOR selects the clock source, based on the device Configuration bit values (FNOSC<2:0> and POSCMD<1:0>).

If an oscillator mode is selected, the BOR activates the Oscillator Start-up Timer (OST). The system clock is held until OST expires. If the PLL is used, the clock is held until the LOCK bit (OSCCON<5>) is '1'.

Concurrently, the PWRT Time-out (TPWRT) is applied before the internal Reset is released. If TPWRT = 0 and a crystal oscillator is being used, then a nominal delay of TFSCM is applied. The total delay in this case is TFSCM. Refer to Parameter SY35 in Table 30-22 of **Section 30.0 "Electrical Characteristics"** for specific TFSCM values.

The BOR status bit (RCON<1>) is set to indicate that a BOR has occurred. The BOR circuit continues to operate while in Sleep or Idle modes and resets the device should VDD fall below the BOR threshold voltage.

### 33.1 Package Marking Information (Continued)

48-Lead UQFN (6x6x0.5 mm)



Example 33EP64GP 504-I/MV (3) 1310017

64-Lead QFN (9x9x0.9 mm)



Example dsPIC33EP 64GP506 -I/MR® 1310017

64-Lead TQFP (10x10x1 mm)



Example



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#### 33.2 Package Details

#### 28-Lead Skinny Plastic Dual In-Line (SP) – 300 mil Body [SPDIP]

**Note:** For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



	Units		INCHES	
Dimensio	n Limits	MIN	NOM	MAX
Number of Pins	Ν		28	
Pitch	е		.100 BSC	
Top to Seating Plane	А	-	-	.200
Molded Package Thickness	A2	.120	.135	.150
Base to Seating Plane	A1	.015	-	-
Shoulder to Shoulder Width	E	.290	.310	.335
Molded Package Width	E1	.240	.285	.295
Overall Length	D	1.345	1.365	1.400
Tip to Seating Plane	L	.110	.130	.150
Lead Thickness	С	.008	.010	.015
Upper Lead Width	b1	.040	.050	.070
Lower Lead Width	b	.014	.018	.022
Overall Row Spacing §	eB	_	_	.430

#### Notes:

1. Pin 1 visual index feature may vary, but must be located within the hatched area.

2. § Significant Characteristic.

3. Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed .010" per side.

4. Dimensioning and tolerancing per ASME Y14.5M.

BSC: Basic Dimension. Theoretically exact value shown without tolerances.

Microchip Technology Drawing C04-070B