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Applications of "<u>Embedded -</u> <u>Microcontrollers</u>"

Details

Product Status	Obsolete
Core Processor	PIC
Core Size	16-Bit
Speed	60 MIPs
Connectivity	I ² C, IrDA, LINbus, QEI, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, DMA, Motor Control PWM, POR, PWM, WDT
Number of I/O	21
Program Memory Size	128KB (43K x 24)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	8K x 16
Voltage - Supply (Vcc/Vdd)	3V ~ 3.6V
Data Converters	A/D 6x10b/12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 150°C (TA)
Mounting Type	Surface Mount
Package / Case	28-SSOP (0.209", 5.30mm Width)
Supplier Device Package	28-SSOP
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/pic24ep128mc202-h-ss

Email: info@E-XFL.COM

Address: Room A, 16/F, Full Win Commercial Centre, 573 Nathan Road, Mongkok, Hong Kong



FIGURE 4-3: PROGRAM MEMORY MAP FOR dsPIC33EP128GP50X, dsPIC33EP128MC20X/50X AND PIC24EP128GP/MC20X DEVICES

IADLE 4	-10:	QEII	REGI			SFICSSE		5208/50/		CZ4EP/		ZUX DE	VICES U					
File Name	Addr.	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	All Resets
QEI1CON	01C0	QEIEN	—	QEISIDL		PIMOD<2:0>		IMV-	<1:0>			INTDIV<2:0	>	CNTPOL	GATEN	CCM	<1:0>	0000
QEI1IOC	01C2	QCAPEN	FLTREN		QFDIV<2:0>		OUTFN	NC<1:0>	SWPAB	HOMPOL	IDXPOL	QEBPOL	QEAPOL	HOME	INDEX	QEB	QEA	000x
QEI1STAT	01C4	_	—	PCHEQIRQ	PCHEQIEN	PCLEQIRQ	PCLEQIEN	POSOVIRQ	POSOVIEN	PCIIRQ	PCIIEN	VELOVIRQ	VELOVIEN	HOMIRQ	HOMIEN	IDXIRQ	IDXIEN	0000
POS1CNTL	01C6								POSCNT<15	0>								0000
POS1CNTH	01C8							F	POSCNT<31:	16>								0000
POS1HLD	01CA								POSHLD<15	0>								0000
VEL1CNT	01CC								VELCNT<15:	0>								0000
INT1TMRL	01CE								INTTMR<15:	0>								0000
INT1TMRH	01D0								INTTMR<31:1	6>								0000
INT1HLDL	01D2								INTHLD<15:)>								0000
INT1HLDH	01D4								INTHLD<31:1	6>								0000
INDX1CNTL	01D6								INDXCNT<15	:0>								0000
INDX1CNTH	01D8							I	NDXCNT<31:	16>								0000
INDX1HLD	01DA								INDXHLD<15	:0>								0000
QEI1GECL	01DC								QEIGEC<15:	0>								0000
QEI1ICL	01DC		QEIIC<15:0> 0000						0000									
QEI1GECH	01DE		QEIGEC<31:16> 000						0000									
QEI1ICH	01DE		QEIIC<31:16> 000						0000									
QEI1LECL	01E0		QEILEC<15:0> 0000						0000									
QEI1LECH	01E2		QEILEC<31:16> 0000															

TABLE 4-16: QEI1 REGISTER MAP FOR dsPIC33EPXXXMC20X/50X AND PIC24EPXXXMC20X DEVICES ONLY

Legend: x = unknown value on Reset, — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

TABLE 4-19: SPI1 AND SPI2 REGISTER MAP

SFR Name	Addr.	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	All Resets
SPI1STAT	0240	SPIEN	—	SPISIDL	—	—	:	SPIBEC<2:0	>	SRMPT	SPIROV	SRXMPT		SISEL<2:0>		SPITBF	SPIRBF	0000
SPI1CON1	0242	_	_	_	DISSCK	DISSDO	MODE16	SMP	CKE	SSEN	CKP	MSTEN		SPRE<2:0>		PPRE	<1:0>	0000
SPI1CON2	0244	FRMEN	SPIFSD	FRMPOL	_	_	_	_	_	_	_	—	_	_	_	FRMDLY	SPIBEN	0000
SPI1BUF	0248	8 SPI1 Transmit and Receive Buffer Register								0000								
SPI2STAT	0260	SPIEN	—	SPISIDL	—	—	:	SPIBEC<2:0)>	SRMPT	SPIROV	SRXMPT		SISEL<2:0>		SPITBF	SPIRBF	0000
SPI2CON1	0262	_	—		DISSCK	DISSDO	MODE16	SMP	CKE	SSEN	CKP	MSTEN		SPRE<2:0>		PPRE	<1:0>	0000
SPI2CON2	0264	FRMEN	SPIFSD	FRMPOL	_	_	_	_	_	_	_	—	_	_	_	FRMDLY	SPIBEN	0000
SPI2BUF	0268	SPI2 Transmit and Receive Buffer Register							0000									

Legend: — = unimplemented, read as '0'. Reset values are shown in hexadecimal.



EXAMPLE 4-3: PAGED DATA MEMORY SPACE

dsPIC33EPXXXGP50X, dsPIC33EPXXXMC20X/50X AND PIC24EPXXXGP/MC20X

4.4.3 DATA MEMORY ARBITRATION AND BUS MASTER PRIORITY

EDS accesses from bus masters in the system are arbitrated.

The arbiter for data memory (including EDS) arbitrates between the CPU, the DMA and the ICD module. In the event of coincidental access to a bus by the bus masters, the arbiter determines which bus master access has the highest priority. The other bus masters are suspended and processed after the access of the bus by the bus master with the highest priority.

By default, the CPU is Bus Master 0 (M0) with the highest priority and the ICD is Bus Master 4 (M4) with the lowest priority. The remaining bus master (DMA Controller) is allocated to M3 (M1 and M2 are reserved and cannot be used). The user application may raise or lower the priority of the DMA Controller to be above that of the CPU by setting the appropriate bits in the EDS Bus Master Priority Control (MSTRPR) register. All bus masters with raised priorities will maintain the same priority relationship relative to each other (i.e., M1 being highest and M3 being lowest, with M2 in between). Also, all the bus masters with priorities below

FIGURE 4-18: ARBITER ARCHITECTURE

that of the CPU maintain the same priority relationship relative to each other. The priority schemes for bus masters with different MSTRPR values are tabulated in Table 4-62.

This bus master priority control allows the user application to manipulate the real-time response of the system, either statically during initialization or dynamically in response to real-time events.

TABLE 4-62:	DATA MEMORY BUS
	ARBITER PRIORITY

Briority	MSTRPR<15:0> Bit Setting ⁽¹⁾					
Phoney	0x0000	0x0020				
M0 (highest)	CPU	DMA				
M1	Reserved	CPU				
M2	Reserved	Reserved				
M3	DMA	Reserved				
M4 (lowest)	ICD	ICD				

Note 1: All other values of MSTRPR<15:0> are reserved.



4.8.1 DATA ACCESS FROM PROGRAM MEMORY USING TABLE INSTRUCTIONS

The TBLRDL and TBLWTL instructions offer a direct method of reading or writing the lower word of any address within the Program Space without going through Data Space. The TBLRDH and TBLWTH instructions are the only method to read or write the upper 8 bits of a Program Space word as data.

The PC is incremented by two for each successive 24-bit program word. This allows program memory addresses to directly map to Data Space addresses. Program memory can thus be regarded as two 16-bit-wide word address spaces, residing side by side, each with the same address range. TBLRDL and TBLWTL access the space that contains the least significant data word. TBLRDH and TBLWTH access the space that contains the upper data byte.

Two table instructions are provided to move byte or word-sized (16-bit) data to and from Program Space. Both function as either byte or word operations.

- TBLRDL (Table Read Low):
 - In Word mode, this instruction maps the lower word of the Program Space location (P<15:0>) to a data address (D<15:0>)

- In Byte mode, either the upper or lower byte of the lower program word is mapped to the lower byte of a data address. The upper byte is selected when Byte Select is '1'; the lower byte is selected when it is '0'.
- TBLRDH (Table Read High):
 - In Word mode, this instruction maps the entire upper word of a program address (P<23:16>) to a data address. The 'phantom' byte (D<15:8>) is always '0'.
 - In Byte mode, this instruction maps the upper or lower byte of the program word to D<7:0> of the data address in the TBLRDL instruction. The data is always '0' when the upper 'phantom' byte is selected (Byte Select = 1).

In a similar fashion, two table instructions, TBLWTH and TBLWTL, are used to write individual bytes or words to a Program Space address. The details of their operation are explained in **Section 5.0 "Flash Program Memory"**.

For all table operations, the area of program memory space to be accessed is determined by the Table Page register (TBLPAG). TBLPAG covers the entire program memory space of the device, including user application and configuration spaces. When TBLPAG<7> = 0, the table page is located in the user memory space. When TBLPAG<7> = 1, the page is located in configuration space.



FIGURE 4-23: ACCESSING PROGRAM MEMORY WITH TABLE INSTRUCTIONS

11.5 I/O Helpful Tips

- 1. In some cases, certain pins, as defined in Table 30-11, under "Injection Current", have internal protection diodes to VDD and Vss. The term, "Injection Current", is also referred to as "Clamp Current". On designated pins, with sufficient external current-limiting precautions by the user, I/O pin input voltages are allowed to be greater or less than the data sheet absolute maximum ratings, with respect to the Vss and VDD supplies. Note that when the user application forward biases either of the high or low side internal input clamp diodes, that the resulting current being injected into the device, that is clamped internally by the VDD and Vss power rails, may affect the ADC accuracy by four to six counts.
- 2. I/O pins that are shared with any analog input pin (i.e., ANx) are always analog pins by default after any Reset. Consequently, configuring a pin as an analog input pin automatically disables the digital input pin buffer and any attempt to read the digital input level by reading PORTx or LATx will always return a '0', regardless of the digital logic level on the pin. To use a pin as a digital I/O pin on a shared ANx pin, the user application needs to configure the Analog Pin Configuration registers in the I/O ports module (i.e., ANSELx) by setting the appropriate bit that corresponds to that I/O port pin to a '0'.
- **Note:** Although it is not possible to use a digital input pin when its analog function is enabled, it is possible to use the digital I/O output function, TRISx = 0x0, while the analog function is also enabled. However, this is not recommended, particularly if the analog input is connected to an external analog voltage source, which would create signal contention between the analog signal and the output pin driver.
- 3. Most I/O pins have multiple functions. Referring to the device pin diagrams in this data sheet, the priorities of the functions allocated to any pins are indicated by reading the pin name from left-to-right. The left most function name takes precedence over any function to its right in the naming convention. For example: AN16/T2CK/T7CK/RC1. This indicates that AN16 is the highest priority in this example and will supersede all other functions to its right in the list. Those other functions to its right, even if enabled, would not work as long as any other function to its left was enabled. This rule applies to all of the functions listed for a given pin.
- 4. Each pin has an internal weak pull-up resistor and pull-down resistor that can be configured using the CNPUx and CNPDx registers, respectively. These resistors eliminate the need for external resistors in certain applications. The internal pull-up is up to ~(VDD - 0.8), not VDD. This value is still above the minimum VIH of CMOS and TTL devices.

5. When driving LEDs directly, the I/O pin can source or sink more current than what is specified in the VOH/IOH and VOL/IOL DC characteristic specification. The respective IOH and IOL current rating only applies to maintaining the corresponding output at or above the VOH, and at or below the VOL levels. However, for LEDs, unlike digital inputs of an externally connected device, they are not governed by the same minimum VIH/VIL levels. An I/O pin output can safely sink or source any current less than that listed in the absolute maximum rating section of this data sheet. For example:

VOH = 2.4V @ IOH = -8 mA and VDD = 3.3VThe maximum output current sourced by any 8 mA I/O pin = 12 mA.

LED source current < 12 mA is technically permitted. Refer to the VOH/IOH graphs in Section 30.0 "Electrical Characteristics" for additional information.

- 6. The Peripheral Pin Select (PPS) pin mapping rules are as follows:
 - a) Only one "output" function can be active on a given pin at any time, regardless if it is a dedicated or remappable function (one pin, one output).
 - b) It is possible to assign a "remappable output" function to multiple pins and externally short or tie them together for increased current drive.
 - c) If any "dedicated output" function is enabled on a pin, it will take precedence over any remappable "output" function.
 - d) If any "dedicated digital" (input or output) function is enabled on a pin, any number of "input" remappable functions can be mapped to the same pin.
 - e) If any "dedicated analog" function(s) are enabled on a given pin, "digital input(s)" of any kind will all be disabled, although a single "digital output", at the user's cautionary discretion, can be enabled and active as long as there is no signal contention with an external analog input signal. For example, it is possible for the ADC to convert the digital output logic level, or to toggle a digital output on a comparator or ADC input provided there is no external analog input, such as for a built-in self-test.
 - f) Any number of "input" remappable functions can be mapped to the same pin(s) at the same time, including to any pin with a single output from either a dedicated or remappable "output".

11.7 **Peripheral Pin Select Registers**

REGISTER 11-1: RPINR0: PERIPHERAL PIN SELECT INPUT REGISTER 0

U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
—				INT1R<6:0>			
bit 15							bit 8
U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
—	—	-	—	—	_	—	—
bit 7			•	•			bit 0

Legend:

Legena:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read	as '0'
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 14-8 INT1R<6:0>: Assign External Interrupt 1 (INT1) to the Corresponding RPn Pin bits (see Table 11-2 for input pin selection numbers) 1111001 = Input tied to RPI121 0000001 = Input tied to CMP1 0000000 = Input tied to Vss bit 7-0 Unimplemented: Read as '0'

15.1 Output Compare Resources

Many useful resources are provided on the main product page of the Microchip web site for the devices listed in this data sheet. This product page, which can be accessed using this link, contains the latest updates and additional information.

Note:	In the event you are not able to access the
	product page using the link above, enter
	this URL in your browser:
	http://www.microchip.com/wwwproducts/
	Devices.aspx?dDocName=en555464

15.1.1 KEY RESOURCES

- "Output Compare" (DS70358) in the "dsPIC33/ PIC24 Family Reference Manual"
- · Code Samples
- Application Notes
- Software Libraries
- Webinars
- All Related "dsPIC33/PIC24 Family Reference Manual" Sections
- Development Tools

16.0 HIGH-SPEED PWM MODULE (dsPIC33EPXXXMC20X/50X AND PIC24EPXXXMC20X DEVICES ONLY)

- Note 1: This data sheet summarizes the features of the dsPIC33EPXXXGP50X, dsPIC33EPXXXMC20X/50X and PIC24EPXXXGP/MC20X families of devices. It is not intended to be a comprehensive reference source. To complement the information in this data sheet, refer to "High-Speed PWM" (DS70645) in the "dsPIC33/PIC24 Family Reference Manual", which is available from the Microchip web site (www.microchip.com).
 - Some registers and associated bits described in this section may not be available on all devices. Refer to Section 4.0 "Memory Organization" in this data sheet for device-specific register and bit information.

The dsPIC33EPXXXMC20X/50X and PIC24EPXXXMC20X devices support a dedicated Pulse-Width Modulation (PWM) module with up to 6 outputs.

The high-speed PWMx module consists of the following major features:

- Three PWM generators
- Two PWM outputs per PWM generator
- Individual period and duty cycle for each PWM pair
- Duty cycle, dead time, phase shift and frequency resolution of Tcy/2 (7.14 ns at Fcy = 70MHz)
- Independent Fault and current-limit inputs for six PWM outputs
- · Redundant output
- Center-Aligned PWM mode
- Output override control
- Chop mode (also known as Gated mode)
- Special Event Trigger
- Prescaler for input clock
- PWMxL and PWMxH output pin swapping
- Independent PWM frequency, duty cycle and phase-shift changes for each PWM generator
- Dead-time compensation
- Enhanced Leading-Edge Blanking (LEB) functionality
- Frequency resolution enhancement
- PWM capture functionality

Note: In Edge-Aligned PWM mode, the duty cycle, dead time, phase shift and frequency resolution are 8.32 ns.

The high-speed PWMx module contains up to three PWM generators. Each PWM generator provides two PWM outputs: PWMxH and PWMxL. The master time base generator provides a synchronous signal as a common time base to synchronize the various PWM outputs. The individual PWM outputs are available on the output pins of the device. The input Fault signals and current-limit signals, when enabled, can monitor and protect the system by placing the PWM outputs into a known "safe" state.

Each PWMx can generate a trigger to the ADC module to sample the analog signal at a specific instance during the PWM period. In addition, the high-speed PWMx module also generates a Special Event Trigger to the ADC module based on either of the two master time bases.

The high-speed PWMx module can synchronize itself with an external signal or can act as a synchronizing source to any external device. The SYNCI1 input pin that utilizes PPS, can synchronize the high-speed PWMx module with an external signal. The SYNC01 pin is an output pin that provides a synchronous signal to an external device.

Figure 16-1 illustrates an architectural overview of the high-speed PWMx module and its interconnection with the CPU and other peripherals.

16.1 PWM Faults

The PWMx module incorporates multiple external Fault inputs to include FLT1 and FLT2 which are remappable using the PPS feature, FLT3 and FLT4 which are available only on the larger 44-pin and 64-pin packages, and FLT32 which has been implemented with Class B safety features, and is available on a fixed pin on all dsPIC33EPXXXMC20X/50X and PIC24EPXXXMC20X devices.

These Faults provide a safe and reliable way to safely shut down the PWM outputs when the Fault input is asserted.

16.1.1 PWM FAULTS AT RESET

During any Reset event, the PWMx module maintains ownership of the Class B Fault, FLT32. At Reset, this Fault is enabled in Latched mode to ensure the fail-safe power-up of the application. The application software must clear the PWM Fault before enabling the highspeed motor control PWMx module. To clear the Fault condition, the FLT32 pin must first be pulled low externally or the internal pull-down resistor in the CNPDx register can be enabled.

Note: The Fault mode may be changed using the FLTMOD<1:0> bits (FCLCON<1:0>), regardless of the state of FLT32.

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
QCAPEN	FLTREN	QFDIV2	QFDIV1	QFDIV0	OUTFNC1	OUTFNC0	SWPAB
bit 15					• •		bit 8
R/W-0	R/W-0	R/W-0	R/W-0	R-x	R-x	R-x	R-x
HOMPOL	IDXPOL	QEBPOL	QEAPOL	HOME	INDEX	QEB	QEA
bit 7							bit 0
Legend:	a hit	\// - \//ritabla	h it	II – Unimploy	monted bit read	4 a.a. (0)	
n - Value at		vv = vvii(able	DIL	$0^{\circ} = 0$	nented bit, read	v – Ritic unkn	
		1 - Dit 13 36t			areu		
bit 15	OCAPEN: OF	-I Position Cou	nter Input Cap	ture Enable bit			
	1 = Index ma	tch event trigge	ers a position c	apture event			
	0 = Index ma	tch event does	not trigger a p	osition capture	event		
bit 14	FLTREN: QE	Ax/QEBx/INDX	x/HOMEx Digi	ital Filter Enabl	e bit		
	1 = Input pin	digital filter is e digital filter is d	nabled isabled (bypas	eed)			
hit 13_11			NDXv/HOMEv	Digital Input Fi	ilter Clock Divid	a Salact hits	
511 15-11	111 = 1:128 (clock divide		Digital Input I			
	110 = 1:64 cl	ock divide					
	101 = 1:32 cl	ock divide					
	100 = 1.16 cm 011 = 1:8 clo	ck divide					
	010 = 1:4 clo	ck divide					
	001 = 1:2 clo	ck divide ck divide					
hit 10₋9			Output Functi	ion Mode Sele	rt hits		
bit 10 5	11 = The CTN	VCMPx pin ace	s high when C	$EI1LEC \ge POS$	$S1CNT \ge QEI10$	GEC	
	10 = The CTM	NCMPx pin goe	s high when P	$OS1CNT \leq QE$	EIILEC		
	01 = The CT	NCMPx pin goe	s high when P	$OS1CNT \ge QE$	EI1GEC		
hit 8	SWPAB: Swa	s uisabled an OEA and OE	B Innuts hit				
bit 0	1 = QEAx and	d QEBx are swa	apped prior to	quadrature de	coder logic		
	0 = QEAx and	d QEBx are not	swapped	1			
bit 7	HOMPOL: HO	OMEx Input Po	larity Select bit	t			
	1 = Input is in	iverted					
hit 6		ot inverted Vy Input Dolori	ty Soloot bit				
DILO	1 = Input is in	verted	ly Select bit				
	0 = Input is no	ot inverted					
bit 5	QEBPOL: QE	EBx Input Polar	ity Select bit				
	1 = Input is ir	nverted					
L:1 4		ot inverted	:				
DIT 4		EAX Input Polar	ity Select bit				
	1 = 10000000000000000000000000000000000	not inverted					
bit 3	HOME: Statu	s of HOMEx In	out Pin After P	olarity Control			
	1 = Pin is at I	logic '1'		-			
	0 = Pin is at	logic '0'					

REGISTER 17-2: QEI1IOC: QEI1 I/O CONTROL REGISTER

REGISTER 17-3: QEI1STAT: QEI1 STATUS REGISTER (CONTINUED)

bit 2	HOMIEN: Home Input Event Interrupt Enable bit 1 = Interrupt is enabled 0 = Interrupt is disabled
bit 1	IDXIRQ: Status Flag for Index Event Status bit 1 = Index event has occurred 0 = No Index event has occurred
bit 0	IDXIEN: Index Input Event Interrupt Enable bit 1 = Interrupt is enabled 0 = Interrupt is disabled

Note 1: This status bit is only applicable to PIMOD<2:0> modes, '011' and '100'.

20.3 UARTx Control Registers

REGISTER 20-1: UXMODE: UARTX MODE REGISTER

R/W-0	U-0	R/W-0	R/W-0	R/W-0	U-0	R/W-0	R/W-0		
UARTEN ⁽	¹⁾ —	USIDL	IREN ⁽²⁾	RTSMD	—	UEN1	UEN0		
bit 15							bit 8		
R/W-0, H	C R/W-0	R/W-0, HC	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0		
WAKE	LPBACK	ABAUD	URXINV	BRGH	PDSEL1	PDSEL0	STSEL		
bit 7							bit 0		
Legend: HC = Hardware Clearable bit									
R = Reada	ıble bit	W = Writable	bit	U = Unimplem	ented bit, read	as '0'			
-n = Value	at POR	'1' = Bit is set		'0' = Bit is clea	ared	x = Bit is unkn	iown		
bit 15	UARTEN: UA 1 = UARTx is 0 = UARTx is minimal	RTx Enable bits enabled; all U disabled; all L	(1) ARTx pins are IARTx pins are	controlled by U controlled by F	ARTx as define ORT latches; L	d by UEN<1:0 JARTx power c	> onsumption is		
bit 14	Unimplemen	ted: Read as ')'						
bit 13	USIDL: UART	Tx Stop in Idle I	Mode bit						
	1 = Discontin 0 = Continue	 1 = Discontinues module operation when device enters Idle mode 0 = Continues module operation in Idle mode 							
bit 12	IREN: IrDA [®] I 1 = IrDA enc 0 = IrDA enc	Encoder and Do oder and decoo	ecoder Enable ler are enablec ler are disable	bit ⁽²⁾ 1 d					
bit 11	RTSMD: Mod 1 = $\overline{\text{UxRTS}}$ p 0 = $\overline{\text{UxRTS}}$ p	le Selection for in is in Simplex in is in Flow Co	UxRTS Pin bit mode ontrol mode						
bit 10	Unimplemen	ted: Read as ')'						
bit 9-8	UEN<1:0>: U	ARTx Pin Enat	ole bits						
	11 = UxTX, UxRX and BCLKx pins are enabled and used; UxCTS pin is controlled by PORT latches ⁽³⁾ 10 = UxTX, UxRX, UxCTS and UxRTS pins are enabled and used ⁽⁴⁾ 01 = UxTX, UxRX and UxRTS pins are enabled and used; UxCTS pin is controlled by PORT latches ⁽⁴⁾ 00 = UxTX and UxRX pins are enabled and used; UxCTS and UxRTS/BCLKx pins are controlled by PORT latches								
bit 7	WAKE: Wake	WAKE: Wake-up on Start bit Detect During Sleep Mode Enable bit							
	1 = UARTx c in hardwa 0 = No wake	 1 = UARTx continues to sample the UxRX pin; interrupt is generated on the falling edge; bit is cleared in hardware on the following rising edge 0 = No wake-up is enabled 							
bit 6	LPBACK: UA	LPBACK: UARTx Loopback Mode Select bit							
	1 = Enables Loopback mode								
	0 = Loopbacl	k mode is disat	led						
Note 1:	Refer to the "UAF enabling the UAR	RT " (DS70582) Tx module for r	section in the " eceive or transi	dsPIC33/PIC24 mit operation.	Family Referen	ce Manual" for i	nformation on		
2:	This feature is on	ly available for	the 16x BRG r	node (BRGH =	0).				
3:	his feature is only available on 44-pin and 64-pin devices.								

4: This feature is only available on 64-pin devices.

U-0	U-0	R-0	R-0	R-0	R-0	R-0	R-0		
	_	FBP5	FBP4	FBP3	FBP2	FBP1	FBP0		
bit 15	÷						bit 8		
U-0	U-0	R-0	R-0	R-0	R-0	R-0	R-0		
_	—	FNRB5	FNRB4	FNRB3	FNRB2	FNRB1	FNRB0		
bit 7 bit									
Legend:									
R = Readab	le bit	W = Writable	bit	U = Unimpler	mented bit, read	d as '0'			
-n = Value a	t POR	'1' = Bit is set		'0' = Bit is cle	ared	x = Bit is unk	nown		
bit 15-14	Unimplemen	ted: Read as '	0'						
bit 13-8	FBP<5:0>: F	IFO Buffer Poir	nter bits						
	011111 = RE	331 buffer							
	•	50 bullet							
	•								
	•								
	000001 = TR	RB1 buffer							
	000000 = TR	RB0 buffer							
bit 7-6	Unimplemen	ted: Read as '	0'						
bit 5-0	FNRB<5:0>:	FIFO Next Rea	ad Buffer Poin	ter bits					
	011111 = RE	331 buffer							
	011110 = RE	330 buffer							
	•								
	•								
	•	DD1 buffor							
	000001 = TR	RB0 buffer							

REGISTER 21-5: CxFIFO: ECANx FIFO STATUS REGISTER

26.0 PROGRAMMABLE CYCLIC REDUNDANCY CHECK (CRC) GENERATOR

- Note 1: This data sheet summarizes the features of the dsPIC33EPXXXGP50X, dsPIC33EPXXXMC20X/50X and PIC24EPXXXGP/MC20X families of devices. It is not intended to be a comprehensive reference source. To complement the information in this data sheet, refer to "Programmable Cyclic Redundancy Check (CRC)" (DS70346) of the "dsPIC33/PIC24 Family Reference Manual", which is available from the Microchip web site (www.microchip.com).
 - Some registers and associated bits described in this section may not be available on all devices. Refer to Section 4.0 "Memory Organization" in this data sheet for device-specific register and bit information.

The programmable CRC generator offers the following features:

- User-programmable (up to 32nd order) polynomial CRC equation
- Interrupt output
- Data FIFO

The programmable CRC generator provides a hardware implemented method of quickly generating checksums for various networking and security applications. It offers the following features:

- User-programmable CRC polynomial equation, up to 32 bits
- Programmable shift direction (little or big-endian)
- · Independent data and polynomial lengths
- Configurable interrupt output
- Data FIFO

A simplified block diagram of the CRC generator is shown in Figure 26-1. A simple version of the CRC shift engine is shown in Figure 26-2.



FIGURE 26-1: CRC BLOCK DIAGRAM

DC CHARACTERISTICS Standard Operating Conditions: (unless otherwise stated) Operating temperature -40°C ≤ 1 -40°C < 1				ating Conditions: 3.0V to ise stated) erature $-40^{\circ}C \le TA \le +82$ $-40^{\circ}C < TA < +12$	3.6V 5°C for Industrial 25°C for Extended				
Parameter No.	Тур.	Max.	Units	itions					
Power-Down	Power-Down Current (IPD) ⁽¹⁾ – dsPIC33EP32GP50X, dsPIC33EP32MC20X/50X and PIC24EP32GP/MC20X								
DC60d	30	100	μA	-40°C					
DC60a	35	100	μA	+25°C	3.3V				
DC60b	150	200	μA	+85°C					
DC60c	250	500	μA	+125°C					
Power-Down	Current (IPD) ⁽¹⁾ -	dsPIC33EP64GI	P50X, dsPIC33EI	P64MC20X/50X and PIC2	24EP64GP/MC20X				
DC60d	25	100	μA	-40°C	3 3\/				
DC60a	30	100	μA	+25°C					
DC60b	150	350	μA	+85°C	3.3V				
DC60c	350	800	μA	+125°C					
Power-Down	Current (IPD) ⁽¹⁾ –	dsPIC33EP128G	P50X, dsPIC33E	P128MC20X/50X and PI	C24EP128GP/MC20X				
DC60d	30	100	μA	-40°C					
DC60a	35	100	μA	+25°C	3 3//				
DC60b	150	350	μA	+85°C	5.50				
DC60c	550	1000	μA	+125°C					
Power-Down	Current (IPD) ⁽¹⁾ –	dsPIC33EP256G	P50X, dsPIC33E	P256MC20X/50X and PIC	C24EP256GP/MC20X				
DC60d	35	100	μA	-40°C					
DC60a	40	100	μA	+25°C	3 3//				
DC60b	250	450	μA	+85°C	5.5 V				
DC60c	1000	1200	μA	+125°C					
Power-Down	Current (IPD) ⁽¹⁾ –	dsPIC33EP512G	P50X, dsPIC33E	P512MC20X/50X and PI	C24EP512GP/MC20X				
DC60d	40	100	μA	-40°C					
DC60a	45	100	μA	+25°C	3 3\/				
DC60b	350	800	μA	+85°C	3.3V				
DC60c	1100	1500	μA	+125°C					

TABLE 30-8: DC CHARACTERISTICS: POWER-DOWN CURRENT (IPD)

Note 1: IPD (Sleep) current is measured as follows:

• CPU core is off, oscillator is configured in EC mode and external clock is active; OSC1 is driven with external square wave from rail-to-rail (EC clock overshoot/undershoot < 250 mV required)

- · CLKO is configured as an I/O input pin in the Configuration Word
- All I/O pins are configured as inputs and pulled to Vss
- MCLR = VDD, WDT and FSCM are disabled
- All peripheral modules are disabled (PMDx bits are all set)
- The VREGS bit (RCON<8>) = 0 (i.e., core regulator is set to standby while the device is in Sleep mode)
- The VREGSF bit (RCON<11>) = 0 (i.e., Flash regulator is set to standby while the device is in Sleep mode)
- JTAG is disabled

DC CHARACTERISTICS			$\begin{tabular}{lllllllllllllllllllllllllllllllllll$					
Param No.	Symbol	Characteristic	Min.	Conditions				
		Program Flash Memory						
D130	Eр	Cell Endurance	10,000		_	E/W	-40°C to +125°C	
D131	Vpr	VDD for Read	3.0		3.6	V		
D132b	VPEW	VDD for Self-Timed Write	3.0		3.6	V		
D134	TRETD	Characteristic Retention	20	—	—	Year	Provided no other specifications are violated, -40°C to +125°C	
D135	IDDP	Supply Current during Programming ⁽²⁾	—	10	—	mA		
D136	IPEAK	Instantaneous Peak Current During Start-up	_	_	150	mA		
D137a	Тре	Page Erase Time	17.7	—	22.9	ms	TPE = 146893 FRC cycles, Ta = +85°C (See Note 3)	
D137b	Тре	Page Erase Time	17.5	_	23.1	ms	TPE = 146893 FRC cycles, TA = +125°C (See Note 3)	
D138a	Tww	Word Write Cycle Time	41.7	_	53.8	μs	Tww = 346 FRC cycles, TA = +85°C (See Note 3)	
D138b	Tww	Word Write Cycle Time	41.2	—	54.4	μs	Tww = 346 FRC cycles, Ta = +125°C (See Note 3)	

TABLE 30-14: DC CHARACTERISTICS: PROGRAM MEMORY

Note 1: Data in "Typical" column is at 3.3V, +25°C unless otherwise stated.

2: Parameter characterized but not tested in manufacturing.

3: Other conditions: FRC = 7.37 MHz, TUN<5:0> = 011111 (for Minimum), TUN<5:0> = 100000 (for Maximum). This parameter depends on the FRC accuracy (see Table 30-19) and the value of the FRC Oscillator Tuning register (see Register 9-4). For complete details on calculating the Minimum and Maximum time, see Section 5.3 "Programming Operations".



AC CHARACTERISTICS			Standard Ope (unless other) Operating tem	rating Co wise state perature	pnditions: 3.0V to 3.6V ed) $-40^{\circ}C \le TA \le +85^{\circ}C$ for Industrial $-40^{\circ}C \le TA \le +125^{\circ}C$ for Extended			
Param No.	Symb	Characteristic	Min.	Тур. ⁽¹⁾	Max.	Units	Conditions	
OS10	FIN	External CLKI Frequency (External clocks allowed only in EC and ECPLL modes)	DC	_	60	MHz	EC	
		Oscillator Crystal Frequency	3.5 10	—	10 25	MHz MHz	XT HS	
OS20	Tosc	Tosc = 1/Fosc	8.33	—	DC	ns	+125°C	
		Tosc = 1/Fosc	7.14	—	DC	ns	+85°C	
OS25	TCY	Instruction Cycle Time ⁽²⁾	16.67	—	DC	ns	+125°C	
		Instruction Cycle Time ⁽²⁾	14.28	—	DC	ns	+85°C	
OS30	TosL, TosH	External Clock in (OSC1) High or Low Time	0.45 x Tosc	—	0.55 x Tosc	ns	EC	
OS31	TosR, TosF	External Clock in (OSC1) Rise or Fall Time	—	—	20	ns	EC	
OS40	TckR	CLKO Rise Time ^(3,4)	—	5.2	—	ns		
OS41	TckF	CLKO Fall Time ^(3,4)	—	5.2	—	ns		
OS42	Gм	External Oscillator Transconductance ⁽⁴⁾	—	12	—	mA/V	HS, VDD = 3.3V, TA = +25°C	
			—	6	—	mA/V	XT, VDD = 3.3V, TA = +25°C	

TABLE 30-17: EXTERNAL CLOCK TIMING REQUIREMENTS

Note 1: Data in "Typical" column is at 3.3V, +25°C unless otherwise stated.

- 2: Instruction cycle period (TCY) equals two times the input oscillator time base period. All specified values are based on characterization data for that particular oscillator type under standard operating conditions with the device executing code. Exceeding these specified limits may result in an unstable oscillator operation and/or higher than expected current consumption. All devices are tested to operate at "Minimum" values with an external clock applied to the OSC1 pin. When an external clock input is used, the "Maximum" cycle time limit is "DC" (no clock) for all devices.
- 3: Measurements are taken in EC mode. The CLKO signal is measured on the OSC2 pin.
- 4: This parameter is characterized, but not tested in manufacturing.

TABLE 30-47:SPI1 SLAVE MODE (FULL-DUPLEX, CKE = 0, CKP = 1, SMP = 0)TIMING REQUIREMENTS

AC CHARACTERISTICS			$\label{eq:standard operating Conditions: 3.0V to 3.6V} \mbox{(unless otherwise stated)} \mbox{Operating temperature} $-40^{\circ}C \le TA \le +85^{\circ}C$ for Industrial $-40^{\circ}C \le TA \le +125^{\circ}C$ for Extended} $				
Param.	Symbol	Characteristic ⁽¹⁾	Min.	Typ. ⁽²⁾	Max.	Units	Conditions
SP70	FscP	Maximum SCK1 Input Frequency	—	—	15	MHz	(Note 3)
SP72	TscF	SCK1 Input Fall Time	—	-	_	ns	See Parameter DO32 (Note 4)
SP73	TscR	SCK1 Input Rise Time	_	—	—	ns	See Parameter DO31 (Note 4)
SP30	TdoF	SDO1 Data Output Fall Time			_	ns	See Parameter DO32 (Note 4)
SP31	TdoR	SDO1 Data Output Rise Time	—	-	_	ns	See Parameter DO31 (Note 4)
SP35	TscH2doV, TscL2doV	SDO1 Data Output Valid after SCK1 Edge	—	6	20	ns	
SP36	TdoV2scH, TdoV2scL	SDO1 Data Output Setup to First SCK1 Edge	30	_	_	ns	
SP40	TdiV2scH, TdiV2scL	Setup Time of SDI1 Data Input to SCK1 Edge	30	_	_	ns	
SP41	TscH2diL, TscL2diL	Hold Time of SDI1 Data Input to SCK1 Edge	30	—	_	ns	
SP50	TssL2scH, TssL2scL	$\overline{SS1}$ ↓ to SCK1 ↑ or SCK1 ↓ Input	120		—	ns	
SP51	TssH2doZ	SS1 ↑ to SDO1 Output High-Impedance	10	—	50	ns	(Note 4)
SP52	TscH2ssH, TscL2ssH	SS1 ↑ after SCK1 Edge	1.5 Tcy + 40	—	_	ns	(Note 4)

Note 1: These parameters are characterized, but are not tested in manufacturing.

2: Data in "Typical" column is at 3.3V, +25°C unless otherwise stated.

3: The minimum clock period for SCK1 is 66.7 ns. Therefore, the SCK1 clock generated by the master must not violate this specification.

4: Assumes 50 pF load on all SPI1 pins.

31.2 **AC Characteristics and Timing Parameters**

The information contained in this section defines dsPIC33EPXXXGP50X, dsPIC33EPXXXMC20X/50X and PIC24EPXXXGP/MC20X AC characteristics and timing parameters for high-temperature devices. However, all AC timing specifications in this section are the same as those in Section 30.2 "AC Characteristics and Timing Parameters", with the exception of the parameters listed in this section.

Parameters in this section begin with an H, which denotes High temperature. For example, Parameter OS53 in Section 30.2 "AC Characteristics and Timing Parameters" is the Industrial and Extended temperature equivalent of HOS53.

TABLE 31-9: TEMPERATURE AND VOLTAGE SPECIFICATIONS – AC

	Standard Operating Conditions: 3.0V to 3.6V
	(unless otherwise stated)
AC CHARACTERISTICS	Operating temperature $-40^{\circ}C \le TA \le +150^{\circ}C$
	Operating voltage VDD range as described in Table 31-1.

FIGURE 31-1: LOAD CONDITIONS FOR DEVICE TIMING SPECIFICATIONS



TABLE 31-10: PLL CLOCK TIMING SPECIFICATIONS

AC CHARACTERISTICS			Standard Operating Conditions: 3.0V to 3.6V(unless otherwise stated)Operating temperature $-40^{\circ}C \le TA \le +150^{\circ}C$				
Param No.	Symbol	Characteristic	Min Typ Max Units Conditions				
HOS53	DCLK	CLKO Stability (Jitter) ⁽¹⁾	-5	0.5	5	%	Measured over 100 ms period

These parameters are characterized by similarity, but are not tested in manufacturing. This specification is Note 1: based on clock cycle by clock cycle measurements. To calculate the effective jitter for individual time bases or communication clocks use this formula:

$$Peripheral Clock Jitter = \frac{DCLK}{\sqrt{\frac{FOSC}{Peripheral Bit Rate Clock}}}$$

For example: FOSC = 32 MHz, DCLK = 5%, SPIx bit rate clock (i.e., SCKx) is 2 MHz. Г

$$SPI SCK Jitter = \left\lfloor \frac{D_{CLK}}{\sqrt{\left(\frac{32 MHz}{2 MHz}\right)}} \right\rfloor = \left\lfloor \frac{5\%}{\sqrt{16}} \right\rfloor = \left\lfloor \frac{5\%}{4} \right\rfloor = 1.25\%$$

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