What is "<u>Embedded - Microcontrollers</u>"?

"<u>Embedded - Microcontrollers</u>" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.
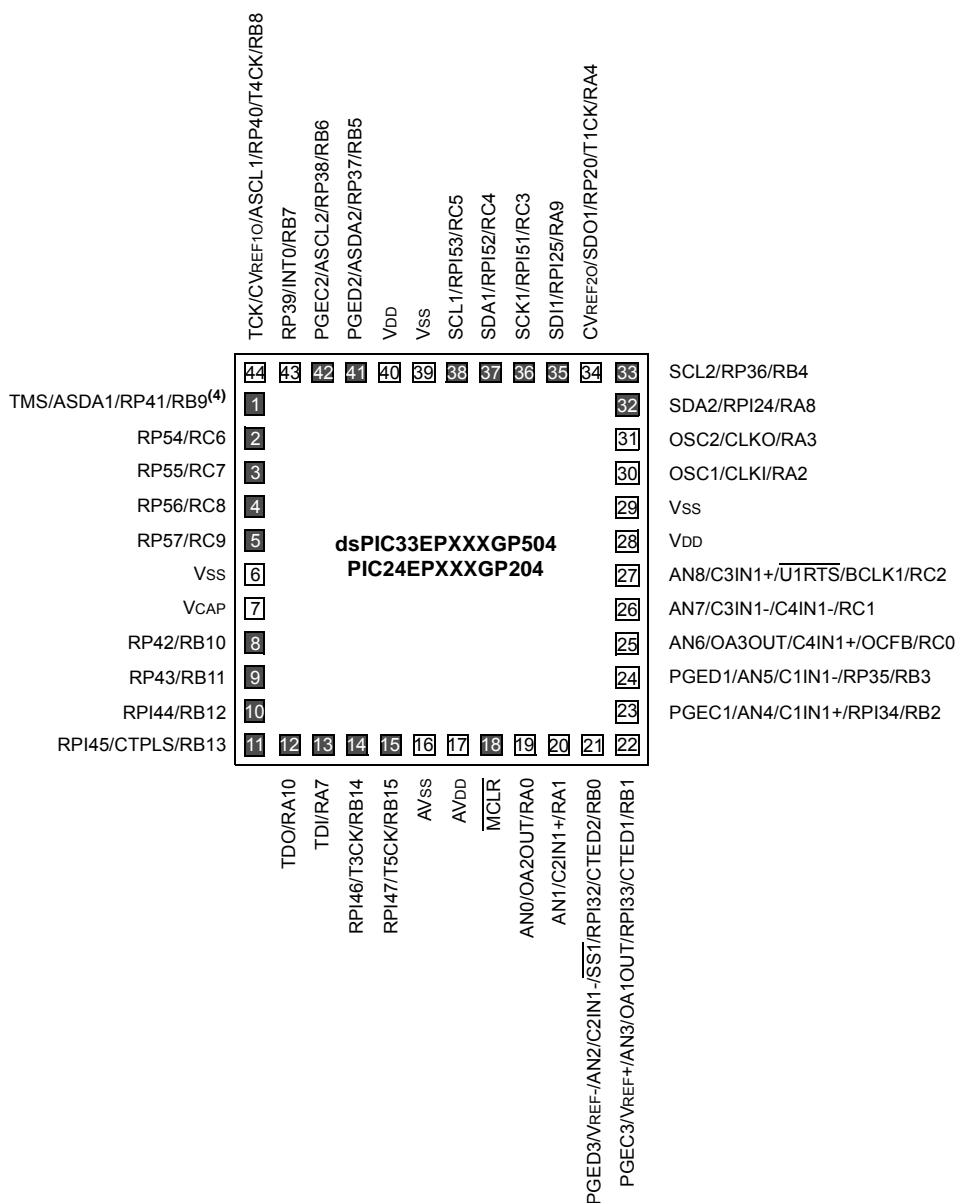
Applications of "<u>Embedded - Microcontrollers</u>"

Details	
Product Status	Active
Core Processor	PIC
Core Size	16-Bit
Speed	70 MIPs
Connectivity	I²C, IrDA, LINbus, QEI, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, DMA, Motor Control PWM, POR, PWM, WDT
Number of I/O	21
Program Memory Size	128KB (43K x 24)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	8K x 16
Voltage - Supply (Vcc/Vdd)	3V ~ 3.6V
Data Converters	A/D 6x10b/12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	28-VQFN Exposed Pad
Supplier Device Package	28-QFN-S (6x6)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/pic24ep128mc202-i-mm

Pin Diagrams (Continued)

44-Pin VTLA[1,2,3]

■ = Pins are up to 5V tolerant

Top pins (left to right), pins 44–34:
- 44: TCK/CVREF1O/ASCL1/RP40/T4CK/RB8
- 43: RP39/INT0/RB7
- 42: PGEC2/ASCL2/RP38/RB6
- 41: PGED2/ASDA2/RP37/RB5
- 40: VDD
- 39: VSS
- 38: SCL1/RPI53/RC5
- 37: SDA1/RPI52/RC4
- 36: SCK1/RPI51/RC3
- 35: SDI1/RPI25/RA9
- 34: CVREF2O/SDO1/RP20/T1CK/RA4

Left side pins 1–11:
- 1: TMS/ASDA1/RP41/RB9[4]
- 2: RP54/RC6
- 3: RP55/RC7
- 4: RP56/RC8
- 5: RP57/RC9
- 6: VSS
- 7: VCAP
- 8: RP42/RB10
- 9: RP43/RB11
- 10: RPI44/RB12
- 11: RPI45/CTPLS/RB13

Center:
dsPIC33EPXXXGP504
PIC24EPXXXGP204

Right side pins 33–23:
- 33: SCL2/RP36/RB4
- 32: SDA2/RPI24/RA8
- 31: OSC2/CLKO/RA3
- 30: OSC1/CLKI/RA2
- 29: VSS
- 28: VDD
- 27: AN8/C3IN1+/U1RTS/BCLK1/RC2
- 26: AN7/C3IN1-/C4IN1-/RC1
- 25: AN6/OA3OUT/C4IN1+/OCFB/RC0
- 24: PGED1/AN5/C1IN1-/RP35/RB3
- 23: PGEC1/AN4/C1IN1+/RPI34/RB2

Bottom pins (left to right) 12–22:
- 12: TDO/RA10
- 13: TDI/RA7
- 14: RPI46/T3CK/RB14
- 15: RPI47/T5CK/RB15
- 16: AVSS
- 17: AVDD
- 18: MCLR
- 19: AN0/OA2OUT/RA0
- 20: AN1/C2IN1+/RA1
- 21: PGED3/VREF-/AN2/C2IN1-/SS1/RPI32/CTED2/RB0
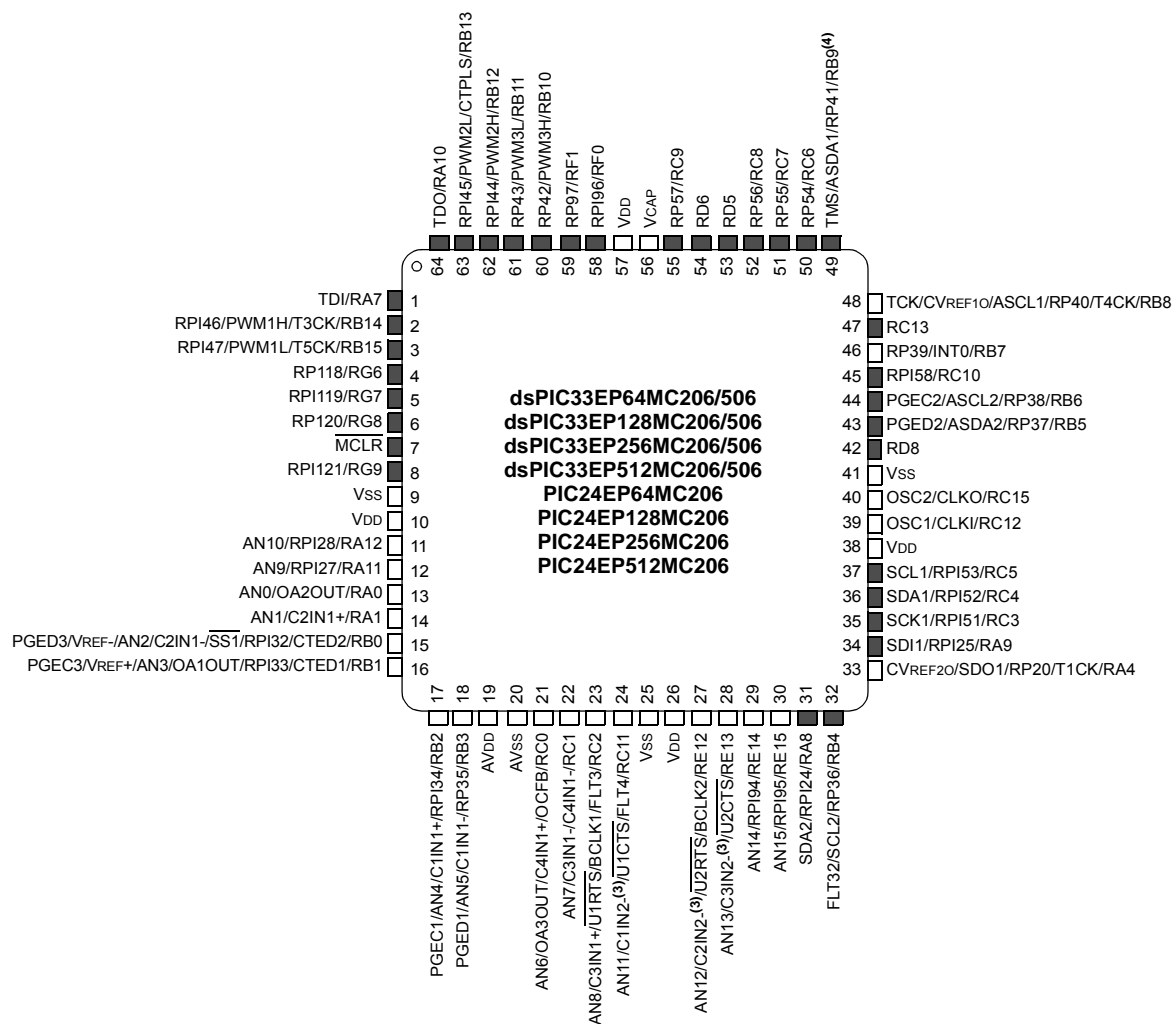- 22: PGEC3/VREF+/AN3/OA1OUT/RPI33/CTED1/RB1

Note 1: The RPn/RPIn pins can be used by any remappable peripheral with some limitation. See **Section 11.4 "Peripheral Pin Select (PPS)"** for available peripherals and for information on limitations.

2: Every I/O port pin (RAx-RGx) can be used as a Change Notification pin (CNAx-CNGx). See **Section 11.0 "I/O Ports"** for more information.

3: The metal pad at the bottom of the device is not connected to any pins and is recommended to be connected to VSS externally.

4: There is an internal pull-up resistor connected to the TMS pin when the JTAG interface is active. See the JTAGEN bit field in Table 27-2.
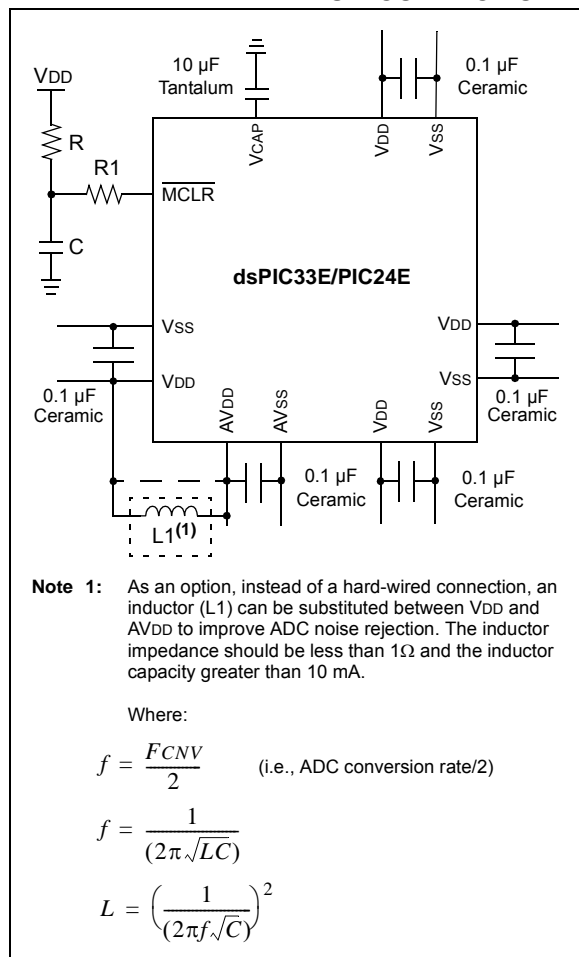
Pin Diagrams (Continued)

64-Pin TQFP[1,2,3]

■ = Pins are up to 5V tolerant

Top pins (left to right, 64–49):
64 TDO/RA10
63 RPI45/PWM2L/CTPLS/RB13
62 RPI44/PWM2H/RB12
61 RP43/PWM3L/RB11
60 RP42/PWM3H/RB10
59 RP97/RF1
58 RPI96/RF0
57 VDD
56 VCAP
55 RP57/RC9
54 RD6
53 RD5
52 RP56/RC8
51 RP55/RC7
50 RP54/RC6
49 TMS/ASDA1/RP41/RB9[4]

Left pins (1–16):
1 TDI/RA7
2 RPI46/PWM1H/T3CK/RB14
3 RPI47/PWM1L/T5CK/RB15
4 RP118/RG6
5 RPI119/RG7
6 RP120/RG8
7 MCLR
8 RPI121/RG9
9 VSS
10 VDD
11 AN10/RPI28/RA12
12 AN9/RPI27/RA11
13 AN0/OA2OUT/RA0
14 AN1/C2IN1+/RA1
15 PGED3/VREF-/AN2/C2IN1-/SS1/RPI32/CTED2/RB0
16 PGEC3/VREF+/AN3/OA1OUT/RPI33/CTED1/RB1

Right pins (48–33):
48 TCK/CVREF1O/ASCL1/RP40/T4CK/RB8
47 RC13
46 RP39/INT0/RB7
45 RPI58/RC10
44 PGEC2/ASCL2/RP38/RB6
43 PGED2/ASDA2/RP37/RB5
42 RD8
41 VSS
40 OSC2/CLKO/RC15
39 OSC1/CLKI/RC12
38 VDD
37 SCL1/RPI53/RC5
36 SDA1/RPI52/RC4
35 SCK1/RPI51/RC3
34 SDI1/RPI25/RA9
33 CVREF2O/SDO1/RP20/T1CK/RA4

Center device labels:
dsPIC33EP64MC206/506
dsPIC33EP128MC206/506
dsPIC33EP256MC206/506
dsPIC33EP512MC206/506
PIC24EP64MC206
PIC24EP128MC206
PIC24EP256MC206
PIC24EP512MC206

Bottom pins (17–32):
17 PGEC1/AN4/C1IN1+/RPI34/RB2
18 PGED1/AN5/C1IN1-/RP35/RB3
19 AVDD
20 AVSS
21 AN6/OA3OUT/C4IN1+/OCFB/RC0
22 AN7/C3IN1-/C4IN1-/RC1
23 AN8/C3IN1+/U1RTS/BCLK1/FLT3/RC2
24 AN11/C1IN2-/U1CTS/FLT4/RC11
25 VSS
26 VDD
27 AN12/C2IN2-/U2RTS/BCLK2/RE12
28 AN13/C3IN2-/U2CTS/RE13
29 AN14/RPI94/RE14
30 AN15/RPI95/RE15
31 SDA2/RPI24/RA8
32 FLT32/SCL2/RP36/RB4

Note 1: The RPn/RPIn pins can be used by any remappable peripheral with some limitation. See **Section 11.4 "Peripheral Pin Select (PPS)"** for available peripherals and for information on limitations.

2: Every I/O port pin (RAx-RGx) can be used as a Change Notification pin (CNAx-CNGx). See **Section 11.0 "I/O Ports"** for more information.

3: The metal pad at the bottom of the device is not connected to any pins and is recommended to be connected to Vss externally.

4: There is an internal pull-up resistor connected to the TMS pin when the JTAG interface is active. See the JTAGEN bit field in Table 27-2.

FIGURE 2-1: **RECOMMENDED MINIMUM CONNECTION**

Note 1: As an option, instead of a hard-wired connection, an inductor (L1) can be substituted between V_{DD} and AV_{DD} to improve ADC noise rejection. The inductor impedance should be less than 1Ω and the inductor capacity greater than 10 mA.

Where:

$$f = \frac{FCNV}{2} \qquad \text{(i.e., ADC conversion rate/2)}$$

$$f = \frac{1}{(2\pi\sqrt{LC})}$$

$$L = \left(\frac{1}{(2\pi f\sqrt{C})}\right)^2$$

2.2.1   TANK CAPACITORS

On boards with power traces running longer than six inches in length, it is suggested to use a tank capacitor for integrated circuits including DSCs to supply a local power source. The value of the tank capacitor should be determined based on the trace resistance that connects the power supply source to the device and the maximum current drawn by the device in the application. In other words, select the tank capacitor so that it meets the acceptable voltage sag at the device. Typical values range from 4.7 µF to 47 µF.

2.3   CPU Logic Filter Capacitor Connection (V_{CAP})

A low-ESR (< 1 Ohm) capacitor is required on the V_{CAP} pin, which is used to stabilize the voltage regulator output voltage. The V_{CAP} pin must not be connected to V_{DD} and must have a capacitor greater than 4.7 µF (10 µF is recommended), 16V connected to ground. The type can be ceramic or tantalum. See **Section 30.0 "Electrical Characteristics"** for additional information.

The placement of this capacitor should be close to the V_{CAP} pin. It is recommended that the trace length not exceeds one-quarter inch (6 mm). See **Section 27.3 "On-Chip Voltage Regulator"** for details.

2.4   Master Clear (MCLR) Pin

The MCLR pin provides two specific device functions:

• Device Reset
• Device Programming and Debugging.

During device programming and debugging, the resistance and capacitance that can be added to the pin must be considered. Device programmers and debuggers drive the MCLR pin. Consequently, specific voltage levels (V_{IH} and V_{IL}) and fast signal transitions must not be adversely affected. Therefore, specific values of R and C will need to be adjusted based on the application and PCB requirements.

For example, as shown in Figure 2-2, it is recommended that the capacitor, C, be isolated from the MCLR pin during programming and debugging operations.

Place the components as shown in Figure 2-2 within one-quarter inch (6 mm) from the MCLR pin.

FIGURE 2-2: **EXAMPLE OF MCLR PIN CONNECTIONS**

Note 1: R ≤ 10 kΩ is recommended. A suggested starting value is 10 kΩ. Ensure that the MCLR pin V_{IH} and V_{IL} specifications are met.

2: R1 ≤ 470Ω will limit any current flowing into MCLR from the external capacitor, C, in the event of MCLR pin breakdown, due to Electrostatic Discharge (ESD) or Electrical Overstress (EOS). Ensure that the MCLR pin V_{IH} and V_{IL} specifications are met.
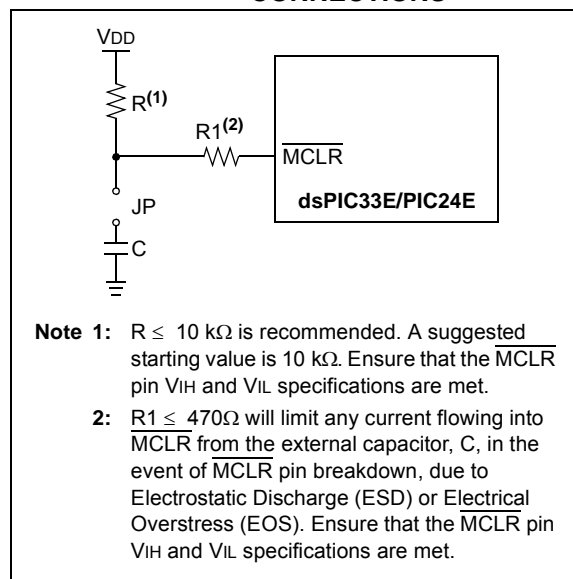
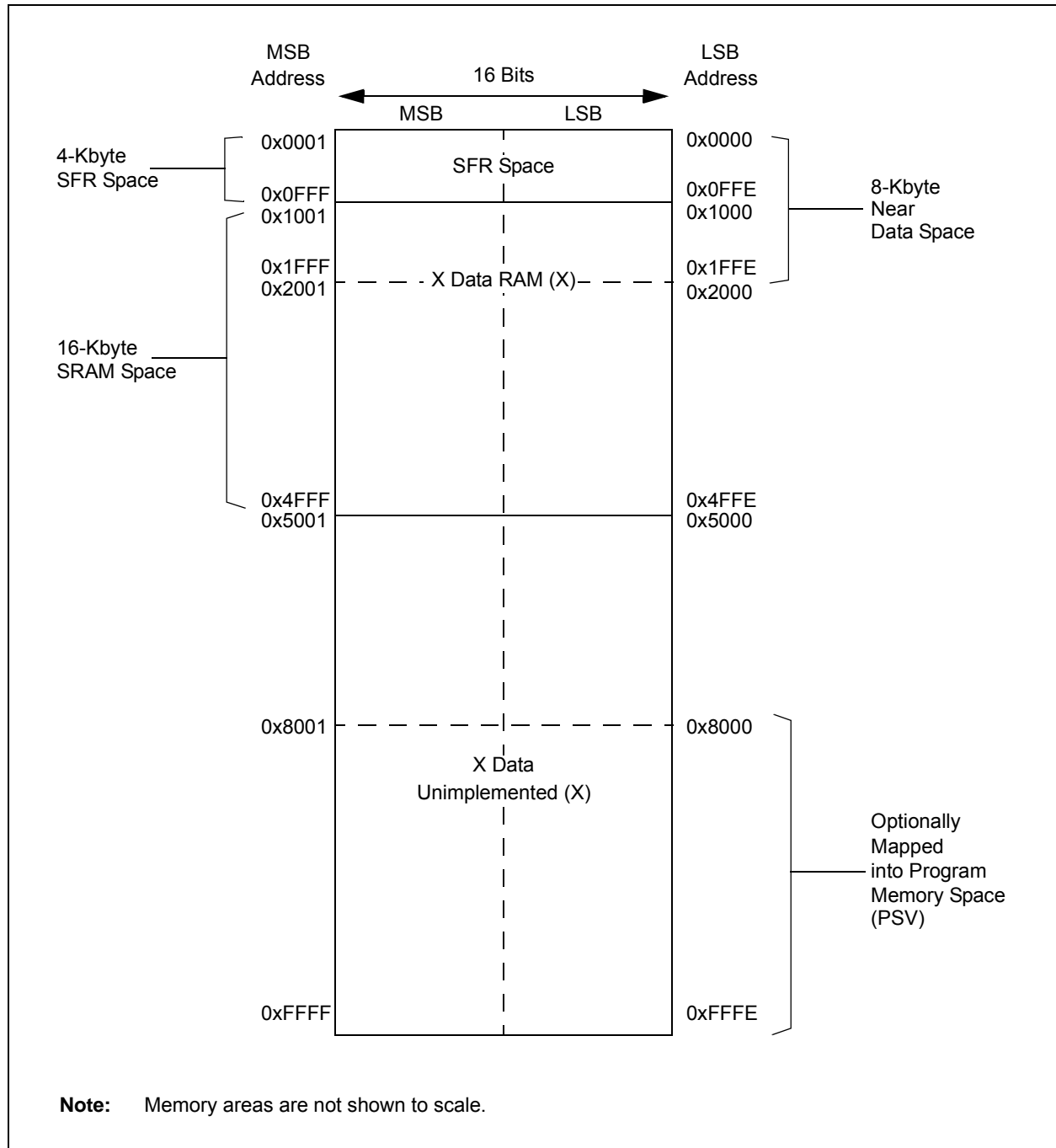**FIGURE 4-14:   DATA MEMORY MAP FOR PIC24EP128GP/MC20X/50X DEVICES**

TABLE 4-53: PORTA REGISTER MAP FOR PIC24EPXXXGP/MC204 AND dsPIC33EPXXXGP/MC204/504 DEVICES ONLY

File Name	Addr.	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	All Resets
TRISA	0E00	—	—	—	—	—	TRISA10	TRISA9	TRISA8	TRISA7	—	—	TRISA4	TRISA3	TRISA2	TRISA1	TRISA0	079F
PORTA	0E02	—	—	—	—	—	RA10	RA9	RA8	RA7	—	—	RA4	RA3	RA2	RA1	RA0	0000
LATA	0E04	—	—	—	—	—	LATA10	LATA9	LATA8	LATA7	—	—	LATA4	LATA3	LATA2	LA1TA1	LA0TA0	0000
ODCA	0E06	—	—	—	—	—	ODCA10	ODCA9	ODCA8	ODCA7	—	—	ODCA4	ODCA3	ODCA2	ODCA1	ODCA0	0000
CNENA	0E08	—	—	—	—	—	CNIEA10	CNIEA9	CNIEA8	CNIEA7	—	—	CNIEA4	CNIEA3	CNIEA2	CNIEA1	CNIEA0	0000
CNPUA	0E0A	—	—	—	—	—	CNPUA10	CNPUA9	CNPUA8	CNPUA7	—	—	CNPUA4	CNPUA3	CNPUA2	CNPUA1	CNPUA0	0000
CNPDA	0E0C	—	—	—	—	—	CNPDA10	CNPDA9	CNPDA8	CNPDA7	—	—	CNPDA4	CNPDA3	CNPDA2	CNPDA1	CNPDA0	0000
ANSELA	0E0E	—	—	—	—	—	—	—	—	—	—	—	ANSA4	—	—	ANSA1	ANSA0	0013

Legend: — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

TABLE 4-54: PORTB REGISTER MAP FOR PIC24EPXXXGP/MC204 AND dsPIC33EPXXXGP/MC204/504 DEVICES ONLY

File Name	Addr.	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	All Resets
TRISB	0E10	TRISB15	TRISB14	TRISB13	TRISB12	TRISB11	TRISB10	TRISB9	TRISB8	TRISB7	TRISB6	TRISB5	TRISB4	TRISB3	TRISB2	TRISB1	TRISB0	FFFF
PORTB	0E12	RB15	RB14	RB13	RB12	RB11	RB10	RB9	RB8	RB7	RB6	RB5	RB4	RB3	RB2	RB1	RB0	xxxx
LATB	0E14	LATB15	LATB14	LATB13	LATB12	LATB11	LATB10	LATB9	LATB8	LATB7	LATB6	LATB5	LATB4	LATB3	LATB2	LATB1	LATB0	xxxx
ODCB	0E16	ODCB15	ODCB14	ODCB13	ODCB12	ODCB11	ODCB10	ODCB9	ODCB8	ODCB7	ODCB6	ODCB5	ODCB4	ODCB3	ODCB2	ODCB1	ODCB0	0000
CNENB	0E18	CNIEB15	CNIEB14	CNIEB13	CNIEB12	CNIEB11	CNIEB10	CNIEB9	CNIEB8	CNIEB7	CNIEB6	CNIEB5	CNIEB4	CNIEB3	CNIEB2	CNIEB1	CNIEB0	0000
CNPUB	0E1A	CNPUB15	CNPUB14	CNPUB13	CNPUB12	CNPUB11	CNPUB10	CNPUB9	CNPUB8	CNPUB7	CNPUB6	CNPUB5	CNPUB4	CNPUB3	CNPUB2	CNPUB1	CNPUB0	0000
CNPDB	0E1C	CNPDB15	CNPDB14	CNPDB13	CNPDB12	CNPDB11	CNPDB10	CNPDB9	CNPDB8	CNPDB7	CNPDB6	CNPDB5	CNPDB4	CNPDB3	CNPDB2	CNPDB1	CNPDB0	0000
ANSELB	0E1E	—	—	—	—	—	—	—	ANSB8	—	—	—	—	ANSB3	ANSB2	ANSB1	ANSB0	010F

Legend: x = unknown value on Reset, — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

TABLE 4-55: PORTC REGISTER MAP FOR PIC24EPXXXGP/MC204 AND dsPIC33EPXXXGP/MC204/504 DEVICES ONLY

File Name	Addr.	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	All Resets
TRISC	0E20	—	—	—	—	—	—	TRISC9	TRISC8	TRISC7	TRISC6	TRISC5	TRISC4	TRISC3	TRISC2	TRISC1	TRISC0	03FF
PORTC	0E22	—	—	—	—	—	—	RC9	RC8	RC7	RC6	RC5	RC4	RC3	RC2	RC1	RC0	xxxx
LATC	0E24	—	—	—	—	—	—	LATC9	LATC8	LATC7	LATC6	LATC5	LATC4	LATC3	LATC2	LATC1	LATC0	xxxx
ODCC	0E26	—	—	—	—	—	—	ODCC9	ODCC8	ODCC7	ODCC6	ODCC5	ODCC4	ODCC3	ODCC2	ODCC1	ODCC0	0000
CNENC	0E28	—	—	—	—	—	—	CNIEC9	CNIEC8	CNIEC7	CNIEC6	CNIEC5	CNIEC4	CNIEC3	CNIEC2	CNIEC1	CNIEC0	0000
CNPUC	0E2A	—	—	—	—	—	—	CNPUC9	CNPUC8	CNPUC7	CNPUC6	CNPUC5	CNPUC4	CNPUC3	CNPUC2	CNPUC1	CNPUC0	0000
CNPDC	0E2C	—	—	—	—	—	—	CNPDC9	CNPDC8	CNPDC7	CNPDC6	CNPDC5	CNPDC4	CNPDC3	CNPDC2	CNPDC1	CNPDC0	0000
ANSELC	0E2E	—	—	—	—	—	—	—	—	—	—	—	—	—	ANSC2	ANSC1	ANSC0	0007

Legend: x = unknown value on Reset, — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

Allocating different Page registers for read and write access allows the architecture to support data movement between different pages in data memory. This is accomplished by setting the DSRPAG register value to the page from which you want to read, and configuring the DSWPAG register to the page to which it needs to be written. Data can also be moved from different PSV to EDS pages, by configuring the DSRPAG and DSWPAG registers to address PSV and EDS space, respectively. The data can be moved between pages by a single instruction.

When an EDS or PSV page overflow or underflow occurs, EA<15> is cleared as a result of the register indirect EA calculation. An overflow or underflow of the EA in the EDS or PSV pages can occur at the page boundaries when:

• The initial address prior to modification addresses an EDS or PSV page
• The EA calculation uses Pre-Modified or Post-Modified Register Indirect Addressing; however, this does not include Register Offset Addressing

In general, when an overflow is detected, the DSxPAG register is incremented and the EA<15> bit is set to keep the base address within the EDS or PSV window. When an underflow is detected, the DSxPAG register is decremented and the EA<15> bit is set to keep the base address within the EDS or PSV window. This creates a linear EDS and PSV address space, but only when using Register Indirect Addressing modes.

Exceptions to the operation described above arise when entering and exiting the boundaries of Page 0, EDS and PSV spaces. Table 4-61 lists the effects of overflow and underflow scenarios at different boundaries.

In the following cases, when overflow or underflow occurs, the EA<15> bit is set and the DSxPAG is not modified; therefore, the EA will wrap to the beginning of the current page:

• Register Indirect with Register Offset Addressing
• Modulo Addressing
• Bit-Reversed Addressing

TABLE 4-61: OVERFLOW AND UNDERFLOW SCENARIOS AT PAGE 0, EDS and PSV SPACE BOUNDARIES[(2,3,4)]

O/U, R/W	Operation	Before			After		
		DSxPAG	**DS EA<15>**	**Page Description**	**DSxPAG**	**DS EA<15>**	**Page Description**
O, Read	`[++Wn]` or `[Wn++]`	DSRPAG = 0x1FF	1	EDS: Last page	DSRPAG = 0x1FF	0	See **Note 1**
O, Read		DSRPAG = 0x2FF	1	PSV: Last lsw page	DSRPAG = 0x300	1	PSV: First MSB page
O, Read		DSRPAG = 0x3FF	1	PSV: Last MSB page	DSRPAG = 0x3FF	0	See **Note 1**
O, Write		DSWPAG = 0x1FF	1	EDS: Last page	DSWPAG = 0x1FF	0	See **Note 1**
U, Read	`[--Wn]` or `[Wn--]`	DSRPAG = 0x001	1	PSV page	DSRPAG = 0x001	0	See **Note 1**
U, Read		DSRPAG = 0x200	1	PSV: First lsw page	DSRPAG = 0x200	0	See **Note 1**
U, Read		DSRPAG = 0x300	1	PSV: First MSB page	DSRPAG = 0x2FF	1	PSV: Last lsw page

Legend: O = Overflow, U = Underflow, R = Read, W = Write

Note 1: The Register Indirect Addressing now addresses a location in the base Data Space (0x0000-0x8000).

2: An EDS access with DSxPAG = 0x000 will generate an address error trap.

3: Only reads from PS are supported using DSRPAG. An attempt to write to PS using DSWPAG will generate an address error trap.

4: Pseudo-Linear Addressing is not supported for large offsets.

4.5 Instruction Addressing Modes

The addressing modes shown in Table 4-63 form the basis of the addressing modes optimized to support the specific features of individual instructions. The addressing modes provided in the MAC class of instructions differ from those in the other instruction types.

4.5.1 FILE REGISTER INSTRUCTIONS

Most file register instructions use a 13-bit address field (f) to directly address data present in the first 8192 bytes of data memory (Near Data Space). Most file register instructions employ a working register, W0, which is denoted as WREG in these instructions. The destination is typically either the same file register or WREG (with the exception of the MUL instruction), which writes the result to a register or register pair. The MOV instruction allows additional flexibility and can access the entire Data Space.

4.5.2 MCU INSTRUCTIONS

The three-operand MCU instructions are of the form:

`Operand 3 = Operand 1 <function> Operand 2`

where Operand 1 is always a working register (that is, the addressing mode can only be Register Direct), which is referred to as Wb. Operand 2 can be a W register fetched from data memory or a 5-bit literal. The result location can either be a W register or a data memory location. The following addressing modes are supported by MCU instructions:

- Register Direct
- Register Indirect
- Register Indirect Post-Modified
- Register Indirect Pre-Modified
- 5-Bit or 10-Bit Literal

Note:	Not all instructions support all the addressing modes given above. Individual instructions can support different subsets of these addressing modes.

TABLE 4-63: FUNDAMENTAL ADDRESSING MODES SUPPORTED

Addressing Mode	Description
File Register Direct	The address of the file register is specified explicitly.
Register Direct	The contents of a register are accessed directly.
Register Indirect	The contents of Wn form the Effective Address (EA).
Register Indirect Post-Modified	The contents of Wn form the EA. Wn is post-modified (incremented or decremented) by a constant value.
Register Indirect Pre-Modified	Wn is pre-modified (incremented or decremented) by a signed constant value to form the EA.
Register Indirect with Register Offset (Register Indexed)	The sum of Wn and Wb forms the EA.
Register Indirect with Literal Offset	The sum of Wn and a literal forms the EA.

7.0 INTERRUPT CONTROLLER

> **Note 1:** This data sheet summarizes the features of the dsPIC33EPXXXGP50X, dsPIC33EPXXXMC20X/50X and PIC24EPXXXGP/MC20X families of devices. It is not intended to be a comprehensive reference source. To complement the information in this data sheet, refer to **"Interrupts"** (DS70600) in the "*dsPIC33/PIC24 Family Reference Manual"*, which is available from the Microchip web site (www.microchip.com).
>
> **2:** Some registers and associated bits described in this section may not be available on all devices. Refer to **Section 4.0 "Memory Organization"** in this data sheet for device-specific register and bit information.

The dsPIC33EPXXXGP50X, dsPIC33EPXXXMC20X/50X and PIC24EPXXXGP/MC20X interrupt controller reduces the numerous peripheral interrupt request signals to a single interrupt request signal to the dsPIC33EPXXXGP50X, dsPIC33EPXXXMC20X/50X and PIC24EPXXXGP/MC20X CPU.

The interrupt controller has the following features:

- Up to eight processor exceptions and software traps
- Eight user-selectable priority levels
- Interrupt Vector Table (IVT) with a unique vector for each interrupt or exception source
- Fixed priority within a specified user priority level
- Fixed interrupt entry and return latencies

7.1 Interrupt Vector Table

The dsPIC33EPXXXGP50X, dsPIC33EPXXXMC20X/50X and PIC24EPXXXGP/MC20X Interrupt Vector Table (IVT), shown in Figure 7-1, resides in program memory starting at location, 000004h. The IVT contains seven non-maskable trap vectors and up to 246 sources of interrupt. In general, each interrupt source has its own vector. Each interrupt vector contains a 24-bit-wide address. The value programmed into each interrupt vector location is the starting address of the associated Interrupt Service Routine (ISR).

Interrupt vectors are prioritized in terms of their natural priority. This priority is linked to their position in the vector table. Lower addresses generally have a higher natural priority. For example, the interrupt associated with Vector 0 takes priority over interrupts at any other vector address.

7.2 Reset Sequence

A device Reset is not a true exception because the interrupt controller is not involved in the Reset process. The dsPIC33EPXXXGP50X, dsPIC33EPXXXMC20X/50X and PIC24EPXXXGP/MC20X devices clear their registers in response to a Reset, which forces the PC to zero. The device then begins program execution at location, 0x000000. A GOTO instruction at the Reset address can redirect program execution to the appropriate start-up routine.

> **Note:** Any unimplemented or unused vector locations in the IVT should be programmed with the address of a default interrupt handler routine that contains a RESET instruction.

REGISTER 10-5: PMD6: PERIPHERAL MODULE DISABLE CONTROL REGISTER 6

U-0	U-0	U-0	U-0	U-0	R/W-0	R/W-0	R/W-0
—	—	—	—	—	PWM3MD[(1)]	PWM2MD[(1)]	PWM1MD[(1)]
bit 15							bit 8

U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
—	—	—	—	—	—	—	—
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15-11 **Unimplemented:** Read as '0'

bit 10 **PWM3MD:** PWM3 Module Disable bit[(1)]

1 = PWM3 module is disabled
0 = PWM3 module is enabled

bit 9 **PWM2MD:** PWM2 Module Disable bit[(1)]

1 = PWM2 module is disabled
0 = PWM2 module is enabled

bit 8 **PWM1MD:** PWM1 Module Disable bit[(1)]

1 = PWM1 module is disabled
0 = PWM1 module is enabled

bit 7-0 **Unimplemented:** Read as '0'

Note 1: This bit is available on dsPIC33EPXXXMC50X/20X and PIC24EPXXXMC20X devices only.

TABLE 11-2:   INPUT PIN SELECTION FOR SELECTABLE INPUT SOURCES (CONTINUED)

Peripheral Pin Select Input Register Value	Input/Output	Pin Assignment	Peripheral Pin Select Input Register Value	Input/Output	Pin Assignment
010 1000	I/O	RP40	101 0101	—	—
010 1001	I/O	RP41	101 0110	—	—
010 1010	I/O	RP42	101 0111	—	—
010 1011	I/O	RP43	101 1000	—	—
010 1100	I	RPI44	101 1001	—	—
101 1010	—	—	110 1101	—	—
101 1011	—	—	110 1110	—	—
101 1100	—	—	110 1111	—	—
101 1101	—	—	111 0000	—	—
101 1110	I	RPI94	111 0001	—	—
101 1111	I	RPI95	111 0010	—	—
110 0000	I	RPI96	111 0011	—	—
110 0001	I/O	RP97	111 0100	—	—
110 0010	—	—	111 0101	—	—
110 0011	—	—	111 0110	I/O	RP118
110 0100	—	—	111 0111	I	RPI119
110 0101	—	—	111 1000	I/O	RP120
110 0110	—	—	111 1001	I	RPI121
110 0111	—	—	111 1010	—	—
110 1000	—	—	111 1011	—	—
110 1001	—	—	111 1100	—	—
110 1010	—	—	111 1101	—	—
110 1011	—	—	111 1110	—	—
110 1100	—	—	111 1111	—	—

Legend: Shaded rows indicate PPS Input register values that are unimplemented.

Note 1: See **Section 11.4.4.1 "Virtual Connections"** for more information on selecting this pin assignment.

2: These inputs are available on dsPIC33EPXXXGP/MC50X devices only.

REGISTER 11-22:   RPOR4: PERIPHERAL PIN SELECT OUTPUT REGISTER 4

U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
—	—	RP43R<5:0>					

bit 15   bit 8

U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
—	—	RP42R<5:0>					

bit 7   bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15-14   **Unimplemented:** Read as '0'

bit 13-8   **RP43R<5:0>:** Peripheral Output Function is Assigned to RP43 Output Pin bits
(see Table 11-3 for peripheral function numbers)

bit 7-6   **Unimplemented:** Read as '0'

bit 5-0   **RP42R<5:0>:** Peripheral Output Function is Assigned to RP42 Output Pin bits
(see Table 11-3 for peripheral function numbers)

REGISTER 11-23:   RPOR5: PERIPHERAL PIN SELECT OUTPUT REGISTER 5

U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
—	—	RP55R<5:0>					

bit 15   bit 8

U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
—	—	RP54R<5:0>					

bit 7   bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15-14   **Unimplemented:** Read as '0'

bit 13-8   **RP55R<5:0>:** Peripheral Output Function is Assigned to RP55 Output Pin bits
(see Table 11-3 for peripheral function numbers)

bit 7-6   **Unimplemented:** Read as '0'

bit 5-0   **RP54R<5:0>:** Peripheral Output Function is Assigned to RP54 Output Pin bits
(see Table 11-3 for peripheral function numbers)

REGISTER 16-1:   PTCON: PWMx TIME BASE CONTROL REGISTER (CONTINUED)

bit 6-4   **SYNCSRC<2:0>:** Synchronous Source Selection bits[1]

   111 = Reserved
   •
   •
   •
   100 = Reserved
   011 = PTGO17[2]
   010 = PTGO16[2]
   001 = Reserved
   000 = SYNCI1 input from PPS

bit 3-0   **SEVTPS<3:0>:** PWMx Special Event Trigger Output Postscaler Select bits[1]

   1111 = 1:16 Postscaler generates Special Event Trigger on every sixteenth compare match event
   •
   •
   •
   0001 = 1:2 Postscaler generates Special Event Trigger on every second compare match event
   0000 = 1:1 Postscaler generates Special Event Trigger on every compare match event

Note 1:   These bits should be changed only when PTEN = 0. In addition, when using the SYNCI1 feature, the user
            application must program the period register with a value that is slightly larger than the expected period of
            the external synchronization input signal.

   2:   See **Section 24.0 "Peripheral Trigger Generator (PTG) Module"** for information on this selection.

REGISTER 17-3:   QEI1STAT: QEI1 STATUS REGISTER (CONTINUED)

bit 2   **HOMIEN:** Home Input Event Interrupt Enable bit

1 = Interrupt is enabled
0 = Interrupt is disabled

bit 1   **IDXIRQ:** Status Flag for Index Event Status bit

1 = Index event has occurred
0 = No Index event has occurred

bit 0   **IDXIEN:** Index Input Event Interrupt Enable bit

1 = Interrupt is enabled
0 = Interrupt is disabled

Note 1:   This status bit is only applicable to PIMOD<2:0> modes, '011' and '100'.

REGISTER 20-2:   UxSTA: UARTx STATUS AND CONTROL REGISTER (CONTINUED)

bit 5   **ADDEN:** Address Character Detect bit (bit 8 of received data = 1)

                1 = Address Detect mode is enabled; if 9-bit mode is not selected, this does not take effect
                0 = Address Detect mode is disabled

bit 4   **RIDLE:** Receiver Idle bit (read-only)

                1 = Receiver is Idle
                0 = Receiver is active

bit 3   **PERR:** Parity Error Status bit (read-only)

                1 = Parity error has been detected for the current character (character at the top of the receive FIFO)
                0 = Parity error has not been detected

bit 2   **FERR:** Framing Error Status bit (read-only)

                1 = Framing error has been detected for the current character (character at the top of the receive FIFO)
                0 = Framing error has not been detected

bit 1   **OERR:** Receive Buffer Overrun Error Status bit (clear/read-only)

                1 = Receive buffer has overflowed
                0 = Receive buffer has not overflowed; clearing a previously set OERR bit ($1 \rightarrow 0$ transition) resets the receiver buffer and the UxRSR to the empty state

bit 0   **URXDA:** UARTx Receive Buffer Data Available bit (read-only)

                1 = Receive buffer has data, at least one more character can be read
                0 = Receive buffer is empty

Note 1:   Refer to the **"UART"** (DS70582) section in the *"dsPIC33/PIC24 Family Reference Manual"* for information on enabling the UARTx module for transmit operation.

REGISTER 21-8:   CxEC: ECANx TRANSMIT/RECEIVE ERROR COUNT REGISTER

R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0
TERRCNT<7:0>							
bit 15							bit 8

R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0
RERRCNT<7:0>							
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15-8   **TERRCNT<7:0>:** Transmit Error Count bits

bit 7-0   **RERRCNT<7:0>:** Receive Error Count bits

REGISTER 21-9:   CxCFG1: ECANx BAUD RATE CONFIGURATION REGISTER 1

U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
—	—	—	—	—	—	—	—
bit 15							bit 8

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
SJW1	SJW0	BRP5	BRP4	BRP3	BRP2	BRP1	BRP0
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15-8   **Unimplemented:** Read as '0'

bit 7-6   **SJW<1:0>:** Synchronization Jump Width bits

             11 = Length is 4 x TQ
             10 = Length is 3 x TQ
             01 = Length is 2 x TQ
             00 = Length is 1 x TQ

bit 5-0   **BRP<5:0>:** Baud Rate Prescaler bits

             11 1111 = TQ = 2 x 64 x 1/FCAN
             •
             •
             •
             00 0010 = TQ = 2 x 3 x 1/FCAN
             00 0001 = TQ = 2 x 2 x 1/FCAN
             00 0000 = TQ = 2 x 1 x 1/FCAN

REGISTER 21-11:   CxFEN1: ECANx ACCEPTANCE FILTER ENABLE REGISTER 1

R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1
FLTEN15	FLTEN14	FLTEN13	FLTEN12	FLTEN11	FLTEN10	FLTEN9	FLTEN8
bit 15							bit 8

R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1
FLTEN7	FLTEN6	FLTEN5	FLTEN4	FLTEN3	FLTEN2	FLTEN1	FLTEN0
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15-0   **FLTEN<15:0>:** Enable Filter n to Accept Messages bits

1 = Enables Filter n
0 = Disables Filter n

REGISTER 21-12:   CxBUFPNT1: ECANx FILTER 0-3 BUFFER POINTER REGISTER 1

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
F3BP<3:0>				F2BP<3:0>			
bit 15							bit 8

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
F1BP<3:0>				F0BP<3:0>			
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15-12   **F3BP<3:0>:** RX Buffer Mask for Filter 3 bits

1111 = Filter hits received in RX FIFO buffer
1110 = Filter hits received in RX Buffer 14
•
•
•
0001 = Filter hits received in RX Buffer 1
0000 = Filter hits received in RX Buffer 0

bit 11-8   **F2BP<3:0>:** RX Buffer Mask for Filter 2 bits (same values as bits<15:12>)

bit 7-4   **F1BP<3:0>:** RX Buffer Mask for Filter 1 bits (same values as bits<15:12>)

bit 3-0   **F0BP<3:0>:** RX Buffer Mask for Filter 0 bits (same values as bits<15:12>)

25.3   Op Amp/Comparator Registers

REGISTER 25-1:   CMSTAT: OP AMP/COMPARATOR STATUS REGISTER

R/W-0	U-0	U-0	U-0	R-0	R-0	R-0	R-0
PSIDL	—	—	—	C4EVT[1]	C3EVT[1]	C2EVT[1]	C1EVT[1]
bit 15							bit 8

U-0	U-0	U-0	U-0	R-0	R-0	R-0	R-0
—	—	—	—	C4OUT[2]	C3OUT[2]	C2OUT[2]	C1OUT[2]
bit 7							bit 0

Legend:		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared x = Bit is unknown

bit 15 **PSIDL:** Comparator Stop in Idle Mode bit

1 = Discontinues operation of all comparators when device enters Idle mode
0 = Continues operation of all comparators in Idle mode

bit 14-12 **Unimplemented:** Read as '0'

bit 11 **C4EVT:** Op Amp/Comparator 4 Event Status bit[1]

1 = Op amp/comparator event occurred
0 = Op amp/comparator event did not occur

bit 10 **C3EVT:** Comparator 3 Event Status bit[1]

1 = Comparator event occurred
0 = Comparator event did not occur

bit 9 **C2EVT:** Comparator 2 Event Status bit[1]

1 = Comparator event occurred
0 = Comparator event did not occur

bit 8 **C1EVT:** Comparator 1 Event Status bit[1]

1 = Comparator event occurred
0 = Comparator event did not occur

bit 7-4 **Unimplemented:** Read as '0'

bit 3 **C4OUT:** Comparator 4 Output Status bit[2]

When CPOL = 0:
1 = $V_{IN}+ > V_{IN}-$
0 = $V_{IN}+ < V_{IN}-$

When CPOL = 1:
1 = $V_{IN}+ < V_{IN}-$
0 = $V_{IN}+ > V_{IN}-$

bit 2 **C3OUT:** Comparator 3 Output Status bit[2]

When CPOL = 0:
1 = $V_{IN}+ > V_{IN}-$
0 = $V_{IN}+ < V_{IN}-$

When CPOL = 1:
1 = $V_{IN}+ < V_{IN}-$
0 = $V_{IN}+ > V_{IN}-$

Note 1: Reflects the value of the of the CEVT bit in the respective Op Amp/Comparator Control register, CMxCON<9>.

2: Reflects the value of the COUT bit in the respective Op Amp/Comparator Control register, CMxCON<8>.

**TABLE 30-47: SPI1 SLAVE MODE (FULL-DUPLEX, CKE = 0, CKP = 1, SMP = 0)
TIMING REQUIREMENTS**

AC CHARACTERISTICS			Standard Operating Conditions: 3.0V to 3.6V (unless otherwise stated) Operating temperature -40°C ≤ TA ≤ +85°C for Industrial -40°C ≤ TA ≤ +125°C for Extended				
Param.	Symbol	Characteristic[1]	Min.	Typ.[2]	Max.	Units	Conditions
SP70	FscP	Maximum SCK1 Input Frequency	—	—	15	MHz	(Note 3)
SP72	TscF	SCK1 Input Fall Time	—	—	—	ns	See Parameter DO32 (Note 4)
SP73	TscR	SCK1 Input Rise Time	—	—	—	ns	See Parameter DO31 (Note 4)
SP30	TdoF	SDO1 Data Output Fall Time	—	—	—	ns	See Parameter DO32 (Note 4)
SP31	TdoR	SDO1 Data Output Rise Time	—	—	—	ns	See Parameter DO31 (Note 4)
SP35	TscH2doV, TscL2doV	SDO1 Data Output Valid after SCK1 Edge	—	6	20	ns	
SP36	TdoV2scH, TdoV2scL	SDO1 Data Output Setup to First SCK1 Edge	30	—	—	ns	
SP40	TdiV2scH, TdiV2scL	Setup Time of SDI1 Data Input to SCK1 Edge	30	—	—	ns	
SP41	TscH2diL, TscL2diL	Hold Time of SDI1 Data Input to SCK1 Edge	30	—	—	ns	
SP50	TssL2scH, TssL2scL	$\overline{SS1}$ ↓ to SCK1 ↑ or SCK1 ↓ Input	120	—	—	ns	
SP51	TssH2doZ	$\overline{SS1}$ ↑ to SDO1 Output High-Impedance	10	—	50	ns	(Note 4)
SP52	TscH2ssH, TscL2ssH	$\overline{SS1}$ ↑ after SCK1 Edge	1.5 TCY + 40	—	—	ns	(Note 4)

Note 1: These parameters are characterized, but are not tested in manufacturing.

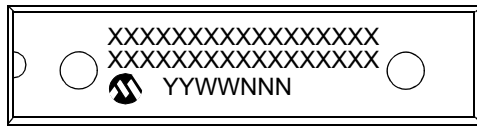**2:** Data in "Typical" column is at 3.3V, +25°C unless otherwise stated.

3: The minimum clock period for SCK1 is 66.7 ns. Therefore, the SCK1 clock generated by the master must not violate this specification.
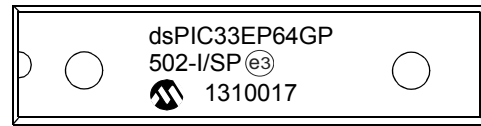
4: Assumes 50 pF load on all SPI1 pins.

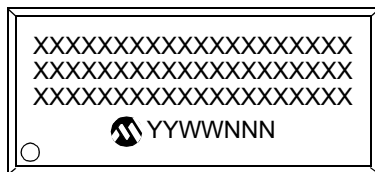## 33.0 PACKAGING INFORMATION

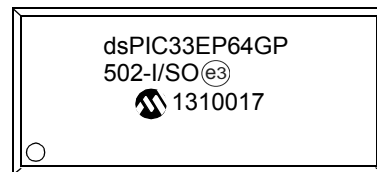### 33.1 Package Marking Information

28-Lead SPDIP

```
XXXXXXXXXXXXXXX
XXXXXXXXXXXXXXX
      YYWWNNN
```

Example

```
dsPIC33EP64GP
502-I/SP (e3)
      1310017
```

28-Lead SOIC (.300")

```
XXXXXXXXXXXXXXXXXXX
XXXXXXXXXXXXXXXXXXX
XXXXXXXXXXXXXXXXXXX
      YYWWNNN
```

Example

```
dsPIC33EP64GP
502-I/SO (e3)
      1310017
```

28-Lead SSOP

```
XXXXXXXXXXX
XXXXXXXXXXX
      YYWWNNN
```

Example

```
dsPIC33EP64
GP502-I/SS (e3)
      1310017
```

28-Lead QFN-S (6x6x0.9 mm)

```
XXXXXXXX
XXXXXXXX
YYWWNNN
```

Example

```
33EP64GP
502-I/MM
 1310017
```
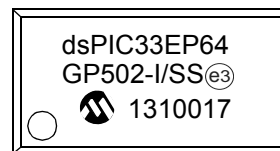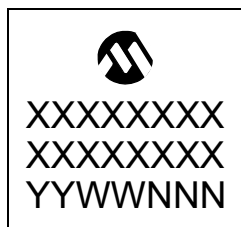
Legend:	XX...X	Customer-specific information
	Y	Year code (last digit of calendar year)
	YY	Year code (last 2 digits of calendar year)
	WW	Week code (week of January 1 is week '01')
	NNN	Alphanumeric traceability code
	(e3)	Pb-free JEDEC designator for Matte Tin (Sn)
	*	This package is Pb-free. The Pb-free JEDEC designator ((e3)) can be found on the outer packaging for this package.
Note:		In the event the full Microchip part number cannot be marked on one line, it will be carried over to the next line, thus limiting the number of available characters for customer-specific information.

44-Lead Plastic Quad Flat, No Lead Package (ML) - 8x8 mm Body [QFN]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging
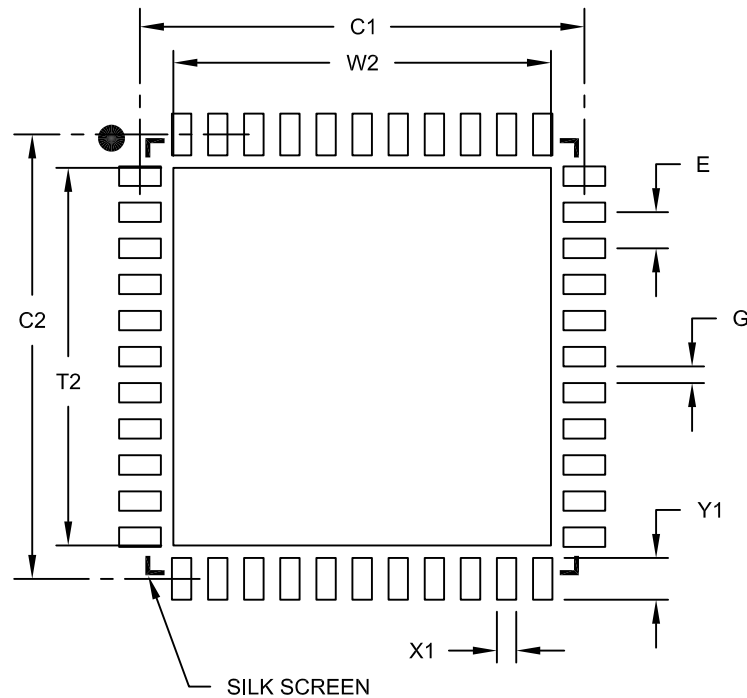
RECOMMENDED LAND PATTERN

	Units	MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Contact Pitch	E	0.65 BSC		
Optional Center Pad Width	W2			6.60
Optional Center Pad Length	T2			6.60
Contact Pad Spacing	C1		8.00	
Contact Pad Spacing	C2		8.00	
Contact Pad Width (X44)	X1			0.35
Contact Pad Length (X44)	Y1			0.85
Distance Between Pads	G	0.25		

Notes:
1. Dimensioning and tolerancing per ASME Y14.5M

BSC: Basic Dimension. Theoretically exact value shown without tolerances.

Microchip Technology Drawing No. C04-2103B