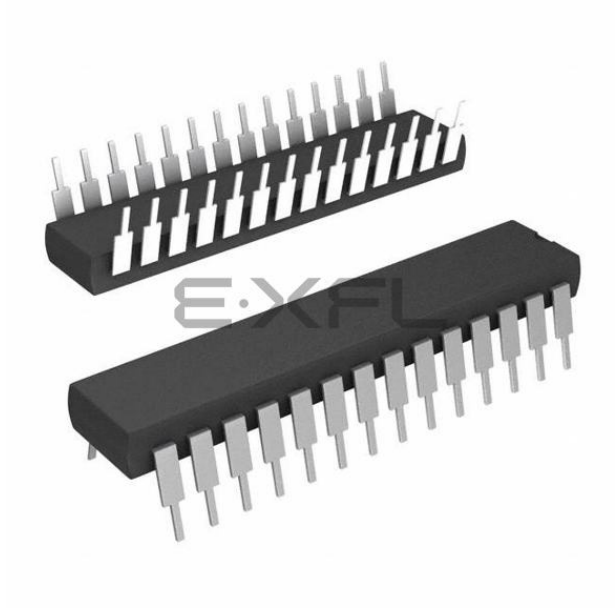

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## What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

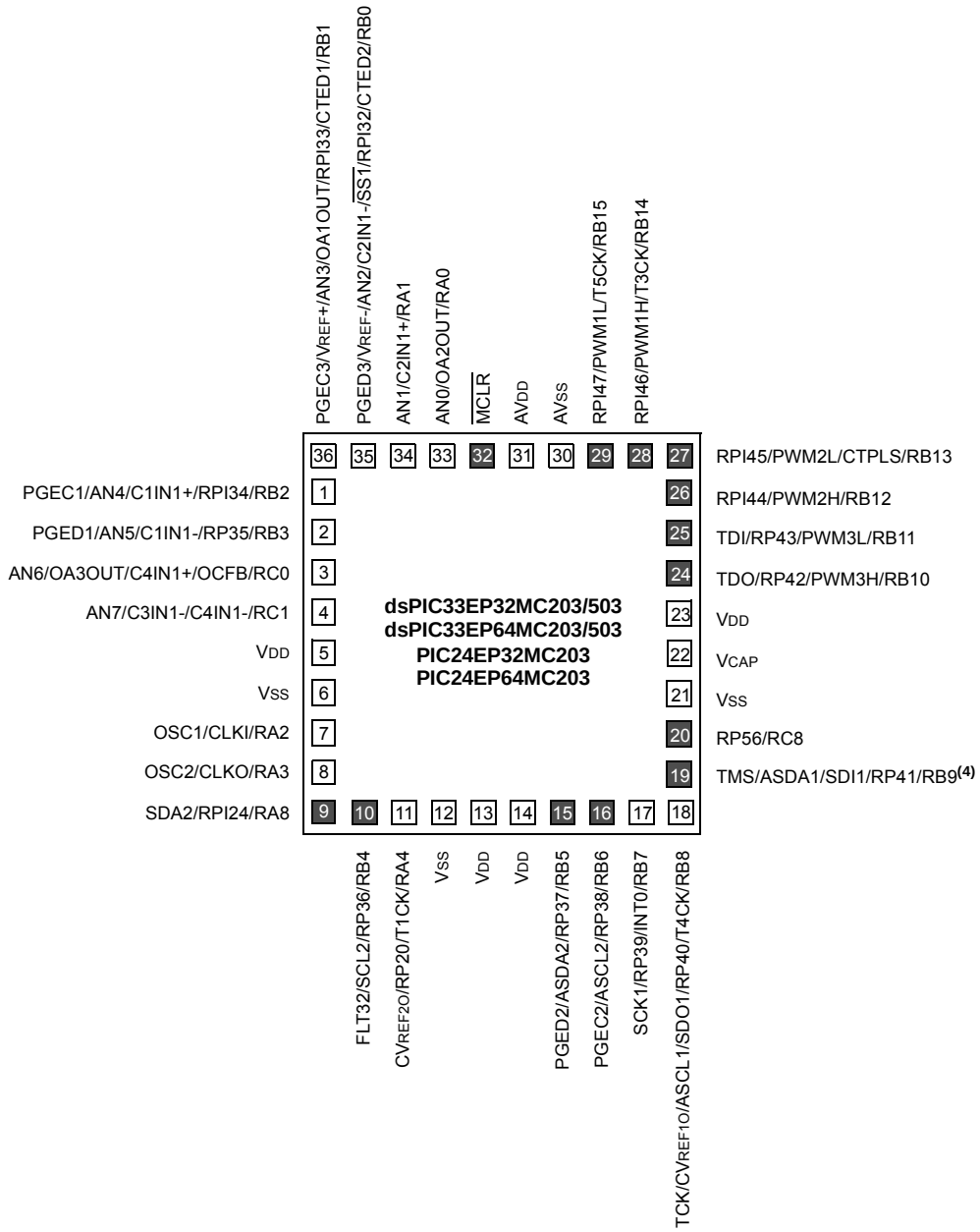
## Applications of "Embedded - Microcontrollers"

| Details | |
|---|---|
| Product Status | Active |
| Core Processor | PIC |
| Core Size | 16-Bit |
| Speed | 70 MIPs |
| Connectivity | I²C, IrDA, LINbus, QEI, SPI, UART/USART |
| Peripherals | Brown-out Detect/Reset, DMA, Motor Control PWM, POR, PWM, WDT |
| Number of I/O | 21 |
| Program Memory Size | 128KB (43K x 24) |
| Program Memory Type | FLASH |
| EEPROM Size | - |
| RAM Size | 8K x 16 |
| Voltage - Supply (Vcc/Vdd) | 3V ~ 3.6V |
| Data Converters | A/D 6x10b/12b |
| Oscillator Type | Internal |
| Operating Temperature | -40°C ~ 85°C (TA) |
| Mounting Type | Through Hole |
| Package / Case | 28-DIP (0.300", 7.62mm) |
| Supplier Device Package | 28-SPDIP |
| Purchase URL | https://www.e-xfl.com/product-detail/microchip-technology/pic24ep128mc202-i-sp |

## Pin Diagrams (Continued)

**36-Pin VTLA(1,2,3)**

■ = Pins are up to 5V tolerant




**Note 1:** The RPn/RPIn pins can be used by any remappable peripheral with some limitation. See **Section 11.4 "Peripheral Pin Select (PPS)"** for available peripherals and for information on limitations.

**2:** Every I/O port pin (RAx-RGx) can be used as a Change Notification pin (CNAx-CNGx). See **Section 11.0 "I/O Ports"** for more information.

**3:** The metal pad at the bottom of the device is not connected to any pins and is recommended to be connected to VSS externally.

**4:** There is an internal pull-up resistor connected to the TMS pin when the JTAG interface is active. See the JTAGEN bit field in Table 27-2.

**TABLE 1-1: PINOUT I/O DESCRIPTIONS**

| Pin Name(4) | Pin Type | Buffer Type | PPS | Description |
|---|---|---|---|---|
| AN0-AN15 | I | Analog | No | Analog input channels. |
| CLKI | I | ST/ CMOS | No | External clock source input. Always associated with OSC1 pin function. |
| CLKO | O | — | No | Oscillator crystal output. Connects to crystal or resonator in Crystal Oscillator mode. Optionally functions as CLKO in RC and EC modes. Always associated with OSC2 pin function. |
| OSC1 | I | ST/ CMOS | No | Oscillator crystal input. ST buffer when configured in RC mode; CMOS otherwise. |
| OSC2 | I/O | — | No | Oscillator crystal output. Connects to crystal or resonator in Crystal Oscillator mode. Optionally functions as CLKO in RC and EC modes. |
| REFCLKO | O | — | Yes | Reference clock output. |
| IC1-IC4 | I | ST | Yes | Capture Inputs 1 through 4. |
| OCFA | I | ST | Yes | Compare Fault A input (for Compare channels). |
| OCFB | I | ST | No | Compare Fault B input (for Compare channels). |
| OC1-OC4 | O | — | Yes | Compare Outputs 1 through 4. |
| INT0 | I | ST | No | External Interrupt 0. |
| INT1 | I | ST | Yes | External Interrupt 1. |
| INT2 | I | ST | Yes | External Interrupt 2. |
| RA0-RA4, RA7-RA12 | I/O | ST | No | PORTA is a bidirectional I/O port. |
| RB0-RB15 | I/O | ST | No | PORTB is a bidirectional I/O port. |
| RC0-RC13, RC15 | I/O | ST | No | PORTC is a bidirectional I/O port. |
| RD5, RD6, RD8 | I/O | ST | No | PORTD is a bidirectional I/O port. |
| RE12-RE15 | I/O | ST | No | PORTE is a bidirectional I/O port. |
| RF0, RF1 | I/O | ST | No | PORTF is a bidirectional I/O port. |
| RG6-RG9 | I/O | ST | No | PORTG is a bidirectional I/O port. |
| T1CK | I | ST | No | Timer1 external clock input. |
| T2CK | I | ST | Yes | Timer2 external clock input. |
| T3CK | I | ST | No | Timer3 external clock input. |
| T4CK | I | ST | No | Timer4 external clock input. |
| T5CK | I | ST | No | Timer5 external clock input. |
| CTPLS | O | ST | No | CTMU pulse output. |
| CTED1 | I | ST | No | CTMU External Edge Input 1. |
| CTED2 | I | ST | No | CTMU External Edge Input 2. |
| $\overline{U1CTS}$ | I | ST | No | UART1 Clear-To-Send. |
| $\overline{U1RTS}$ | O | — | No | UART1 Ready-To-Send. |
| U1RX | I | ST | Yes | UART1 receive. |
| U1TX | O | — | Yes | UART1 transmit. |
| BCLK1 | O | ST | No | UART1 IrDA® baud clock output. |

**Legend:** CMOS = CMOS compatible input or output; Analog = Analog input; P = Power
ST = Schmitt Trigger input with CMOS levels; O = Output; I = Input
PPS = Peripheral Pin Select; TTL = TTL input buffer

**Note 1:** This pin is available on dsPIC33EPXXXMC20X/50X and PIC24EPXXXMC20X devices only.

**2:** This pin is available on dsPIC33EPXXXGP/MC50X devices only.

**3:** This is the default Fault on Reset for dsPIC33EPXXXMC20X/50X and PIC24EPXXXMC20X devices. See **Section 16.0 "High-Speed PWM Module (dsPIC33EPXXXMC20X/50X and PIC24EPXXXMC20X Devices Only)"** for more information.

**4:** Not all pins are available in all packages variants. See the **"Pin Diagrams"** section for pin availability.

**5:** There is an internal pull-up resistor connected to the TMS pin when the JTAG interface is active. See the JTAGEN bit field in Table 27-2.

**TABLE 1-1: PINOUT I/O DESCRIPTIONS (CONTINUED)**

| Pin Name(4) | Pin Type | Buffer Type | PPS | Description |
|---|---|---|---|---|
| U2CTS | I | ST | No | UART2 Clear-To-Send. |
| U2RTS | O | — | No | UART2 Ready-To-Send. |
| U2RX | I | ST | Yes | UART2 receive. |
| U2TX | O | — | Yes | UART2 transmit. |
| BCLK2 | O | ST | No | UART2 IrDA® baud clock output. |
| SCK1 | I/O | ST | No | Synchronous serial clock input/output for SPI1. |
| SDI1 | I | ST | No | SPI1 data in. |
| SDO1 | O | — | No | SPI1 data out. |
| SS1 | I/O | ST | No | SPI1 slave synchronization or frame pulse I/O. |
| SCK2 | I/O | ST | Yes | Synchronous serial clock input/output for SPI2. |
| SDI2 | I | ST | Yes | SPI2 data in. |
| SDO2 | O | — | Yes | SPI2 data out. |
| SS2 | I/O | ST | Yes | SPI2 slave synchronization or frame pulse I/O. |
| SCL1 | I/O | ST | No | Synchronous serial clock input/output for I2C1. |
| SDA1 | I/O | ST | No | Synchronous serial data input/output for I2C1. |
| ASCL1 | I/O | ST | No | Alternate synchronous serial clock input/output for I2C1. |
| ASDA1 | I/O | ST | No | Alternate synchronous serial data input/output for I2C1. |
| SCL2 | I/O | ST | No | Synchronous serial clock input/output for I2C2. |
| SDA2 | I/O | ST | No | Synchronous serial data input/output for I2C2. |
| ASCL2 | I/O | ST | No | Alternate synchronous serial clock input/output for I2C2. |
| ASDA2 | I/O | ST | No | Alternate synchronous serial data input/output for I2C2. |
| TMS(5) | I | ST | No | JTAG Test mode select pin. |
| TCK | I | ST | No | JTAG test clock input pin. |
| TDI | I | ST | No | JTAG test data input pin. |
| TDO | O | — | No | JTAG test data output pin. |
| C1RX(2) | I | ST | Yes | ECAN1 bus receive pin. |
| C1TX(2) | O | — | Yes | ECAN1 bus transmit pin. |
| FLT1(1), FLT2(1) | I | ST | Yes | PWM Fault Inputs 1 and 2. |
| FLT3(1), FLT4(1) | I | ST | No | PWM Fault Inputs 3 and 4. |
| FLT32(1,3) | I | ST | No | PWM Fault Input 32 (Class B Fault). |
| DTCMP1-DTCMP3(1) | I | ST | Yes | PWM Dead-Time Compensation Inputs 1 through 3. |
| PWM1L-PWM3L(1) | O | — | No | PWM Low Outputs 1 through 3. |
| PWM1H-PWM3H(1) | O | — | No | PWM High Outputs 1 through 3. |
| SYNCI1(1) | I | ST | Yes | PWM Synchronization Input 1. |
| SYNCO1(1) | O | — | Yes | PWM Synchronization Output 1. |
| INDX1(1) | I | ST | Yes | Quadrature Encoder Index1 pulse input. |
| HOME1(1) | I | ST | Yes | Quadrature Encoder Home1 pulse input. |
| QEA1(1) | I | ST | Yes | Quadrature Encoder Phase A input in QEI1 mode. Auxiliary timer external clock/gate input in Timer mode. |
| QEB1(1) | I | ST | Yes | Quadrature Encoder Phase B input in QEI1 mode. Auxiliary timer external clock/gate input in Timer mode. |
| CNTCMP1(1) | O | — | Yes | Quadrature Encoder Compare Output 1. |

**Legend:** CMOS = CMOS compatible input or output; Analog = Analog input; P = Power
ST = Schmitt Trigger input with CMOS levels; O = Output; I = Input
PPS = Peripheral Pin Select; TTL = TTL input buffer

**Note 1:** This pin is available on dsPIC33EPXXXMC20X/50X and PIC24EPXXXMC20X devices only.

**2:** This pin is available on dsPIC33EPXXXGP/MC50X devices only.

**3:** This is the default Fault on Reset for dsPIC33EPXXXMC20X/50X and PIC24EPXXXMC20X devices. See **Section 16.0 "High-Speed PWM Module (dsPIC33EPXXXMC20X/50X and PIC24EPXXXMC20X Devices Only)"** for more information.

**4:** Not all pins are available in all packages variants. See the **"Pin Diagrams"** section for pin availability.

**5:** There is an internal pull-up resistor connected to the TMS pin when the JTAG interface is active. See the JTAGEN bit field in Table 27-2.

**TABLE 4-11: PTG REGISTER MAP**

| File Name | Addr. | Bit 15 | Bit 14 | Bit 13 | Bit 12 | Bit 11 | Bit 10 | Bit 9 | Bit 8 | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 | All Resets |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| PTGCST | 0AC0 | PTGEN | — | PTGSIDL | PTGTOGL | — | PTGSWT | PTGSSEN | PTGIVIS | PTGSTRT | PTGWTO | — | — | — | — | PTGITM<1:0> | | 0000 |
| PTGCON | 0AC2 | PTGCLK<2:0> | | | PTGDIV<4:0> | | | | | PTGPWD<3:0> | | | | — | PTGWDT<2:0> | | | 0000 |
| PTGBTE | 0AC4 | ADCTS<4:1> | | | | IC4TSS | IC3TSS | IC2TSS | IC1TSS | OC4CS | OC3CS | OC2CS | OC1CS | OC4TSS | OC3TSS | OC2TSS | OC1TSS | 0000 |
| PTGHOLD | 0AC6 | PTGHOLD<15:0> | | | | | | | | | | | | | | | | 0000 |
| PTGT0LIM | 0AC8 | PTGT0LIM<15:0> | | | | | | | | | | | | | | | | 0000 |
| PTGT1LIM | 0ACA | PTGT1LIM<15:0> | | | | | | | | | | | | | | | | 0000 |
| PTGSDLIM | 0ACC | PTGSDLIM<15:0> | | | | | | | | | | | | | | | | 0000 |
| PTGC0LIM | 0ACE | PTGC0LIM<15:0> | | | | | | | | | | | | | | | | 0000 |
| PTGC1LIM | 0AD0 | PTGC1LIM<15:0> | | | | | | | | | | | | | | | | 0000 |
| PTGADJ | 0AD2 | PTGADJ<15:0> | | | | | | | | | | | | | | | | 0000 |
| PTGL0 | 0AD4 | PTGL0<15:0> | | | | | | | | | | | | | | | | 0000 |
| PTGQPTR | 0AD6 | — | — | — | — | — | — | — | — | — | — | — | PTGQPTR<4:0> | | | | | 0000 |
| PTGQUE0 | 0AD8 | STEP1<7:0> | | | | | | | | STEP0<7:0> | | | | | | | | 0000 |
| PTGQUE1 | 0ADA | STEP3<7:0> | | | | | | | | STEP2<7:0> | | | | | | | | 0000 |
| PTGQUE2 | 0ADC | STEP5<7:0> | | | | | | | | STEP4<7:0> | | | | | | | | 0000 |
| PTGQUE3 | 0ADE | STEP7<7:0> | | | | | | | | STEP6<7:0> | | | | | | | | 0000 |
| PTGQUE4 | 0AE0 | STEP9<7:0> | | | | | | | | STEP8<7:0> | | | | | | | | 0000 |
| PTGQUE5 | 0AE2 | STEP11<7:0> | | | | | | | | STEP10<7:0> | | | | | | | | 0000 |
| PTGQUE6 | 0AE4 | STEP13<7:0> | | | | | | | | STEP12<7:0> | | | | | | | | 0000 |
| PTGQUE7 | 0AE6 | STEP15<7:0> | | | | | | | | STEP14<7:0> | | | | | | | | 0000 |

**Legend:** — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

## 4.5 Instruction Addressing Modes

The addressing modes shown in Table 4-63 form the basis of the addressing modes optimized to support the specific features of individual instructions. The addressing modes provided in the MAC class of instructions differ from those in the other instruction types.

### 4.5.1 FILE REGISTER INSTRUCTIONS

Most file register instructions use a 13-bit address field (f) to directly address data present in the first 8192 bytes of data memory (Near Data Space). Most file register instructions employ a working register, W0, which is denoted as WREG in these instructions. The destination is typically either the same file register or WREG (with the exception of the MUL instruction), which writes the result to a register or register pair. The MOV instruction allows additional flexibility and can access the entire Data Space.

### 4.5.2 MCU INSTRUCTIONS

The three-operand MCU instructions are of the form:

```
Operand 3 = Operand 1 <function> Operand 2
```

where Operand 1 is always a working register (that is, the addressing mode can only be Register Direct), which is referred to as Wb. Operand 2 can be a W register fetched from data memory or a 5-bit literal. The result location can either be a W register or a data memory location. The following addressing modes are supported by MCU instructions:

- Register Direct
- Register Indirect
- Register Indirect Post-Modified
- Register Indirect Pre-Modified
- 5-Bit or 10-Bit Literal

**Note:** Not all instructions support all the addressing modes given above. Individual instructions can support different subsets of these addressing modes.

**TABLE 4-63: FUNDAMENTAL ADDRESSING MODES SUPPORTED**

| Addressing Mode | Description |
|---|---|
| File Register Direct | The address of the file register is specified explicitly. |
| Register Direct | The contents of a register are accessed directly. |
| Register Indirect | The contents of Wn form the Effective Address (EA). |
| Register Indirect Post-Modified | The contents of Wn form the EA. Wn is post-modified (incremented or decremented) by a constant value. |
| Register Indirect Pre-Modified | Wn is pre-modified (incremented or decremented) by a signed constant value to form the EA. |
| Register Indirect with Register Offset (Register Indexed) | The sum of Wn and Wb forms the EA. |
| Register Indirect with Literal Offset | The sum of Wn and a literal forms the EA. |

**TABLE 7-1: INTERRUPT VECTOR DETAILS (CONTINUED)**

| Interrupt Source | Vector # | IRQ # | IVT Address | Interrupt Bit Location | | |
|---|---|---|---|---|---|---|
| | | | | Flag | Enable | Priority |
| QEI1 – QEI1 Position Counter Compare(2) | 66 | 58 | 0x000088 | IFS3<10> | IEC3<10> | IPC14<10:8> |
| Reserved | 67-72 | 59-64 | 0x00008A-0x000094 | — | — | — |
| U1E – UART1 Error Interrupt | 73 | 65 | 0x000096 | IFS4<1> | IEC4<1> | IPC16<6:4> |
| U2E – UART2 Error Interrupt | 74 | 66 | 0x000098 | IFS4<2> | IEC4<2> | IPC16<10:8> |
| CRC – CRC Generator Interrupt | 75 | 67 | 0x00009A | IFS4<3> | IEC4<3> | IPC16<14:12> |
| Reserved | 76-77 | 68-69 | 0x00009C-0x00009E | — | — | — |
| C1TX – CAN1 TX Data Request(1) | 78 | 70 | 0x000A0 | IFS4<6> | IEC4<6> | IPC17<10:8> |
| Reserved | 79-84 | 71-76 | 0x0000A2-0x0000AC | — | — | — |
| CTMU – CTMU Interrupt | 85 | 77 | 0x0000AE | IFS4<13> | IEC4<13> | IPC19<6:4> |
| Reserved | 86-101 | 78-93 | 0x0000B0-0x0000CE | — | — | — |
| PWM1 – PWM Generator 1(2) | 102 | 94 | 0x0000D0 | IFS5<14> | IEC5<14> | IPC23<10:8> |
| PWM2 – PWM Generator 2(2) | 103 | 95 | 0x0000D2 | IFS5<15> | IEC5<15> | IPC23<14:12> |
| PWM3 – PWM Generator 3(2) | 104 | 96 | 0x0000D4 | IFS6<0> | IEC6<0> | IPC24<2:0> |
| Reserved | 105-149 | 97-141 | 0x0001D6-0x00012E | — | — | — |
| ICD – ICD Application | 150 | 142 | 0x000142 | IFS8<14> | IEC8<14> | IPC35<10:8> |
| JTAG – JTAG Programming | 151 | 143 | 0x000130 | IFS8<15> | IEC8<15> | IPC35<14:12> |
| Reserved | 152 | 144 | 0x000134 | — | — | — |
| PTGSTEP – PTG Step | 153 | 145 | 0x000136 | IFS9<1> | IEC9<1> | IPC36<6:4> |
| PTGWDT – PTG Watchdog Time-out | 154 | 146 | 0x000138 | IFS9<2> | IEC9<2> | IPC36<10:8> |
| PTG0 – PTG Interrupt 0 | 155 | 147 | 0x00013A | IFS9<3> | IEC9<3> | IPC36<14:12> |
| PTG1 – PTG Interrupt 1 | 156 | 148 | 0x00013C | IFS9<4> | IEC9<4> | IPC37<2:0> |
| PTG2 – PTG Interrupt 2 | 157 | 149 | 0x00013E | IFS9<5> | IEC9<5> | IPC37<6:4> |
| PTG3 – PTG Interrupt 3 | 158 | 150 | 0x000140 | IFS9<6> | IEC9<6> | IPC37<10:8> |
| Reserved | 159-245 | 151-245 | 0x000142-0x0001FE | — | — | — |
| Lowest Natural Order Priority | | | | | | |

**Note 1:** This interrupt source is available on dsPIC33EPXXXGP50X and dsPIC33EPXXXMC50X devices only.

**2:** This interrupt source is available on dsPIC33EPXXXMC20X/50X and PIC24EPXXXMC20X devices only.

**REGISTER 7-3: INTCON1: INTERRUPT CONTROL REGISTER 1**

| R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
|---|---|---|---|---|---|---|---|
| NSTDIS | OVAERR(1) | OVBERR(1) | COVAERR(1) | COVBERR(1) | OVATE(1) | OVBTE(1) | COVTE(1) |
| bit 15 | | | | | | | bit 8 |

| R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | U-0 |
|---|---|---|---|---|---|---|---|
| SFTACERR(1) | DIV0ERR | DMACERR | MATHERR | ADDRERR | STKERR | OSCFAIL | — |
| bit 7 | | | | | | | bit 0 |

| **Legend:** | | | |
|---|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as '0' | |
| -n = Value at POR | '1' = Bit is set | '0' = Bit is cleared | x = Bit is unknown |

bit 15 **NSTDIS:** Interrupt Nesting Disable bit
1 = Interrupt nesting is disabled
0 = Interrupt nesting is enabled

bit 14 **OVAERR:** Accumulator A Overflow Trap Flag bit(1)
1 = Trap was caused by overflow of Accumulator A
0 = Trap was not caused by overflow of Accumulator A

bit 13 **OVBERR:** Accumulator B Overflow Trap Flag bit(1)
1 = Trap was caused by overflow of Accumulator B
0 = Trap was not caused by overflow of Accumulator B

bit 12 **COVAERR:** Accumulator A Catastrophic Overflow Trap Flag bit(1)
1 = Trap was caused by catastrophic overflow of Accumulator A
0 = Trap was not caused by catastrophic overflow of Accumulator A

bit 11 **COVBERR:** Accumulator B Catastrophic Overflow Trap Flag bit(1)
1 = Trap was caused by catastrophic overflow of Accumulator B
0 = Trap was not caused by catastrophic overflow of Accumulator B

bit 10 **OVATE:** Accumulator A Overflow Trap Enable bit(1)
1 = Trap overflow of Accumulator A
0 = Trap is disabled

bit 9 **OVBTE:** Accumulator B Overflow Trap Enable bit(1)
1 = Trap overflow of Accumulator B
0 = Trap is disabled

bit 8 **COVTE:** Catastrophic Overflow Trap Enable bit(1)
1 = Trap on catastrophic overflow of Accumulator A or B is enabled
0 = Trap is disabled

bit 7 **SFTACERR:** Shift Accumulator Error Status bit(1)
1 = Math error trap was caused by an invalid accumulator shift
0 = Math error trap was not caused by an invalid accumulator shift

bit 6 **DIV0ERR:** Divide-by-Zero Error Status bit
1 = Math error trap was caused by a divide-by-zero
0 = Math error trap was not caused by a divide-by-zero

bit 5 **DMACERR:** DMAC Trap Flag bit
1 = DMAC trap has occurred
0 = DMAC trap has not occurred

**Note 1:** These bits are available on dsPIC33EPXXXMC20X/50X and dsPIC33EPXXXGP50X devices only.

## 11.4 Peripheral Pin Select (PPS)

A major challenge in general purpose devices is providing the largest possible set of peripheral features while minimizing the conflict of features on I/O pins. The challenge is even greater on low pin count devices. In an application where more than one peripheral needs to be assigned to a single pin, inconvenient workarounds in application code, or a complete redesign, may be the only option.

Peripheral Pin Select configuration provides an alternative to these choices by enabling peripheral set selection and their placement on a wide range of I/O pins. By increasing the pinout options available on a particular device, users can better tailor the device to their entire application, rather than trimming the application to fit the device.

The Peripheral Pin Select configuration feature operates over a fixed subset of digital I/O pins. Users may independently map the input and/or output of most digital peripherals to any one of these I/O pins. Hardware safeguards are included that prevent accidental or spurious changes to the peripheral mapping once it has been established.

### 11.4.1 AVAILABLE PINS

The number of available pins is dependent on the particular device and its pin count. Pins that support the Peripheral Pin Select feature include the label, “RPn” or “RPIn”, in their full pin designation, where “n” is the remappable pin number. “RP” is used to designate pins that support both remappable input and output functions, while “RPI” indicates pins that support remappable input functions only.

### 11.4.2 AVAILABLE PERIPHERALS

The peripherals managed by the Peripheral Pin Select are all digital-only peripherals. These include general serial communications (UART and SPI), general purpose timer clock inputs, timer-related peripherals (input capture and output compare) and interrupt-on-change inputs.

In comparison, some digital-only peripheral modules are never included in the Peripheral Pin Select feature. This is because the peripheral’s function requires special I/O circuitry on a specific port and cannot be easily connected to multiple pins. These modules include $I^2C$™ and the PWM. A similar requirement excludes all modules with analog inputs, such as the ADC Converter.

A key difference between remappable and non-remappable peripherals is that remappable peripherals are not associated with a default I/O pin. The peripheral must always be assigned to a specific I/O pin before it can be used. In contrast, non-remappable peripherals are always available on a default pin, assuming that the peripheral is active and not conflicting with another peripheral.

When a remappable peripheral is active on a given I/O pin, it takes priority over all other digital I/O and digital communication peripherals associated with the pin. Priority is given regardless of the type of peripheral that is mapped. Remappable peripherals never take priority over any analog functions associated with the pin.

### 11.4.3 CONTROLLING PERIPHERAL PIN SELECT

Peripheral Pin Select features are controlled through two sets of SFRs: one to map peripheral inputs and one to map outputs. Because they are separately controlled, a particular peripheral’s input and output (if the peripheral has both) can be placed on any selectable function pin without constraint.

The association of a peripheral to a peripheral-selectable pin is handled in two different ways, depending on whether an input or output is being mapped.

**REGISTER 16-1: PTCON: PWMx TIME BASE CONTROL REGISTER (CONTINUED)**

bit 6-4 **SYNCSRC<2:0>:** Synchronous Source Selection bits(1)
111 = Reserved
•
•
•
100 = Reserved
011 = PTGO17(2)
010 = PTGO16(2)
001 = Reserved
000 = SYNCI1 input from PPS

bit 3-0 **SEVTPS<3:0>:** PWMx Special Event Trigger Output Postscaler Select bits(1)
1111 = 1:16 Postscaler generates Special Event Trigger on every sixteenth compare match event
•
•
•
0001 = 1:2 Postscaler generates Special Event Trigger on every second compare match event
0000 = 1:1 Postscaler generates Special Event Trigger on every compare match event

**Note 1:** These bits should be changed only when PTEN = 0. In addition, when using the SYNCI1 feature, the user application must program the period register with a value that is slightly larger than the expected period of the external synchronization input signal.

**2:** See **Section 24.0 "Peripheral Trigger Generator (PTG) Module"** for information on this selection.

**REGISTER 17-1: QEI1CON: QEI1 CONTROL REGISTER (CONTINUED)**

bit 6-4 **INTDIV<2:0>:** Timer Input Clock Prescale Select bits (interval timer, main timer (position counter), velocity counter and index counter internal clock divider select)(3)

111 = 1:128 prescale value
110 = 1:64 prescale value
101 = 1:32 prescale value
100 = 1:16 prescale value
011 = 1:8 prescale value
010 = 1:4 prescale value
001 = 1:2 prescale value
000 = 1:1 prescale value

bit 3 **CNTPOL:** Position and Index Counter/Timer Direction Select bit

1 = Counter direction is negative unless modified by external up/down signal
0 = Counter direction is positive unless modified by external up/down signal

bit 2 **GATEN:** External Count Gate Enable bit

1 = External gate signal controls position counter operation
0 = External gate signal does not affect position counter/timer operation

bit 1-0 **CCM<1:0>:** Counter Control Mode Selection bits

11 = Internal Timer mode with optional external count is selected
10 = External clock count with optional external count is selected
01 = External clock count with external up/down direction is selected
00 = Quadrature Encoder Interface (x4 mode) Count mode is selected

**Note 1:** When CCM<1:0> = 10 or 11, all of the QEI counters operate as timers and the PIMOD<2:0> bits are ignored.

**2:** When CCM<1:0> = 00, and QEA and QEB values match the Index Match Value (IMV), the POSCNTH and POSCNTL registers are reset. QEA/QEB signals used for the index match have swap and polarity values applied, as determined by the SWPAB and QEAPOL/QEBPOL bits.

**3:** The selected clock rate should be at least twice the expected maximum quadrature count rate.

## 18.1 SPI Helpful Tips

1. In Frame mode, if there is a possibility that the master may not be initialized before the slave:
   a) If FRMPOL (SPIxCON2<13>) = 1, use a pull-down resistor on SSx.
   b) If FRMPOL = 0, use a pull-up resistor on SSx.

| **Note:** | This insures that the first frame transmission after initialization is not shifted or corrupted. |
|---|---|

2. In Non-Framed 3-Wire mode, (i.e., not using SSx from a master):
   a) If CKP (SPIxCON1<6>) = 1, always place a pull-up resistor on SSx.
   b) If CKP = 0, always place a pull-down resistor on SSx.

| **Note:** | This will insure that during power-up and initialization the master/slave will not lose Sync due to an errant SCKx transition that would cause the slave to accumulate data shift errors for both transmit and receive appearing as corrupted data. |
|---|---|

3. FRMEN (SPIxCON2<15>) = 1 and SSEN (SPIxCON1<7>) = 1 are exclusive and invalid. In Frame mode, SCKx is continuous and the Frame Sync pulse is active on the SSx pin, which indicates the start of a data frame.

| **Note:** | Not all third-party devices support Frame mode timing. Refer to the SPIx specifications in **Section 30.0 "Electrical Characteristics"** for details. |
|---|---|

4. In Master mode only, set the SMP bit (SPIxCON1<9>) to a '1' for the fastest SPIx data rate possible. The SMP bit can only be set at the same time or after the MSTEN bit (SPIxCON1<5>) is set.

To avoid invalid slave read data to the master, the user's master software must ensure enough time for slave software to fill its write buffer before the user application initiates a master write/read cycle. It is always advisable to preload the SPIxBUF Transmit register in advance of the next master transaction cycle. SPIxBUF is transferred to the SPIx Shift register and is empty once the data transmission begins.

## 18.2 SPI Resources

Many useful resources are provided on the main product page of the Microchip web site for the devices listed in this data sheet. This product page, which can be accessed using this link, contains the latest updates and additional information.

| **Note:** | In the event you are not able to access the product page using the link above, enter this URL in your browser: http://www.microchip.com/wwwproducts/Devices.aspx?dDocName=en555464 |
|---|---|

### 18.2.1 KEY RESOURCES

- **"Serial Peripheral Interface (SPI)"** (DS70569) in the *"dsPIC33/PIC24 Family Reference Manual"*
- Code Samples
- Application Notes
- Software Libraries
- Webinars
- All Related *"dsPIC33/PIC24 Family Reference Manual"* Sections
- Development Tools

**REGISTER 21-17: CxRXFnEID: ECANx ACCEPTANCE FILTER n EXTENDED IDENTIFIER REGISTER (n = 0-15)**

| R/W-x | R/W-x | R/W-x | R/W-x | R/W-x | R/W-x | R/W-x | R/W-x |
|---|---|---|---|---|---|---|---|
| EID15 | EID14 | EID13 | EID12 | EID11 | EID10 | EID9 | EID8 |
| bit 15 | | | | | | | bit 8 |

| R/W-x | R/W-x | R/W-x | R/W-x | R/W-x | R/W-x | R/W-x | R/W-x |
|---|---|---|---|---|---|---|---|
| EID7 | EID6 | EID5 | EID4 | EID3 | EID2 | EID1 | EID0 |
| bit 7 | | | | | | | bit 0 |

| **Legend:** | | | |
|---|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as '0' | |
| -n = Value at POR | '1' = Bit is set | '0' = Bit is cleared | x = Bit is unknown |

bit 15-0 **EID<15:0>:** Extended Identifier bits
1 = Message address bit, EIDx, must be '1' to match filter
0 = Message address bit, EIDx, must be '0' to match filter

**REGISTER 21-18: CxFMSKSEL1: ECANx FILTER 7-0 MASK SELECTION REGISTER 1**

| R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
|---|---|---|---|---|---|---|---|
| F7MSK<1:0> | | F6MSK<1:0> | | F5MSK<1:0> | | F4MSK<1:0> | |
| bit 15 | | | | | | | bit 8 |

| R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
|---|---|---|---|---|---|---|---|
| F3MSK<1:0> | | F2MSK<1:0> | | F1MSK<1:0> | | F0MSK<1:0> | |
| bit 7 | | | | | | | bit 0 |

| **Legend:** | | | |
|---|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as '0' | |
| -n = Value at POR | '1' = Bit is set | '0' = Bit is cleared | x = Bit is unknown |

bit 15-14 **F7MSK<1:0>:** Mask Source for Filter 7 bits
11 = Reserved
10 = Acceptance Mask 2 registers contain mask
01 = Acceptance Mask 1 registers contain mask
00 = Acceptance Mask 0 registers contain mask

bit 13-12 **F6MSK<1:0>:** Mask Source for Filter 6 bits (same values as bits<15:14>)

bit 11-10 **F5MSK<1:0>:** Mask Source for Filter 5 bits (same values as bits<15:14>)

bit 9-8 **F4MSK<1:0>:** Mask Source for Filter 4 bits (same values as bits<15:14>)

bit 7-6 **F3MSK<1:0>:** Mask Source for Filter 3 bits (same values as bits<15:14>)

bit 5-4 **F2MSK<1:0>:** Mask Source for Filter 2 bits (same values as bits<15:14>)

bit 3-2 **F1MSK<1:0>:** Mask Source for Filter 1 bits (same values as bits<15:14>)

bit 1-0 **F0MSK<1:0>:** Mask Source for Filter 0 bits (same values as bits<15:14>)

**REGISTER 21-19: CxFMSKSEL2: ECANx FILTER 15-8 MASK SELECTION REGISTER 2**

| R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
|---|---|---|---|---|---|---|---|
| F15MSK<1:0> | | F14MSK<1:0> | | F13MSK<1:0> | | F12MSK<1:0> | |
| bit 15 | | | | | | | bit 8 |

| R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
|---|---|---|---|---|---|---|---|
| F11MSK<1:0> | | F10MSK<1:0> | | F9MSK<1:0> | | F8MSK<1:0> | |
| bit 7 | | | | | | | bit 0 |

| **Legend:** | | | |
|---|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as ‘0’ | |
| -n = Value at POR | ‘1’ = Bit is set | ‘0’ = Bit is cleared | x = Bit is unknown |

bit 15-14 **F15MSK<1:0>:** Mask Source for Filter 15 bits
11 = Reserved
10 = Acceptance Mask 2 registers contain mask
01 = Acceptance Mask 1 registers contain mask
00 = Acceptance Mask 0 registers contain mask

bit 13-12 **F14MSK<1:0>:** Mask Source for Filter 14 bits (same values as bits<15:14>)

bit 11-10 **F13MSK<1:0>:** Mask Source for Filter 13 bits (same values as bits<15:14>)

bit 9-8 **F12MSK<1:0>:** Mask Source for Filter 12 bits (same values as bits<15:14>)

bit 7-6 **F11MSK<1:0>:** Mask Source for Filter 11 bits (same values as bits<15:14>)

bit 5-4 **F10MSK<1:0>:** Mask Source for Filter 10 bits (same values as bits<15:14>)

bit 3-2 **F9MSK<1:0>:** Mask Source for Filter 9 bits (same values as bits<15:14>)

bit 1-0 **F8MSK<1:0>:** Mask Source for Filter 8 bits (same values as bits<15:14>)

## 25.0 OP AMP/COMPARATOR MODULE

**Note 1:** This data sheet summarizes the features of the dsPIC33EPXXXGP50X, dsPIC33EPXXXMC20X/50X and PIC24EPXXXGP/MC20X families of devices. It is not intended to be a comprehensive reference source. To complement the information in this data sheet, refer to **"Op Amp/Comparator"** (DS70357) in the "*dsPIC33/PIC24 Family Reference Manual*", which is available from the Microchip web site (www.microchip.com).

**2:** Some registers and associated bits described in this section may not be available on all devices. Refer to **Section 4.0 "Memory Organization"** in this data sheet for device-specific register and bit information.

The dsPIC33EPXXXGP50X, dsPIC33EPXXXMC20X/50X and PIC24EPXXXGP/MC20X devices contain up to four comparators, which can be configured in various ways. Comparators, CMP1, CMP2 and CMP3, also have the option to be configured as op amps, with the output being brought to an external pin for gain/filtering connections. As shown in Figure 25-1, individual comparator options are specified by the comparator module's Special Function Register (SFR) control bits.

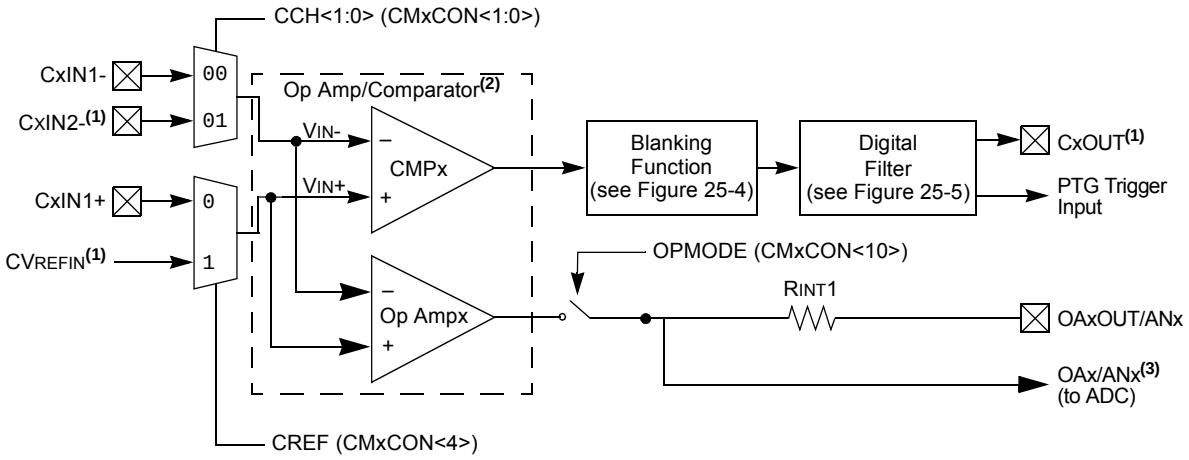
**Note:** Op Amp/Comparator 3 is not available on the dsPIC33EPXXXGP502/MC502/MC202 and PIC24EP256GP/MC202 (28-pin) devices.

These options allow users to:

- Select the edge for trigger and interrupt generation
- Configure the comparator voltage reference
- Configure output blanking and masking
- Configure as a comparator or op amp (CMP1, CMP2 and CMP3 only)

**Note:** Not all op amp/comparator input/output connections are available on all devices. See the **"Pin Diagrams"** section for available connections.

**FIGURE 25-1: OP AMP/COMPARATOR x MODULE BLOCK DIAGRAM (MODULES 1, 2 AND 3)**




**Note 1:** This input/output is not available as a selection when configured as an op amp (OPMODE (CMxCON<10>) = 1).

**2:** This module can be configured either as an op amp or a comparator using the OPMODE bit.

**3:** When configured as an op amp (OPMODE = 1), the ADC samples the op amp output; otherwise, the ADC samples the ANx pin.

**REGISTER 25-2: CMxCON: COMPARATOR x CONTROL REGISTER (x = 1, 2 OR 3) (CONTINUED)**

bit 7-6 **EVPOL<1:0>:** Trigger/Event/Interrupt Polarity Select bits
- 11 = Trigger/event/interrupt generated on any change of the comparator output (while CEVT = 0)
- 10 = Trigger/event/interrupt generated only on high-to-low transition of the polarity selected comparator output (while CEVT = 0)
  - If CPOL = 1 (inverted polarity):
    Low-to-high transition of the comparator output.
  - If CPOL = 0 (non-inverted polarity):
    High-to-low transition of the comparator output.
- 01 = Trigger/event/interrupt generated only on low-to-high transition of the polarity-selected comparator output (while CEVT = 0)
  - If CPOL = 1 (inverted polarity):
    High-to-low transition of the comparator output.
  - If CPOL = 0 (non-inverted polarity):
    Low-to-high transition of the comparator output
- 00 = Trigger/event/interrupt generation is disabled

bit 5 **Unimplemented:** Read as '0'

bit 4 **CREF:** Comparator Reference Select bit ($V_{IN+}$ input)(1)
- 1 = $V_{IN+}$ input connects to internal $CV_{REFIN}$ voltage(2)
- 0 = $V_{IN+}$ input connects to CxIN1+ pin

bit 3-2 **Unimplemented:** Read as '0'

bit 1-0 **CCH<1:0>:** Op Amp/Comparator Channel Select bits(1)
- 11 = Unimplemented
- 10 = Unimplemented
- 01 = Inverting input of the comparator connects to the CxIN2- pin(2)
- 00 = Inverting input of the op amp/comparator connects to the CxIN1- pin

**Note 1:** Inputs that are selected and not available will be tied to $V_{SS}$. See the **"Pin Diagrams"** section for available inputs for each package.

**2:** This output is not available when OPMODE (CMxCON<10>) = 1.

## 30.2 AC Characteristics and Timing Parameters

This section defines dsPIC33EPXXXGP50X, dsPIC33EPXXXMC20X/50X and PIC24EPXXXGP/MC20X AC characteristics and timing parameters.

**TABLE 30-15: TEMPERATURE AND VOLTAGE SPECIFICATIONS – AC**

| | |
|---|---|
| **AC CHARACTERISTICS** | **Standard Operating Conditions: 3.0V to 3.6V (unless otherwise stated)**<br>Operating temperature -40°C ≤ TA ≤ +85°C for Industrial<br>-40°C ≤ TA ≤ +125°C for Extended<br>Operating voltage VDD range as described in **Section 30.1 "DC Characteristics"**. |

**FIGURE 30-1: LOAD CONDITIONS FOR DEVICE TIMING SPECIFICATIONS**

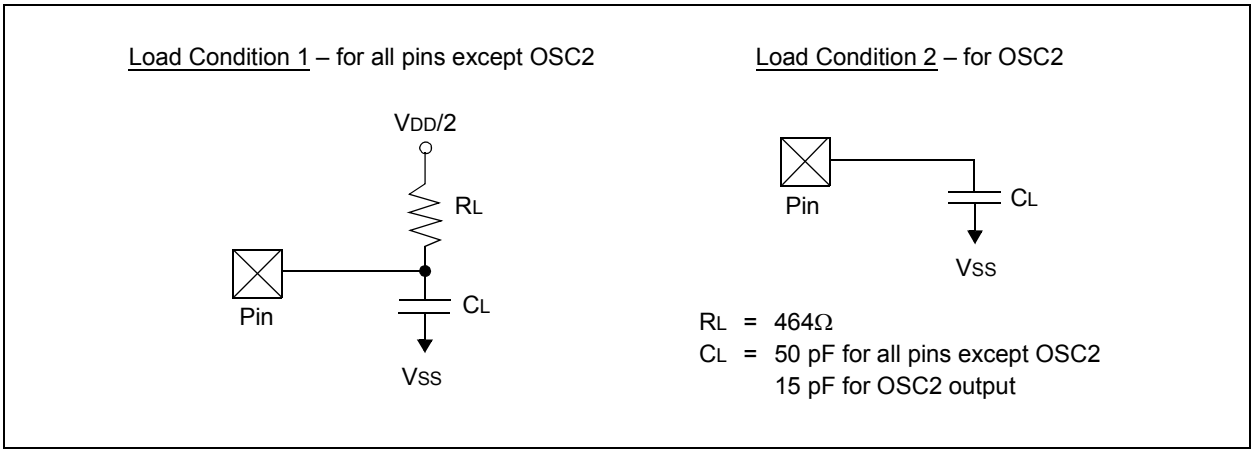



**TABLE 30-16: CAPACITIVE LOADING REQUIREMENTS ON OUTPUT PINS**

| Param No. | Symbol | Characteristic | Min. | Typ. | Max. | Units | Conditions |
|---|---|---|---|---|---|---|---|
| DO50 | COSCO | OSC2 Pin | — | — | 15 | pF | In XT and HS modes, when external clock is used to drive OSC1 |
| DO56 | CIO | All I/O Pins and OSC2 | — | — | 50 | pF | EC mode |
| DO58 | CB | SCLx, SDAx | — | — | 400 | pF | In $I^2C$™ mode |

**TABLE 30-40: SPI2 SLAVE MODE (FULL-DUPLEX, CKE = 0, CKP = 0, SMP = 0) TIMING REQUIREMENTS**

| AC CHARACTERISTICS | | | Standard Operating Conditions: 3.0V to 3.6V (unless otherwise stated)<br>Operating temperature -40°C ≤ TA ≤ +85°C for Industrial<br>-40°C ≤ TA ≤ +125°C for Extended | | | | |
|---|---|---|---|---|---|---|---|
| **Param.** | **Symbol** | **Characteristic(1)** | **Min.** | **Typ.(2)** | **Max.** | **Units** | **Conditions** |
| SP70 | FscP | Maximum SCK2 Input Frequency | — | — | 11 | MHz | **(Note 3)** |
| SP72 | TscF | SCK2 Input Fall Time | — | — | — | ns | See Parameter DO32 **(Note 4)** |
| SP73 | TscR | SCK2 Input Rise Time | — | — | — | ns | See Parameter DO31 **(Note 4)** |
| SP30 | TdoF | SDO2 Data Output Fall Time | — | — | — | ns | See Parameter DO31 **(Note 4)** |
| SP31 | TdoR | SDO2 Data Output Rise Time | — | — | — | ns | See Parameter DO31 **(Note 4)** |
| SP35 | TscH2doV, TscL2doV | SDO2 Data Output Valid after SCK2 Edge | — | 6 | 20 | ns | |
| SP36 | TdoV2scH, TdoV2scL | SDO2 Data Output Setup to First SCK2 Edge | 30 | — | — | ns | |
| SP40 | TdiV2scH, TdiV2scL | Setup Time of SDI2 Data Input to SCK2 Edge | 30 | — | — | ns | |
| SP41 | TscH2diL, TscL2diL | Hold Time of SDI2 Data Input to SCK2 Edge | 30 | — | — | ns | |
| SP50 | TssL2scH, TssL2scL | $\overline{SS2}$ ↓ to SCK2 ↑ or SCK2 ↓ Input | 120 | — | — | ns | |
| SP51 | TssH2doZ | $\overline{SS2}$ ↑ to SDO2 Output High-Impedance | 10 | — | 50 | ns | **(Note 4)** |
| SP52 | TscH2ssH TscL2ssH | $\overline{SS2}$ ↑ after SCK2 Edge | 1.5 TCY + 40 | — | — | ns | **(Note 4)** |

**Note 1:** These parameters are characterized, but are not tested in manufacturing.

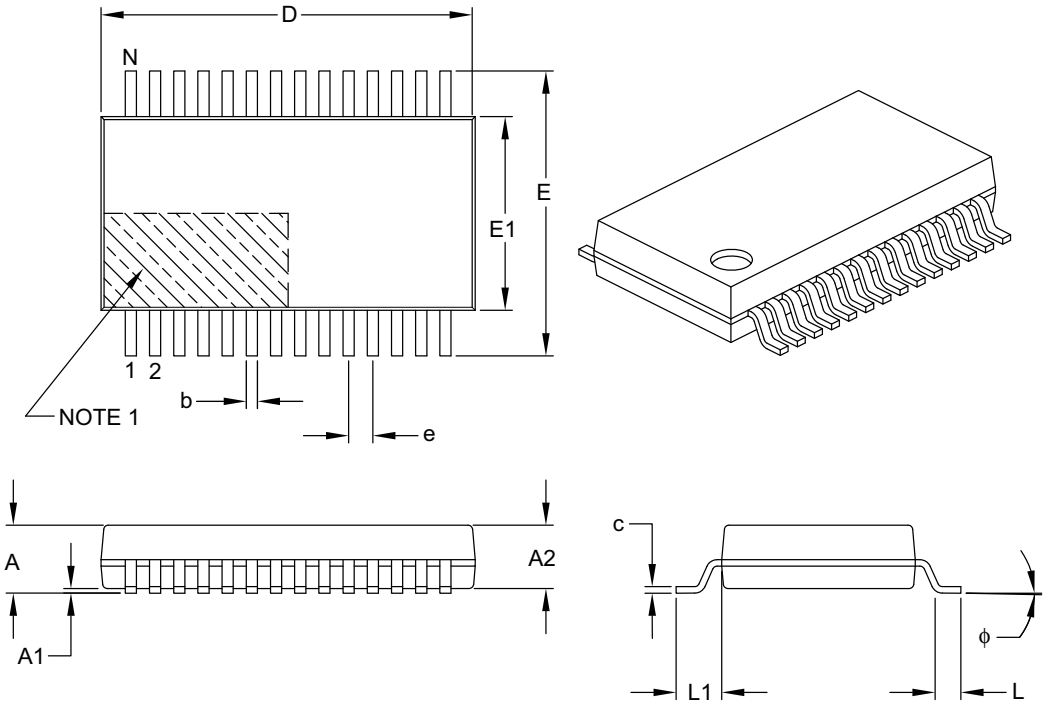
**2:** Data in "Typical" column is at 3.3V, +25°C unless otherwise stated.

**3:** The minimum clock period for SCK2 is 91 ns. Therefore, the SCK2 clock generated by the master must not violate this specification.

**4:** Assumes 50 pF load on all SPI2 pins.

## 28-Lead Plastic Shrink Small Outline (SS) – 5.30 mm Body [SSOP]

**Note:** For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging




| Units | | MILLIMETERS | | |
|---|---|---|---|---|
| Dimension Limits | | MIN | NOM | MAX |
| Number of Pins | N | | 28 | |
| Pitch | e | | 0.65 BSC | |
| Overall Height | A | – | – | 2.00 |
| Molded Package Thickness | A2 | 1.65 | 1.75 | 1.85 |
| Standoff | A1 | 0.05 | – | – |
| Overall Width | E | 7.40 | 7.80 | 8.20 |
| Molded Package Width | E1 | 5.00 | 5.30 | 5.60 |
| Overall Length | D | 9.90 | 10.20 | 10.50 |
| Foot Length | L | 0.55 | 0.75 | 0.95 |
| Footprint | L1 | | 1.25 REF | |
| Lead Thickness | c | 0.09 | – | 0.25 |
| Foot Angle | ϕ | 0° | 4° | 8° |
| Lead Width | b | 0.22 | – | 0.38 |

**Notes:**

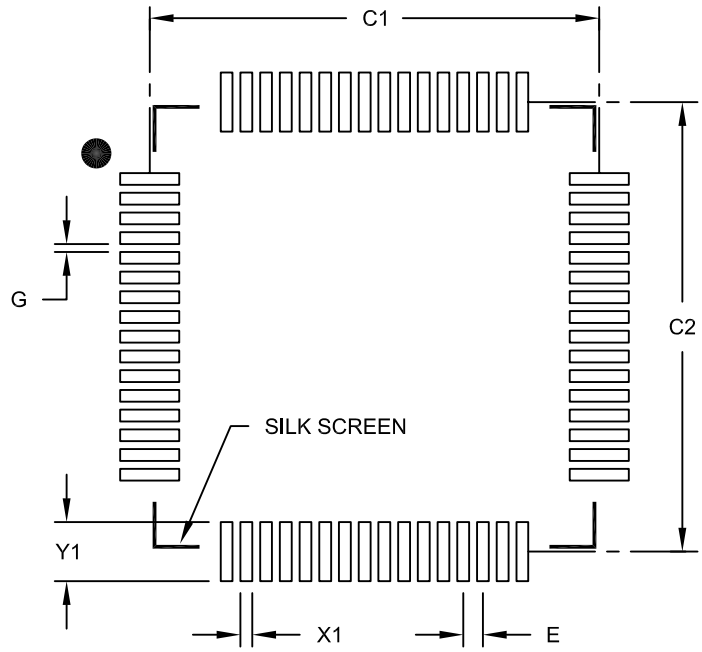
1. Pin 1 visual index feature may vary, but must be located within the hatched area.
2. Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.20 mm per side.
3. Dimensioning and tolerancing per ASME Y14.5M.

BSC: Basic Dimension. Theoretically exact value shown without tolerances.
REF: Reference Dimension, usually without tolerance, for information purposes only.

Microchip Technology Drawing C04-073B

64-Lead Plastic Thin Quad Flatpack (PT) 10x10x1 mm Body, 2.00 mm Footprint [TQFP]

**Note:** For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging




RECOMMENDED LAND PATTERN

| Units | | MILLIMETERS | | |
|---|---|---|---|---|
| Dimension Limits | | MIN | NOM | MAX |
| Contact Pitch | E | | 0.50 BSC | |
| Contact Pad Spacing | C1 | | 11.40 | |
| Contact Pad Spacing | C2 | | 11.40 | |
| Contact Pad Width (X64) | X1 | | | 0.30 |
| Contact Pad Length (X64) | Y1 | | | 1.50 |
| Distance Between Pads | G | 0.20 | | |

Notes:

1. Dimensioning and tolerancing per ASME Y14.5M

BSC: Basic Dimension. Theoretically exact value shown without tolerances.

Microchip Technology Drawing No. C04-2085B

**TABLE A-5: MAJOR SECTION UPDATES (CONTINUED)**

| Section Name | Update Description |
|---|---|
| **Section 30.0 "Electrical Characteristics"** | • Throughout: qualifies all footnotes relating to the operation of analog modules below VDDMIN (replaces "will have" with "may have")<br>• Throughout: changes all references of SPI timing parameter symbol "TscP" to "FscP"<br>• Table 30-1: changes VDD range to 3.0V to 3.6V<br>• Table 30-4: removes Parameter DC12 (RAM Retention Voltage)<br>• Table 30-7: updates Maximum values at 10 and 20 MIPS<br>• Table 30-8: adds Maximum IPD values, and removes all ΔIWDT entries<br>• Adds new Table 30-9 (Watchdog Timer Delta Current) with consolidated values removed from Table 30-8. All subsequent tables are renumbered accordingly.<br>• Table 30-10: adds footnote for all parameters for 1:2 Doze ratio<br>• Table 30-11:<br>- changes Minimum and Maximum values for D120 and D130<br>- adds Minimum and Maximum values for D131<br>- adds Minimum and Maximum values for D150 through D156, and removes Typical values<br>• Table 30-12:<br>- reformats table for readability<br>- changes IOL conditions for DO10<br>• Table 30-14: adds footnote to D135<br>• Table 30-17: changes Minimum and Maximum values for OS30<br>• Table 30-19:<br>- splits temperature range and adds new values for F20a<br>- reduces temperature range for F20b to extended temperatures only<br>• Table 30-20:<br>- splits temperature range and adds new values for F21a<br>- reduces temperature range for F20b to extended temperatures only<br>• Table 30-53:<br>- adds Maximum value to CM30<br>- adds footnote ("Parameter characterized...") to multiple parameters<br>• Table 30-55: adds Minimum and Maximum values for all CTMUI specifications, and removes Typical values<br>• Table 30-57: adds new footnote to AD09<br>• Table 30-58:<br>- removes all specifications for accuracy with external voltage references<br>- removes Typical values for AD23a and AD24a<br>- replaces Minimum and Maximum values for AD21a, AD22a, AD23a and AD24a with new values, split by Industrial and Extended temperatures<br>- removes Maximum value of AD30<br>- removes Minimum values from AD31a and AD32a<br>- adds or changes Typical values for AD30, AD31a, AD32a and AD33a<br>• Table 30-59:<br>- removes all specifications for accuracy with external voltage references<br>- removes Maximum value of AD30<br>- removes Typical values for AD23b and AD24b<br>- replaces Minimum and Maximum values for AD21b, AD22b, AD23b and AD24b with new values, split by Industrial and Extended temperatures<br>- removes Minimum and Maximum values from AD31b, AD32b, AD33b and AD34b<br>- adds or changes Typical values for AD30, AD31a, AD32a and AD33a<br>• Table 30-61: Adds footnote to AD51 |
| **Section 32.0 "DC and AC Device Characteristics Graphs"** | • Updates Figure 32-6 (Typical IDD @ 3.3V) with individual current vs. processor speed curves for the different program memory sizes |
| **Section 33.0 "Packaging Information"** | • Replaces drawing C04-149C (64-pin QFN, 7.15 x 7.15 exposed pad) with C04-154A (64-pin QFN, 5.4 x 5.4 exposed pad) |