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Applications of "<u>Embedded -</u> <u>Microcontrollers</u>"

Details

-XF

Product Status	Active
Core Processor	PIC
Core Size	16-Bit
Speed	70 MIPs
Connectivity	I²C, IrDA, LINbus, QEI, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, DMA, Motor Control PWM, POR, PWM, WDT
Number of I/O	21
Program Memory Size	128KB (43K x 24)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	8K x 16
Voltage - Supply (Vcc/Vdd)	3V ~ 3.6V
Data Converters	A/D 6x10b/12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	28-SSOP (0.209", 5.30mm Width)
Supplier Device Package	28-SSOP
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/pic24ep128mc202-i-ss

Email: info@E-XFL.COM

Address: Room A, 16/F, Full Win Commercial Centre, 573 Nathan Road, Mongkok, Hong Kong

TABLE	4-Z:	CPU		EGISTEI	RIMAP		Z4EPX		C20X D	EVICES	ONLT							
File Name	Addr.	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	All Resets
W0	0000								W0 (WR	EG)								xxxx
W1	0002								W1									xxxx
W2	0004								W2									xxxx
W3	0006								W3									xxxx
W4	8000								W4									xxxx
W5	000A								W5									xxxx
W6	000C								W6									xxxx
W7	000E								W7									xxxx
W8	0010								W8									xxxx
W9	0012								W9									xxxx
W10	0014								W10									xxxx
W11	0016								W11									xxxx
W12	0018								W12									xxxx
W13	001A								W13									xxxx
W14	001C								W14									xxxx
W15	001E								W15									xxxx
SPLIM	0020								SPLIM<1	5:0>								0000
PCL	002E			•			•	P	CL<15:1>								—	0000
PCH	0030	—	—	—	—	—	—		—	—				PCH<6:0>				0000
DSRPAG	0032	—	—	—	—	—	—					DSRPA	G<9:0>					0001
DSWPAG	0034	—	—	—	—	—	—	—				DS	SWPAG<8:0)>				0001
RCOUNT	0036			•			•		RCOUNT<	15:0>								0000
SR	0042	—	—		—	_	—	_	DC	IPL2	IPL1	IPL0	RA	N	OV	Z	С	0000
CORCON	0044	VAR	_	—	—	—	—	_	—	—	—	—	—	IPL3	SFA	—	—	0020
DISICNT	0052	—	-							DISICNT	<13:0>							0000
TBLPAG	0054	—	—	—	—	—	—	—	—				TBLPA	G<7:0>				0000
MSTRPR	0058								MSTRPR<	15:0>								0000

D I -4.0 - -

Legend: x = unknown value on Reset, — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

TABLE 4-6: INTERRUPT CONTROLLER REGISTER MAP FOR dsPIC33EPXXXMC20X DEVICES ONLY (CONTINUED)

File Name	Addr.	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	All Resets
IPC35	0886	_		JTAGIP<2:()>	—		ICDIP<2:0	>	_	—	—	—	—	_	—	—	4400
IPC36	0888			PTG0IP<2:0)>	—	PT	GWDTIP<	2:0>		P	TGSTEPIP<2	:0>	—	—		—	4440
IPC37	088A		_		_	—	F	PTG3IP<2:)>			PTG2IP<2:0	>	—	F	PTG1IP<2:0>		0444
INTCON1	08C0	NSTDIS	OVAERR	OVBERR	COVAERR	COVBERR	OVATE	OVBTE	COVTE	SFTACERR	DIV0ERR	DMACERR	MATHERR	ADDRERR	STKERR	OSCFAIL	—	0000
INTCON2	08C2	GIE	DISI	SWTRAP	—	_	_				—	—	—	—	INT2EP	INT1EP	INT0EP	8000
INTCON3	08C4		—		_	_	_				—	DAE	DOOVR	—	—		—	0000
INTCON4	08C6		—		_	_	_				—	—	—	—	—		SGHT	0000
INTTREG	08C8	_	_	_	_		ILR<	3:0>					VECNU	M<7:0>				0000

Legend: — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

TABLE 4-24: CRC REGISTER MAP

File Name	Addr.	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	All Resets
CRCCON1	0640	CRCEN	—	CSIDL		V	WORD<4:()>		CRCFUL	CRCMPT	CRCISEL	CRCGO	LENDIAN	—	-	—	0000
CRCCON2	0642	_	_	_		D	WIDTH<4:0)>		_	_	_		F	PLEN<4:0>			0000
CRCXORL	0644								X<15:1	>							_	0000
CRCXORH	0646								X	<31:16>								0000
CRCDATL	0648								CRC Data	Input Low V	Vord							0000
CRCDATH	064A								CRC Data	Input High \	Nord							0000
CRCWDATL	064C		CRC Result Low Word 0000								0000							
CRCWDATH	064E		CRC Result High Word 0000															

Legend: — = unimplemented, read as '0'. Shaded bits are not used in the operation of the programmable CRC module.

TABLE 4-25: PERIPHERAL PIN SELECT OUTPUT REGISTER MAP FOR dsPIC33EPXXXGP/MC202/502 AND PIC24EPXXXGP/MC202 DEVICES ONLY DEVICES ONLY

File Name	Addr.	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	All Resets
RPOR0	0680	_	—			RP35F	R<5:0>			—	—			RP20F	R<5:0>			0000
RPOR1	0682	_	_			RP37F	२<5:0>			—	_			RP36F	२<5:0>			0000
RPOR2	0684	_	_			RP39F	२<5:0>			—	_			RP38F	२<5:0>			0000
RPOR3	0686	_	_			RP41F	२<5:0>			—	_			RP40F	२<5:0>			0000
RPOR4	0688	_	—			RP43F	R<5:0>			_	_			RP42F	२<5:0>			0000

Legend: — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

TABLE 4-26: PERIPHERAL PIN SELECT OUTPUT REGISTER MAP FOR dsPIC33EPXXXGP/MC203/503 AND PIC24EPXXXGP/MC203 DEVICES ONLY DEVICES ONLY

File Name	Addr.	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	All Resets
RPOR0	0680	—	_			RP35	R<5:0>			_	_			RP20	R<5:0>			0000
RPOR1	0682	_	_			RP37	२<5:0>			_	_			RP36	२<5:0>			0000
RPOR2	0684	_	_			RP39	२<5:0>			_	_			RP38	२<5:0>			0000
RPOR3	0686	_	_			RP41	२<5:0>			_	_			RP40	२<5:0>			0000
RPOR4	0688	_	_			RP43	२<5:0>			_	_			RP42	२<5:0>			0000
RPOR5	068A	_	_	_	_	_	_	_	_	_	_	_	_	_	_	_	_	0000
RPOR6	068C			-	—	_		—			_			RP56	R<5:0>			0000

Legend: — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

10.0 POWER-SAVING FEATURES

- Note 1: This data sheet summarizes the features of the dsPIC33EPXXXGP50X, dsPIC33EPXXXMC20X/50X and PIC24EPXXXGP/MC20X families of devices. It is not intended to be a comprehensive reference source. To complement the information in this data sheet, refer to "Watchdog Timer and Power-Saving Modes" (DS70615) in the "dsPIC33/ PIC24 Family Reference Manual", which is available from the Microchip web site (www.microchip.com).
 - Some registers and associated bits described in this section may not be available on all devices. Refer to Section 4.0 "Memory Organization" in this data sheet for device-specific register and bit information.

The dsPIC33EPXXXGP50X, dsPIC33EPXXXMC20X/ 50X and PIC24EPXXXGP/MC20X devices provide the ability to manage power consumption by selectively managing clocking to the CPU and the peripherals. In general, a lower clock frequency and a reduction in the number of peripherals being clocked constitutes lower consumed power.

dsPIC33EPXXXGP50X, dsPIC33EPXXXMC20X/50X and PIC24EPXXXGP/MC20X devices can manage power consumption in four ways:

- Clock Frequency
- Instruction-Based Sleep and Idle modes
- Software-Controlled Doze mode
- · Selective Peripheral Control in Software

Combinations of these methods can be used to selectively tailor an application's power consumption while still maintaining critical application features, such as timing-sensitive communications.

EXAMPLE 10-1: PWRSAV INSTRUCTION SYNTAX

PWRSAV	#SLEEP_MODE	;	Put	the	device	into	Sleep mode
PWRSAV	#IDLE_MODE	;	Put	the	device	into	Idle mode

10.1 Clock Frequency and Clock Switching

The dsPIC33EPXXXGP50X, dsPIC33EPXXXMC20X/ 50X and PIC24EPXXXGP/MC20X devices allow a wide range of clock frequencies to be selected under application control. If the system clock configuration is not locked, users can choose low-power or highprecision oscillators by simply changing the NOSCx bits (OSCCON<10:8>). The process of changing a system clock during operation, as well as limitations to the process, are discussed in more detail in **Section 9.0 "Oscillator Configuration"**.

10.2 Instruction-Based Power-Saving Modes

The dsPIC33EPXXXGP50X, dsPIC33EPXXXMC20X/ 50X and PIC24EPXXXGP/MC20X devices have two special power-saving modes that are entered through the execution of a special PWRSAV instruction. Sleep mode stops clock operation and halts all code execution. Idle mode halts the CPU and code execution, but allows peripheral modules to continue operation. The assembler syntax of the PWRSAV instruction is shown in Example 10-1.

Note: SLEEP_MODE and IDLE_MODE are constants defined in the assembler include file for the selected device.

Sleep and Idle modes can be exited as a result of an enabled interrupt, WDT time-out or a device Reset. When the device exits these modes, it is said to "wake-up".

10.3 Doze Mode

The preferred strategies for reducing power consumption are changing clock speed and invoking one of the powersaving modes. In some circumstances, this cannot be practical. For example, it may be necessary for an application to maintain uninterrupted synchronous communication, even while it is doing nothing else. Reducing system clock speed can introduce communication errors, while using a power-saving mode can stop communications completely.

Doze mode is a simple and effective alternative method to reduce power consumption while the device is still executing code. In this mode, the system clock continues to operate from the same source and at the same speed. Peripheral modules continue to be clocked at the same speed, while the CPU clock speed is reduced. Synchronization between the two clock domains is maintained, allowing the peripherals to access the SFRs while the CPU executes code at a slower rate.

Doze mode is enabled by setting the DOZEN bit (CLKDIV<11>). The ratio between peripheral and core clock speed is determined by the DOZE<2:0> bits (CLKDIV<14:12>). There are eight possible configurations, from 1:1 to 1:128, with 1:1 being the default setting.

Programs can use Doze mode to selectively reduce power consumption in event-driven applications. This allows clock-sensitive functions, such as synchronous communications, to continue without interruption while the CPU Idles, waiting for something to invoke an interrupt routine. An automatic return to full-speed CPU operation on interrupts can be enabled by setting the ROI bit (CLKDIV<15>). By default, interrupt events have no effect on Doze mode operation.

For example, suppose the device is operating at 20 MIPS and the ECAN[™] module has been configured for 500 kbps, based on this device operating speed. If the device is placed in Doze mode with a clock frequency ratio of 1:4, the ECAN module continues to communicate at the required bit rate of 500 kbps, but the CPU now starts executing instructions at a frequency of 5 MIPS.

10.4 Peripheral Module Disable

The Peripheral Module Disable (PMD) registers provide a method to disable a peripheral module by stopping all clock sources supplied to that module. When a peripheral is disabled using the appropriate PMD control bit, the peripheral is in a minimum power consumption state. The control and status registers associated with the peripheral are also disabled, so writes to those registers do not have effect and read values are invalid.

A peripheral module is enabled only if both the associated bit in the PMD register is cleared and the peripheral is supported by the specific dsPIC[®] DSC variant. If the peripheral is present in the device, it is enabled in the PMD register by default.

Note:	If a PMD bit is set, the corresponding
	module is disabled after a delay of one
	instruction cycle. Similarly, if a PMD bit is
	cleared, the corresponding module is
	enabled after a delay of one instruction
	cycle (assuming the module control regis-
	ters are already configured to enable
	module operation).

10.5 Power-Saving Resources

Many useful resources are provided on the main product page of the Microchip web site for the devices listed in this data sheet. This product page, which can be accessed using this link, contains the latest updates and additional information.



10.5.1 KEY RESOURCES

- "Watchdog Timer and Power-Saving Modes" (DS70615) in the "dsPIC33/PIC24 Family Reference Manual"
- Code Samples
- Application Notes
- Software Libraries
- Webinars
- All Related "dsPIC33/PIC24 Family Reference Manual" Sections
- Development Tools

dsPIC33EPXXXGP50X, dsPIC33EPXXXMC20X/50X AND PIC24EPXXXGP/MC20X

U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
_		—	—	—	—	—	—
bit 15							bit 8
U-0	U-0	U-0	R/W-0	R/W-0	U-0	U-0	U-0
			DMA0MD ⁽¹⁾				
_	_	_	DMA1MD ⁽¹⁾	PTGMD	_	_	_
			DMA2MD ⁽¹⁾	1 TOME			
			DMA3MD ⁽¹⁾				
bit 7							bit 0
Legend:							
R = Readable	e bit	W = Writable	bit	U = Unimplem	nented bit, read	l as '0'	
-n = Value at	POR	'1' = Bit is set		'0' = Bit is clea	ared	x = Bit is unkn	iown
bit 15-5	Unimplement	ted: Read as '	D'				
bit 4	DMA0MD: DN	/A0 Module Di	sable bit ⁽¹⁾				
	1 = DMA0 mo	dule is disable	d				
	0 = DMA0 mo	dule is enable	d 				
	DMA1MD: DN	/A1 Module Di	sable bit(")				
	1 = DMA1 mo 0 = DMA1 mo	dule is disable	d d				
			sable bit(1)				
	1 = DMA2 mo	dule is disable	d				
	0 = DMA2 mo	dule is enable	d				
	DMA3MD: DN	/A3 Module Di	sable bit ⁽¹⁾				
	1 = DMA3 mo	dule is disable	d				
	0 = DMA3 mo	dule is enable	b				
bit 3	PTGMD: PTG	Module Disab	le bit				
	1 = PTG mod	ule is disabled					
	$0 = PIG \mod 1$	uie is enabled	-1				
DIT 2-0	Unimplement	tea: Read as '	J.				
Note 1: Th	nis single bit ena	ables and disat	oles all four DM	A channels.			

REGISTER 10-6: PMD7: PERIPHERAL MODULE DISABLE CONTROL REGISTER 7

REGISTER 11-7: RPINR12: PERIPHERAL PIN SELECT INPUT REGISTER 12 (dsPIC33EPXXXMC20X/50X and PIC24EPXXXMC20X DEVICES ONLY)

U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
_				FLT2R<6:0>			
bit 15							bit 8
U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
				FLT1R<6:0>			
bit 7							bit 0
Legend:							
R = Readab	ole bit	W = Writable	bit	U = Unimplen	nented bit, rea	ad as '0'	
-n = Value a	at POR	'1' = Bit is set		'0' = Bit is cle	ared	x = Bit is unki	nown
bit 15	Unimpleme	ented: Read as '	0'				
bit 14-8	FLT2R<6:0: (see Table 1	Assign PWM 1-2 for input pin	Fault 2 (FLT2 selection nur) to the Corresp mbers)	onding RPn F	Pin bits	
	1111001 =	Input tied to RPI	121				
	•						
	•						
	0000001 =	Input tied to CM	P1				
	0000000 =	Input tied to Vss	5				
bit 7	Unimpleme	ented: Read as '	0'				
bit 6-0	FLT1R<6:0: (see Table 1	Second States	Fault 1 (FLT1 selection nur) to the Corresp nbers)	onding RPn F	Pin bits	
	1111001 =	Input tied to RPI	121				
	•						
	-						
		Input tied to CM	P1				
	0000000 =	Input tied to Vss	; ;				

REGISTER 11-17: RPINR39: PERIPHERAL PIN SELECT INPUT REGISTER 39 (dsPIC33EPXXXMC20X/50X AND PIC24EPXXXMC20X DEVICES ONLY)

	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
—				DTCMP3R<6:0)>		
bit 15							bit 8
U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
				DTCMP2R<6:0)>		
bit 7							bit 0
Legend:							
R = Readab	le bit	W = Writable I	oit	U = Unimplen	nented bit, rea	ad as '0'	
-n = Value a	t POR	'1' = Bit is set		'0' = Bit is clea	ared	x = Bit is unkr	nown
bit 14-8	DTCMP3R< (see Table 1 1111001 =	6:0>: Assign PW 1-2 for input pin nput tied to RPI	/M Dead-Tim selection nun 121	e Compensatio nbers)	n Input 3 to th	ne Corresponding	g RPn Pin bits
	0000001 = 0000000 =	nput tied to CMI nput tied to Vss	P1				
bit 7	0000001 = 0000000 = Unimpleme	nput tied to CMI nput tied to Vss nted: Read as '0	21)'				

12.0 TIMER1

- Note 1: This data sheet summarizes the features of the dsPIC33EPXXXGP50X, dsPIC33EPXXXMC20X/50X and PIC24EPXXXGP/MC20X families of devices. It is not intended to be a comprehensive reference source. To complement the information in this data sheet, refer to "Timers" (DS70362) in the "dsPIC33/PIC24 Family Reference Manual", which is available from the Microchip web site (www.microchip.com).
 - 2: Some registers and associated bits described in this section may not be available on all devices. Refer to Section 4.0 "Memory Organization" in this data sheet for device-specific register and bit information.

The Timer1 module is a 16-bit timer that can operate as a free-running interval timer/counter.

The Timer1 module has the following unique features over other timers:

- Can be operated in Asynchronous Counter mode from an external clock source
- The external clock input (T1CK) can optionally be synchronized to the internal device clock and the clock synchronization is performed after the prescaler
- A block diagram of Timer1 is shown in Figure 12-1.

The Timer1 module can operate in one of the following modes:

- Timer mode
- · Gated Timer mode
- Synchronous Counter mode
- · Asynchronous Counter mode

In Timer and Gated Timer modes, the input clock is derived from the internal instruction cycle clock (FCY). In Synchronous and Asynchronous Counter modes, the input clock is derived from the external clock input at the T1CK pin.

The Timer modes are determined by the following bits:

- Timer Clock Source Control bit (TCS): T1CON<1>
- Timer Synchronization Control bit (TSYNC): T1CON<2>
- Timer Gate Control bit (TGATE): T1CON<6>

Timer control bit setting for different operating modes are given in the Table 12-1.

Mode	TCS	TGATE	TSYNC
Timer	0	0	x
Gated Timer	0	1	х
Synchronous Counter	1	x	1
Asynchronous Counter	1	x	0

TABLE 12-1: TIMER MODE SETTINGS

FIGURE 12-1: 16-BIT TIMER1 MODULE BLOCK DIAGRAM



12.1 Timer1 Resources

Many useful resources are provided on the main product page of the Microchip web site for the devices listed in this data sheet. This product page, which can be accessed using this link, contains the latest updates and additional information.

Note:	In the event you are not able to access the
	product page using the link above, enter
	this URL in your browser:
	http://www.microchip.com/wwwproducts/
	Devices.aspx?dDocName=en555464

12.1.1 KEY RESOURCES

- "Timers" (DS70362) in the "dsPIC33/PIC24 Family Reference Manual"
- · Code Samples
- Application Notes
- · Software Libraries
- Webinars
- All Related "dsPIC33/PIC24 Family Reference Manual" Sections
- Development Tools

13.0 TIMER2/3 AND TIMER4/5

- Note 1: This data sheet summarizes the features of the dsPIC33EPXXXGP50X, dsPIC33EPXXXMC20X/50X and PIC24EPXXXGP/MC20X family of devices. It is not intended to be a comprehensive reference source. To complement the information in this data sheet, refer to "Timers" (DS70362) of the "dsPIC33/PIC24 Family Reference Manual", which is available from the Microchip web site (www.microchip.com).
 - 2: Some registers and associated bits described in this section may not be available on all devices. Refer to **Section 4.0 "Memory Organization"** in this data sheet for device-specific register and bit information.

The Timer2/3 and Timer4/5 modules are 32-bit timers, which can also be configured as four independent 16-bit timers with selectable operating modes.

As 32-bit timers, Timer2/3 and Timer4/5 operate in three modes:

- Two Independent 16-Bit Timers (e.g., Timer2 and Timer3) with all 16-Bit Operating modes (except Asynchronous Counter mode)
- Single 32-Bit Timer
- Single 32-Bit Synchronous Counter
- They also support these features:
- Timer Gate Operation
- Selectable Prescaler Settings
- Timer Operation during Idle and Sleep modes
- Interrupt on a 32-Bit Period Register Match
- Time Base for Input Capture and Output Compare Modules (Timer2 and Timer3 only)
- ADC1 Event Trigger (32-bit timer pairs, and Timer3 and Timer5 only)

Individually, all four of the 16-bit timers can function as synchronous timers or counters. They also offer the features listed previously, except for the event trigger; this is implemented only with Timer2/3. The operating modes and enabled features are determined by setting the appropriate bit(s) in the T2CON, T3CON, and T4CON, T5CON registers. T2CON and T4CON are shown in generic form in Register 13-1. T3CON and T5CON are shown in Register 13-2.

For 32-bit timer/counter operation, Timer2 and Timer4 are the least significant word (lsw); Timer3 and Timer5 are the most significant word (msw) of the 32-bit timers.

Note: For 32-bit operation, T3CON and T5CON control bits are ignored. Only T2CON and T4CON control bits are used for setup and control. Timer2 and Timer4 clock and gate inputs are utilized for the 32-bit timer modules, but an interrupt is generated with the Timer3 and Timer5 interrupt flags.

A block diagram for an example 32-bit timer pair (Timer2/3 and Timer4/5) is shown in Figure 13-3.

Note: Only Timer2, 3, 4 and 5 can trigger a DMA data transfer.

15.1 Output Compare Resources

Many useful resources are provided on the main product page of the Microchip web site for the devices listed in this data sheet. This product page, which can be accessed using this link, contains the latest updates and additional information.

Note:	In the event you are not able to access the
	product page using the link above, enter
	this URL in your browser:
	http://www.microchip.com/wwwproducts/
	Devices.aspx?dDocName=en555464

15.1.1 KEY RESOURCES

- "Output Compare" (DS70358) in the "dsPIC33/ PIC24 Family Reference Manual"
- · Code Samples
- Application Notes
- Software Libraries
- Webinars
- All Related "dsPIC33/PIC24 Family Reference Manual" Sections
- Development Tools

17.2 QEI Control Registers

|--|

R/W-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0			
QEIEN		QEISIDL	PIMOD2 ⁽¹⁾	PIMOD1 ⁽¹⁾ PIMOD0 ⁽¹⁾		IMV1 ⁽²⁾	IMV0 ⁽²⁾			
bit 15	it 15									
U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0			
_	INTDIV2 ⁽³⁾	INTDIV1 ⁽³⁾	INTDIV0 ⁽³⁾	CNTPOL	GATEN	CCM1	CCM0			
bit 7							bit 0			
Legend:										
R = Readable	bit	W = Writable	bit	U = Unimpler	nented bit, read	l as '0'				
-n = Value at I	POR	'1' = Bit is set		'0' = Bit is cle	ared	x = Bit is unkr	Iown			
bit 15	bit 15 QEIEN: Quadrature Encoder Interface Module Counter Enable bit 1 = Module counters are enabled 0 = Module counters are disabled, but SFRs can be read or written to									
bit 14	Unimplemen	ted: Read as 'o)'							
bit 13	QEISIDL: QE	I Stop in Idle M	ode bit							
	1 = Discontinues	ues module opera module opera	eration when c tion in Idle mo	levice enters I de	dle mode					
bit 12-10	PIMOD<2:0>	: Position Coun	iter Initializatio	n Mode Selec	t bits ⁽¹⁾					
	 111 = Reserved 110 = Modulo Count mode for position counter 101 = Resets the position counter when the position counter equals QEI1GEC register 100 = Second index event after home event initializes position counter with contents of QEI1IC register 011 = First index event after home event initializes position counter with contents of QEI1IC register 010 = Next index input event initializes the position counter with contents of QEI1IC register 010 = Next index input event resets the position counter 001 = Every index input event resets the position counter 									
bit 9	IMV1: Index N	Match Value for	Phase B bit ⁽²)						
	1 = Phase B match occurs when QEB = 1 0 = Phase B match occurs when QEB = 0									
bit 8	IMV0: Index N	Match Value for	Phase A bit ⁽²⁾)						
	1 = Phase A r 0 = Phase A r	match occurs w match occurs w	/hen QEA = 1 /hen QEA = 0							
bit 7	Unimplemen	ted: Read as 'o	י)							
	0014.4.0		(II) OF							

Note 1: When CCM<1:0> = 10 or 11, all of the QEI counters operate as timers and the PIMOD<2:0> bits are ignored.

2: When CCM<1:0> = 00, and QEA and QEB values match the Index Match Value (IMV), the POSCNTH and POSCNTL registers are reset. QEA/QEB signals used for the index match have swap and polarity values applied, as determined by the SWPAB and QEAPOL/QEBPOL bits.

3: The selected clock rate should be at least twice the expected maximum quadrature count rate.

BUFFER 21-5: ECAN™ MESSAGE BUFFER WORD 4

R = Readable bit W = Writabl		W = Writable b	it	U = Unimplemented bit, read as '0' (0' = Pit is cleared $x = Pit$ is unknown								
Legend:												
bit 7							bit 0					
	Byte 2											
R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x					
bit 15							bit 8					
			Ву	rte 3								
R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x					

bit 15-8 Byte 3<15:8>: ECAN Message Byte 3 bits

bit 7-0 Byte 2<7:0>: ECAN Message Byte 2 bits

BUFFER 21-6: ECAN™ MESSAGE BUFFER WORD 5

R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x
			Ву	/te 5			
bit 15							bit 8
R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x
			Ву	/te 4			
bit 7							bit 0
Legend:							
R = Readable bit W = Writable bit			bit	U = Unimplemented bit, read as '0'			
-n = Value at POR '1'		'1' = Bit is set	'1' = Bit is set		ared	x = Bit is unknown	
-							

bit 15-8 Byte 5<15:8>: ECAN Message Byte 5 bits

bit 7-0 Byte 4<7:0>: ECAN Message Byte 4 bits

REGISTER 24-3: PTGBTE: PTG BROADCAST TRIGGER ENABLE REGISTER^(1,2) (CONTINUED)

bit 4	OC1CS: Clock Source for OC1 bit
	 1 = Generates clock pulse when the broadcast command is executed 0 = Does not generate clock pulse when the broadcast command is executed
bit 3	OC4TSS: Trigger/Synchronization Source for OC4 bit
	 1 = Generates Trigger/Synchronization when the broadcast command is executed 0 = Does not generate Trigger/Synchronization when the broadcast command is executed
bit 2	OC3TSS: Trigger/Synchronization Source for OC3 bit
	 1 = Generates Trigger/Synchronization when the broadcast command is executed 0 = Does not generate Trigger/Synchronization when the broadcast command is executed
bit 1	OC2TSS: Trigger/Synchronization Source for OC2 bit
	 1 = Generates Trigger/Synchronization when the broadcast command is executed 0 = Does not generate Trigger/Synchronization when the broadcast command is executed
bit 0	OC1TSS: Trigger/Synchronization Source for OC1 bit
	 1 = Generates Trigger/Synchronization when the broadcast command is executed 0 = Does not generate Trigger/Synchronization when the broadcast command is executed

- **Note 1:** This register is read-only when the PTG module is executing Step commands (PTGEN = 1 and PTGSTRT = 1).
 - 2: This register is only used with the PTGCTRL OPTION = 1111 Step command.

U-0	U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0			
		—	DWIDTH4	DWIDTH3	DWIDTH2	DWIDTH1	DWIDTH0			
bit 15							bit 8			
U-0	U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0			
		—	PLEN4	PLEN3	PLEN2	PLEN1	PLEN0			
bit 7							bit 0			
Legend:										
R = Readable	bit	W = Writable	bit	U = Unimpler	nented bit, read	as '0'				
-n = Value at F	POR	'1' = Bit is set		'0' = Bit is cleared x = Bit is unknown			nown			
bit 15-13	bit 15-13 Unimplemented: Read as '0'									
bit 12-8	12-8 DWIDTH<4:0>: Data Width Select bits									
	These bits set the width of the data word (DWIDTH<4:0> + 1).									
bit 7-5	bit 7-5 Unimplemented: Read as '0'									

REGISTER 26-2: CRCCON2: CRC CONTROL REGISTER 2

bit 4-0 **PLEN<4:0>:** Polynomial Length Select bits

These bits set the length of the polynomial (Polynomial Length = PLEN<4:0> + 1).

dsPIC33EPXXXGP50X, dsPIC33EPXXXMC20X/50X AND PIC24EPXXXGP/MC20X

REGISTER 27-1: DEVID: DEVICE ID REGISTER

R	R	R	R	R	R	R	R					
	DEVID<23:16> ⁽¹⁾											
bit 23							bit 16					
R	R	R	R	R	R	R	R					
	DEVID<15:8> ⁽¹⁾											
bit 15							bit 8					
R	R	R	R	R	R	R	R					
			DEVID<	7:0> ⁽¹⁾								
bit 7							bit 0					
Legend:	egend: R = Read-Only bit U = Unimplemented bit											

bit 23-0 **DEVID<23:0>:** Device Identifier bits⁽¹⁾

Note 1: Refer to the "dsPIC33E/PIC24E Flash Programming Specification for Devices with Volatile Configuration *Bits*" (DS70663) for the list of device ID values.

REGISTER 27-2: DEVREV: DEVICE REVISION REGISTER

R	R	R	R	R	R	R	R					
DEVREV<23:16> ⁽¹⁾												
bit 23							bit 16					
R	R	R	R	R	R	R	R					
	DEVREV<15:8> ⁽¹⁾											
bit 15							bit 8					
R	R	R	R	R	R	R	R					
			DEVRE	/<7:0> ⁽¹⁾								
bit 7							bit 0					
Legend:	R = Read-only bit			U = Unimpler	nented bit							

bit 23-0 **DEVREV<23:0>:** Device Revision bits⁽¹⁾

Note 1: Refer to the "dsPIC33E/PIC24E Flash Programming Specification for Devices with Volatile Configuration *Bits*" (DS70663) for the list of device revision values.

DC CHARACTERISTICS		$\begin{tabular}{ l l l l l l l l l l l l l l l l l l l$						
Param No.	Symbol	Characteristic	Min. Typ. Max. Units Conditions					
Operating Voltage								
DC10	Vdd	Supply Voltage	3.0	_	3.6	V		
DC16	VPOR	VDD Start Voltage to Ensure Internal Power-on Reset Signal	_	_	Vss	V		
DC17	Svdd	VDD Rise Rate to Ensure Internal Power-on Reset Signal	0.03	—	—	V/ms	0V-1V in 100 ms	

TABLE 30-4: DC TEMPERATURE AND VOLTAGE SPECIFICATIONS

Note 1: Device is functional at VBORMIN < VDD < VDDMIN. Analog modules (ADC, op amp/comparator and comparator voltage reference) may have degraded performance. Device functionality is tested but not characterized. Refer to Parameter BO10 in Table 30-13 for the minimum and maximum BOR values.

TABLE 30-5: FILTER CAPACITOR (CEFC) SPECIFICATIONS

Standard Operating	$\begin{array}{llllllllllllllllllllllllllllllllllll$								
Param No.SymbolCharacteristicsMin.Typ.Max.UnitsComments									
	Cefc	External Filter Capacitor Value ⁽¹⁾	4.7	10		μF	Capacitor must have a low series resistance (< 1 Ohm)		

Note 1: Typical VCAP voltage = 1.8 volts when VDD \ge VDDMIN.

TABLE 30-46:SPI1 SLAVE MODE (FULL-DUPLEX, CKE = 1, CKP = 1, SMP = 0)TIMING REQUIREMENTS

АС СНА	ARACTERIS	TICS	$\begin{array}{l} \mbox{Standard Operating Conditions: 3.0V to 3.6V} \\ \mbox{(unless otherwise stated)} \\ \mbox{Operating temperature} & -40^{\circ}C \leq TA \leq +85^{\circ}C \mbox{ for Industrial} \\ & -40^{\circ}C \leq TA \leq +125^{\circ}C \mbox{ for Extended} \end{array}$				
Param.	Symbol	Characteristic ⁽¹⁾	Min.	Typ. ⁽²⁾	Max.	Units	Conditions
SP70	FscP	Maximum SCK1 Input Frequency	—	—	Lesserof FP or 11	MHz	(Note 3)
SP72	TscF	SCK1 Input Fall Time	—	_	_	ns	See Parameter DO32 (Note 4)
SP73	TscR	SCK1 Input Rise Time	—	_	_	ns	See Parameter DO31 (Note 4)
SP30	TdoF	SDO1 Data Output Fall Time	—	—	—	ns	See Parameter DO32 (Note 4)
SP31	TdoR	SDO1 Data Output Rise Time	—	-	—	ns	See Parameter DO31 (Note 4)
SP35	TscH2doV, TscL2doV	SDO1 Data Output Valid after SCK1 Edge	—	6	20	ns	
SP36	TdoV2scH, TdoV2scL	SDO1 Data Output Setup to First SCK1 Edge	30	—	—	ns	
SP40	TdiV2scH, TdiV2scL	Setup Time of SDI1 Data Input to SCK1 Edge	30	-	—	ns	
SP41	TscH2diL, TscL2diL	Hold Time of SDI1 Data Input to SCK1 Edge	30	-	—	ns	
SP50	TssL2scH, TssL2scL	$\overline{SS1}$ ↓ to SCK1 ↑ or SCK1 ↓ Input	120	—	—	ns	
SP51	TssH2doZ	SS1 ↑ to SDO1 Output High-Impedance	10	—	50	ns	(Note 4)
SP52	TscH2ssH, TscL2ssH	SS1 ↑ after SCK1 Edge	1.5 Tcy + 40	—	—	ns	(Note 4)
SP60	TssL2doV	SDO1 Data Output Valid after SS1 Edge	—	_	50	ns	

Note 1: These parameters are characterized, but are not tested in manufacturing.

2: Data in "Typical" column is at 3.3V, +25°C unless otherwise stated.

3: The minimum clock period for SCK1 is 91 ns. Therefore, the SCK1 clock generated by the master must not violate this specification.

4: Assumes 50 pF load on all SPI1 pins.

Section Name	Update Description
Section 30.0 "Electrical	These SPI2 Timing Requirements were updated:
Characteristics" (Continued)	 Maximum value for Parameter SP10 and the minimum clock period value for SCKx in Note 3 (see Table 30-36, Table 30-37, and Table 30-38)
	 Maximum value for Parameter SP70 and the minimum clock period value for SCKx in Note 3 (see Table 30-40 and Table 30-42)
	The Maximum Data Rate values were updated for the SPI2 Maximum Data/Clock Rate Summary (see Table 30-43)
	These SPI1 Timing Requirements were updated:
	 Maximum value for Parameters SP10 and the minimum clock period value for SCKx in Note 3 (see Table 30-44, Table 30-45, and Table 30-46)
	 Maximum value for Parameters SP70 and the minimum clock period value for SCKx in Note 3 (see Table 30-47 through Table 30-50)
	 Minimum value for Parameters SP40 and SP41 see Table 30-44 through Table 30-50)
	Updated all Typical values for the CTMU Current Source Specifications (see Table 30-55).
	Updated Note1, the Maximum value for Parameter AD06, the Minimum value for AD07, and the Typical values for AD09 in the ADC Module Specifications (see Table 30-56).
	Added Note 1 to the ADC Module Specifications (12-bit Mode) (see Table 30-57).
	Added Note 1 to the ADC Module Specifications (10-bit Mode) (see Table 30-58).
	Updated the Minimum and Maximum values for Parameter AD21b in the 10-bit Mode ADC Module Specifications (see Table 30-58).
	Updated Note 2 in the ADC Conversion (12-bit Mode) Timing Requirements (see Table 30-59).
	Updated Note 1 in the ADC Conversion (10-bit Mode) Timing Requirements (see Table 30-60).

TABLE A-2: MAJOR SECTION UPDATES (CONTINUED)