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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "<u>Embedded -</u> <u>Microcontrollers</u>"

Details

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Product Status	Obsolete
Core Processor	PIC
Core Size	16-Bit
Speed	60 MIPs
Connectivity	I ² C, IrDA, LINbus, QEI, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, DMA, Motor Control PWM, POR, PWM, WDT
Number of I/O	35
Program Memory Size	128KB (43K x 24)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	8K x 16
Voltage - Supply (Vcc/Vdd)	3V ~ 3.6V
Data Converters	A/D 9x10b/12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 150°C (TA)
Mounting Type	Surface Mount
Package / Case	44-VQFN Exposed Pad
Supplier Device Package	44-QFN (8x8)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/pic24ep128mc204-h-ml

Email: info@E-XFL.COM

Address: Room A, 16/F, Full Win Commercial Centre, 573 Nathan Road, Mongkok, Hong Kong

Pin Diagrams (Continued)



2.7 Oscillator Value Conditions on Device Start-up

If the PLL of the target device is enabled and configured for the device start-up oscillator, the maximum oscillator source frequency must be limited to 3 MHz < F_{IN} < 5.5 MHz to comply with device PLL start-up conditions. This means that if the external oscillator frequency is outside this range, the application must start-up in the FRC mode first. The default PLL settings after a POR with an oscillator frequency outside this range will violate the device operating speed.

Once the device powers up, the application firmware can initialize the PLL SFRs, CLKDIV and PLLFBD, to a suitable value, and then perform a clock switch to the Oscillator + PLL clock source. Note that clock switching must be enabled in the device Configuration Word.

2.8 Unused I/Os

Unused I/O pins should be configured as outputs and driven to a logic low state.

Alternatively, connect a 1k to 10k resistor between Vss and unused pins, and drive the output to logic low.

2.9 Application Examples

- · Induction heating
- Uninterruptable Power Supplies (UPS)
- DC/AC inverters
- · Compressor motor control
- · Washing machine 3-phase motor control
- BLDC motor control
- · Automotive HVAC, cooling fans, fuel pumps
- Stepper motor control
- · Audio and fluid sensor monitoring
- · Camera lens focus and stability control
- Speech (playback, hands-free kits, answering machines, VoIP)
- Consumer audio
- Industrial and building control (security systems and access control)
- · Barcode reading
- Networking: LAN switches, gateways
- Data storage device management
- · Smart cards and smart card readers

Examples of typical application connections are shown in Figure 2-4 through Figure 2-8.

FIGURE 2-4: BOOST CONVERTER IMPLEMENTATION



REGISTER 3-2: CORCON: CORE CONTROL REGISTER (CONTINUED)

bit 2	SFA: Stack Frame Active Status bit
	1 = Stack frame is active; W14 and W15 address 0x0000 to 0xFFFF, regardless of DSRPAG and
	DSWPAG values
	0 = Stack frame is not active; W14 and W15 address of EDS or Base Data Space
hit 1	PND: Dounding Mode Select hit(1)

- bit 1 **RND:** Rounding Mode Select bit⁽¹⁾
 - 1 = Biased (conventional) rounding is enabled
 - 0 = Unbiased (convergent) rounding is enabled

bit 0 IF: Integer or Fractional Multiplier Mode Select bit⁽¹⁾ 1 = Integer mode is enabled for DSP multiply 0 = Fractional mode is enabled for DSP multiply

- Note 1: This bit is available on dsPIC33EPXXXMC20X/50X and dsPIC33EPXXXGP50X devices only.
 - **2:** This bit is always read as '0'.
 - 3: The IPL3 bit is concatenated with the IPL<2:0> bits (SR<7:5>) to form the CPU Interrupt Priority Level.

TABLE 4	-12:	PWM RI	EGISTE	R MAP	FOR de	sPIC33E	PXXXN	AC20X/50	DX AND F	PIC24EP	PXXXM	C20X [DEVICE	S ONI	_Y			
File Name	Addr.	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	All Resets
PTCON	0C00	PTEN	—	PTSIDL	SESTAT	SEIEN	EIPU	SYNCPOL	SYNCOEN	SYNCEN	SY	NCSRC<	2:0>	SEVTPS<3:0>			0000	
PTCON2	0C02	_	—	_	_	_	—	_	—	—	_	—	_	- PCLKDIV<2:0>			0000	
PTPER	0C04		PTPER<15:0> 00:										00F8					
SEVTCMP	0C06								SEVTCMP<	5:0>								0000
MDC	0C0A								MDC<15:)>								0000
CHOP	0C1A	CHPCLKEN	_	_	_	_	_					CHOPCI	_K<9:0>					0000
PWMKEY	0C1E		PWMKEY<15:0> 000								0000							
Legend: -	– = unir	mplemented, re	ead as '0'.	Reset valu	es are show	vn in hexade	ecimal.											-

TABLE 4-13: PWM GENERATOR 1 REGISTER MAP FOR dsPIC33EPXXXMC20X/50X AND PIC24EPXXXMC20X DEVICES ONLY

File Name	Addr.	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	All Resets
PWMCON1	0C20	FLTSTAT	CLSTAT	TRGSTAT	FLTIEN	CLIEN	TRGIEN	ITB	MDCS	DTC<	<1:0>	DTCP	—	MTBS	CAM	XPRES	IUE	0000
IOCON1	0C22	PENH	PENL	POLH	POLL	PMOD)<1:0>	OVRENH	OVRENL	OVRDA	T<1:0>	FLTDA	\T<1:0>	CLDA	T<1:0>	SWAP	OSYNC	C000
FCLCON1	0C24	_		(CLSRC<4:	0>		CLPOL	CLMOD		FL	TSRC<4:)>		FLTPOL	FLTMO	D<1:0>	0000
PDC1	0C26			PDC1<15:0>											FFF8			
PHASE1	0C28			PHASE1<15:0>										0000				
DTR1	0C2A	_	_		DTR1<13:0> 00										0000			
ALTDTR1	0C2C	_	_						A	LTDTR1<1	13:0>							0000
TRIG1	0C32								TRGCMP<1	5:0>								0000
TRGCON1	0C34		TRGDI	V<3:0>		_	_	—	_	_	_			TRG	STRT<5:0	>		0000
LEBCON1	0C3A	PHR	PHF	PLR	PLF	FLTLEBEN	CLLEBEN	_	_	_	_	BCH	BCL	BPHH	BPHL	BPLH	BPLL	0000
LEBDLY1	0C3C	_	_	_	—						LEB<11	:0>						0000
AUXCON1	0C3E	_	_	_	—		BLANKS	SEL<3:0>		_	_		CHOPS	EL<3:0>		CHOPHEN	CHOPLEN	0000

Legend: — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

4.4.2 EXTENDED X DATA SPACE

The lower portion of the base address space range, between 0x0000 and 0x7FFF, is always accessible regardless of the contents of the Data Space Page registers. It is indirectly addressable through the register indirect instructions. It can be regarded as being located in the default EDS Page 0 (i.e., EDS address range of 0x000000 to 0x007FFF with the base address bit, EA<15> = 0, for this address range). However, Page 0 cannot be accessed through the upper 32 Kbytes, 0x8000 to 0xFFFF, of base Data Space, in combination with DSRPAG = 0x000 or DSWPAG = 0x000. Consequently, DSRPAG and DSWPAG are initialized to 0x001 at Reset.

- Note 1: DSxPAG should not be used to access Page 0. An EDS access with DSxPAG set to 0x000 will generate an address error trap.
 - 2: Clearing the DSxPAG in software has no effect.

The remaining pages, including both EDS and PSV pages, are only accessible using the DSRPAG or DSWPAG registers in combination with the upper 32 Kbytes, 0x8000 to 0xFFFF, of the base address, where base address bit, EA<15> = 1.

For example, when DSRPAG = 0x001 or DSWPAG = 0x001, accesses to the upper 32 Kbytes, 0x8000 to 0xFFFF, of the Data Space will map to the EDS address range of 0x008000 to 0x00FFFF. When DSRPAG = 0x002 or DSWPAG = 0x002, accesses to the upper 32 Kbytes of the Data Space will map to the EDS address range of 0x010000 to 0x017FFF and so on, as shown in the EDS memory map in Figure 4-17.

For more information on the PSV page access using Data Space Page registers, refer to the "**Program Space Visibility from Data Space**" section in "**Program Memory**" (DS70613) of the "*dsPIC33/ PIC24 Family Reference Manual*".



FIGURE 4-17: EDS MEMORY MAP

11.4 Peripheral Pin Select (PPS)

A major challenge in general purpose devices is providing the largest possible set of peripheral features while minimizing the conflict of features on I/O pins. The challenge is even greater on low pin count devices. In an application where more than one peripheral needs to be assigned to a single pin, inconvenient workarounds in application code, or a complete redesign, may be the only option.

Peripheral Pin Select configuration provides an alternative to these choices by enabling peripheral set selection and their placement on a wide range of I/O pins. By increasing the pinout options available on a particular device, users can better tailor the device to their entire application, rather than trimming the application to fit the device.

The Peripheral Pin Select configuration feature operates over a fixed subset of digital I/O pins. Users may independently map the input and/or output of most digital peripherals to any one of these I/O pins. Hardware safeguards are included that prevent accidental or spurious changes to the peripheral mapping once it has been established.

11.4.1 AVAILABLE PINS

The number of available pins is dependent on the particular device and its pin count. Pins that support the Peripheral Pin Select feature include the label, "RPn" or "RPIn", in their full pin designation, where "n" is the remappable pin number. "RP" is used to designate pins that support both remappable input and output functions, while "RPI" indicates pins that support remappable input functions only.

11.4.2 AVAILABLE PERIPHERALS

The peripherals managed by the Peripheral Pin Select are all digital-only peripherals. These include general serial communications (UART and SPI), general purpose timer clock inputs, timer-related peripherals (input capture and output compare) and interrupt-on-change inputs. In comparison, some digital-only peripheral modules are never included in the Peripheral Pin Select feature. This is because the peripheral's function requires special I/O circuitry on a specific port and cannot be easily connected to multiple pins. These modules include I^2C^{TM} and the PWM. A similar requirement excludes all modules with analog inputs, such as the ADC Converter.

A key difference between remappable and nonremappable peripherals is that remappable peripherals are not associated with a default I/O pin. The peripheral must always be assigned to a specific I/O pin before it can be used. In contrast, non-remappable peripherals are always available on a default pin, assuming that the peripheral is active and not conflicting with another peripheral.

When a remappable peripheral is active on a given I/O pin, it takes priority over all other digital I/O and digital communication peripherals associated with the pin. Priority is given regardless of the type of peripheral that is mapped. Remappable peripherals never take priority over any analog functions associated with the pin.

11.4.3 CONTROLLING PERIPHERAL PIN SELECT

Peripheral Pin Select features are controlled through two sets of SFRs: one to map peripheral inputs and one to map outputs. Because they are separately controlled, a particular peripheral's input and output (if the peripheral has both) can be placed on any selectable function pin without constraint.

The association of a peripheral to a peripheralselectable pin is handled in two different ways, depending on whether an input or output is being mapped.

REGISTER 11-16: RPINR38: PERIPHERAL PIN SELECT INPUT REGISTER 38 (dsPIC33EPXXXMC20X AND PIC24EPXXXMC20X DEVICES ONLY)

U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
_				DTCMP1R<6:	0>		
bit 15							bit 8
U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
_	—	_		—	—	_	—
bit 7		·		÷			bit 0
Legend:							
R = Readable bit W = Writ			bit	U = Unimpler	nented bit, read	l as '0'	
-n = Value at	POR	'1' = Bit is set		'0' = Bit is cle	ared	x = Bit is unkr	nown
bit 15	Unimplemer	ted: Read as '	0'				
bit 14-8	DTCMP1R<6 (see Table 11	::0>: Assign PV -2 for input pin	VM Dead-Tim selection nun	e Compensation nbers)	on Input 1 to the	e Correspondine	g RPn Pin bits
	1111001 = 	nput tied to RPI	121				
	•						
	•						
	0000001 =	nput tied to CM	P1				
	0000000 = li	nput tied to Vss	}				
bit 7-0	Unimplemer	ted: Read as '	0'				

NOTES:

16.3 PWMx Control Registers

REGISTER 16-1: PTCON: PWMx TIME BASE CONTROL REGISTER

R/W-0	U-0	R/W-0	HS/HC-0	R/W-0	R/W-0	R/W-0	R/W-0
PTEN	—	PTSIDL	SESTAT	SEIEN	EIPU ⁽¹⁾	SYNCPOL ⁽¹⁾	SYNCOEN ⁽¹⁾
bit 15							bit 8

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
SYNCEN ⁽¹⁾	SYNCSRC2 ⁽¹⁾	SYNCSRC1 ⁽¹⁾	SYNCSRC0 ⁽¹⁾	SEVTPS3 ⁽¹⁾	SEVTPS2 ⁽¹⁾	SEVTPS1 ⁽¹⁾	SEVTPS0 ⁽¹⁾
bit 7							bit 0

Legend:	HC = Hardware Clearable bit	HS = Hardware Settable bit				
R = Readable bit	W = Writable bit	U = Unimplemented bit, re	ad as '0'			
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown			

bit 15	PTEN: PWMx Module Enable bit
	 1 = PWMx module is enabled 0 = PWMx module is disabled
bit 14	Unimplemented: Read as '0'
bit 13	PTSIDL: PWMx Time Base Stop in Idle Mode bit
	 1 = PWMx time base halts in CPU Idle mode 0 = PWMx time base runs in CPU Idle mode
bit 12	SESTAT: Special Event Interrupt Status bit
	 1 = Special event interrupt is pending 0 = Special event interrupt is not pending
bit 11	SEIEN: Special Event Interrupt Enable bit
	1 = Special event interrupt is enabled
	0 = Special event interrupt is disabled
bit 10	EIPU: Enable Immediate Period Updates bit ⁽¹⁾
	 1 = Active Period register is updated immediately 0 = Active Period register updates occur on PWMx cycle boundaries
bit 9	SYNCPOL: Synchronize Input and Output Polarity bit ⁽¹⁾
	1 = SYNCI1/SYNCO1 polarity is inverted (active-low)
	0 = SYNCI1/SYNCO1 is active-high
bit 8	SYNCOEN: Primary Time Base Sync Enable bit ⁽¹⁾
	1 = SYNCO1 output is enabled
L:1 7	0 = SYNCOT output is disabled
DIT /	SYNCEN: External Time Base Synchronization Enable bit
	1 = External synchronization of primary time base is enabled
Note 1:	These bits should be changed only when PTEN = 0. In addition, when using the SYNCI1 feature, the user
	application must program the period register with a value that is slightly larger than the expected period of

the external synchronization input signal.

2: See Section 24.0 "Peripheral Trigger Generator (PTG) Module" for information on this selection.

REGISTER 16-1: PTCON: PWMx TIME BASE CONTROL REGISTER (CONTINUED)

bit 6-4	SYNCSRC<2:0>: Synchronous Source Selection bits ⁽¹⁾ 111 = Reserved
	•
	• 100 = Reserved 011 = PTGO17 ⁽²⁾ 010 = PTGO16 ⁽²⁾ 001 = Reserved 000 = SYNCI1 input from PPS
bit 3-0	<pre>SEVTPS<3:0>: PWMx Special Event Trigger Output Postscaler Select bits⁽¹⁾ 1111 = 1:16 Postscaler generates Special Event Trigger on every sixteenth compare match event</pre>
	0001 = 1:2 Postscaler generates Special Event Trigger on every second compare match event 0000 = 1:1 Postscaler generates Special Event Trigger on every compare match event

- **Note 1:** These bits should be changed only when PTEN = 0. In addition, when using the SYNCI1 feature, the user application must program the period register with a value that is slightly larger than the expected period of the external synchronization input signal.
 - 2: See Section 24.0 "Peripheral Trigger Generator (PTG) Module" for information on this selection.

dsPIC33EPXXXGP50X, dsPIC33EPXXXMC20X/50X AND PIC24EPXXXGP/MC20X

U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0			
—	_			DTR)	<13:8>					
bit 15							bit 8			
R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0			
			DTR	2x<7:0>						
bit 7							bit 0			
Legend:										
R = Readable bit W = Writable bit				U = Unimplemented bit, read as '0'						
-n = Value at F	POR	'1' = Bit is set	'0' = Bit is cle	cleared x = Bit is unknown						

REGISTER 16-10: DTRx: PWMx DEAD-TIME REGISTER

bit 15-14 Unimplemented: Read as '0'

bit 13-0 DTRx<13:0>: Unsigned 14-Bit Dead-Time Value for PWMx Dead-Time Unit bits

REGISTER 16-11: ALTDTRx: PWMx ALTERNATE DEAD-TIME REGISTER

U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0			
—	—			ALTDT	Rx<13:8>					
bit 15							bit 8			
R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0			
			ALTDT	Rx<7:0>						
bit 7							bit 0			
Legend:										
R = Readable	bit	W = Writable	bit	U = Unimplemented bit, read as '0'						
-n = Value at P	POR	'1' = Bit is set		'0' = Bit is cle	ared	x = Bit is unknown				

bit 15-14 Unimplemented: Read as '0'

bit 13-0 ALTDTRx<13:0>: Unsigned 14-Bit Dead-Time Value for PWMx Dead-Time Unit bits

dsPIC33EPXXXGP50X, dsPIC33EPXXXMC20X/50X AND PIC24EPXXXGP/MC20X

R/W-0	R/W-0	R/W-0	U-0	R/W-0, HC	R/W-0	R-0	R-1
UTXISEL1	UTXINV	UTXISEL0	—	UTXBRK	UTXEN ⁽¹⁾	UTXBF	TRMT
bit 15							bit 8
R/W-0	R/W-0	R/W-0	R-1	R-0	R-0	R/C-0	R-0
URXISEL1	URXISEL0	ADDEN	RIDLE	PERR	FERR	OERR	URXDA
bit 7					bit 0		
Legend:		HC = Hardwar	e Clearable bit	C = Clearable	e bit		
R = Readable bit W = Writable bit U = Unimplemented bit, read as '0'							

REGISTER 20-2: UxSTA: UARTx STATUS AND CONTROL REGISTER

R = Readable bit	W = Writable bit	U = Unimplemented bit, read	d as '0'
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15,13 UTXISEL<1:0>: UARTx Transmission Interrupt Mode Selection bits

- 11 = Reserved; do not use
- 10 = Interrupt when a character is transferred to the Transmit Shift Register (TSR) and as a result, the transmit buffer becomes empty
- 01 = Interrupt when the last character is shifted out of the Transmit Shift Register; all transmit operations are completed
- 00 = Interrupt when a character is transferred to the Transmit Shift Register (this implies there is at least one character open in the transmit buffer)
- bit 14 UTXINV: UARTx Transmit Polarity Inversion bit
 - $\frac{\text{If IREN = 0:}}{1 = \text{UxTX Idle state is '0'}}$
 - 0 = UxTX Idle state is '1'
 - If IREN = 1:
 - 1 = IrDA encoded, UxTX Idle state is '1'
 - 0 = IrDA encoded, UxTX Idle state is '0'
- bit 12 Unimplemented: Read as '0'
- bit 11 UTXBRK: UARTx Transmit Break bit
 - 1 = Sends Sync Break on next transmission Start bit, followed by twelve '0' bits, followed by Stop bit; cleared by hardware upon completion
 - 0 = Sync Break transmission is disabled or completed
- bit 10 UTXEN: UARTx Transmit Enable bit⁽¹⁾ 1 = Transmit is enabled, UxTX pin is controlled by UARTx
 - 0 = Transmit is disabled, any pending transmission is aborted and buffer is reset; UxTX pin is controlled by the PORT
- bit 9 UTXBF: UARTx Transmit Buffer Full Status bit (read-only)
 - 1 = Transmit buffer is full
 - 0 = Transmit buffer is not full, at least one more character can be written
- bit 8 TRMT: Transmit Shift Register Empty bit (read-only)
 - 1 = Transmit Shift Register is empty and transmit buffer is empty (the last transmission has completed)
 - 0 = Transmit Shift Register is not empty, a transmission is in progress or queued
- bit 7-6 URXISEL<1:0>: UARTx Receive Interrupt Mode Selection bits
 - 11 = Interrupt is set on UxRSR transfer, making the receive buffer full (i.e., has 4 data characters)
 - 10 = Interrupt is set on UxRSR transfer, making the receive buffer 3/4 full (i.e., has 3 data characters)
 - 0x = Interrupt is set when any character is received and transferred from the UxRSR to the receive buffer; receive buffer has one or more characters
- **Note 1:** Refer to the "**UART**" (DS70582) section in the "*dsPIC33/PIC24 Family Reference Manual*" for information on enabling the UARTx module for transmit operation.

24.3 PTG Control Registers

REGISTER 24-1: PTGCST: PTG CONTROL/STATUS REGISTER

R/W-0	U-0	R/W-0	R/W-0	U-0	R/W-0	R/W-0	R/W-0
PTGEN	—	PTGSIDL	PTGTOGL	—	PTGSWT ⁽²⁾	PTGSSEN ⁽³⁾	PTGIVIS
bit 15							bit 8
R/W-0	HS-0	U-0	U-0	U-0	U-0	R/V	V-0
PTGSTRT	PTGWDTO	_	_	_	_	PTGITM1 ⁽¹⁾	PTGITM0 ⁽¹⁾

h	it	7
υ	π.	1

Legend:	HS = Hardware Settable bit			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'		
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown	

bit 15		PTGEN: Module Enable bit
		1 = PTG module is enabled
		0 = PTG module is disabled
bit 14		Unimplemented: Read as '0'
bit 13		PTGSIDL: PTG Stop in Idle Mode bit
		 1 = Discontinues module operation when device enters Idle mode 0 = Continues module operation in Idle mode
bit 12		PTGTOGL: PTG TRIG Output Toggle Mode bit
		 1 = Toggle state of the PTGOx for each execution of the PTGTRIG command 0 = Each execution of the PTGTRIG command will generate a single PTGOx pulse determined by the value in the PTGPWDx bits
bit 11		Unimplemented: Read as '0'
bit 10		PTGSWT: PTG Software Trigger bit ⁽²⁾
		1 = Triggers the PTG module
		0 = No action (clearing this bit will have no effect)
bit 9		PTGSSEN: PTG Enable Single-Step bit ⁽³⁾
		1 = Enables Single-Step mode
		0 = Disables Single-Step mode
bit 8		PTGIVIS: PTG Counter/Timer Visibility Control bit
		1 = Reads of the PTGSDLIM, PTGCxLIM or PTGTxLIM registers return the current values of their corresponding counter/timer registers (PTGSD, PTGCx, PTGTx)
		 Reads of the PTGSDLIM, PTGCxLIM or PTGTxLIM registers return the value previously written to those limit registers
bit 7		PTGSTRT: PTG Start Sequencer bit
		1 = Starts to sequentially execute commands (Continuous mode)0 = Stops executing commands
bit 6		PTGWDTO: PTG Watchdog Timer Time-out Status bit
		1 = PTG Watchdog Timer has timed out
		0 = PTG watchdog Timer has not timed out.
bit 5-2		Unimplemented: Read as '0'
Note	1: Th	nese bits apply to the PTGWHI and PTGWLO commands only.
	2: Th	is bit is only used with the PTGCTRL step command software trigger option.

3: Use of the PTG Single-Step mode is reserved for debugging tools only.

bit 0

REGISTER 24-8: PTGC1LIM: PTG COUNTER 1 LIMIT REGISTER⁽¹⁾

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
			PTGC1L	IM<15:8>			
bit 15							bit 8
R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
PTGC1LIM<7:0>							
bit 7							bit 0
Logond							

Legenu.				
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'		
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown	

bit 15-0 **PTGC1LIM<15:0>:** PTG Counter 1 Limit Register bits May be used to specify the loop count for the PTGJMPC1 Step command or as a limit register for the General Purpose Counter 1.

REGISTER 24-9: PTGHOLD: PTG HOLD REGISTER⁽¹⁾

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
PTGHOLD<15:8>							
bit 15							bit 8

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	
PTGHOLD<7:0>								
bit 7 bit 0								

Legend:				
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'		
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown	

bit 15-0 **PTGHOLD<15:0>:** PTG General Purpose Hold Register bits Holds user-supplied data to be copied to the PTGTxLIM, PTGCxLIM, PTGSDLIM or PTGL0 registers with the PTGCOPY command.

Note 1: This register is read-only when the PTG module is executing Step commands (PTGEN = 1 and PTGSTRT = 1).

Note 1: This register is read-only when the PTG module is executing Step commands (PTGEN = 1 and PTGSTRT = 1).

27.2 User ID Words

dsPIC33EPXXXGP50X, dsPIC33EPXXXMC20X/50X and PIC24EPXXXGP/MC20X devices contain four User ID Words, located at addresses, 0x800FF8 through 0x800FFE. The User ID Words can be used for storing product information such as serial numbers, system manufacturing dates, manufacturing lot numbers and other application-specific information.

The User ID Words register map is shown in Table 27-3.

TABLE 27-3:USER ID WORDS REGISTER
MAP

File Name	Address	Bits 23-16	Bits 15-0
FUID0	0x800FF8	—	UID0
FUID1	0x800FFA	—	UID1
FUID2	0x800FFC	—	UID2
FUID3	0x800FFE	—	UID3

Legend: — = unimplemented, read as '1'.

27.3 On-Chip Voltage Regulator

All of the dsPIC33EPXXXGP50X, dsPIC33EPXXXMC20X/50X and PIC24EPXXXGP/ MC20X devices power their core digital logic at a nominal 1.8V. This can create a conflict for designs that are required to operate at a higher typical voltage, such as 3.3V. To simplify system design, all devices in the dsPIC33EPXXXGP50X, dsPIC33EPXXXMC20X/50X and PIC24EPXXXGP/MC20X family incorporate an onchip regulator that allows the device to run its core logic from VDD.

The regulator provides power to the core from the other VDD pins. A low-ESR (less than 1 Ohm) capacitor (such as tantalum or ceramic) must be connected to the VCAP pin (Figure 27-1). This helps to maintain the stability of the regulator. The recommended value for the filter capacitor is provided in Table 30-5 located in **Section 30.0 "Electrical Characteristics"**.

Note: It is important for the low-ESR capacitor to be placed as close as possible to the VCAP pin.

FIGURE 27-1: CONNECTIONS FOR THE ON-CHIP VOLTAGE

REGULATOR^(1,2,3)



27.4 Brown-out Reset (BOR)

The Brown-out Reset (BOR) module is based on an internal voltage reference circuit that monitors the regulated supply voltage, VCAP. The main purpose of the BOR module is to generate a device Reset when a brown-out condition occurs. Brown-out conditions are generally caused by glitches on the AC mains (for example, missing portions of the AC cycle waveform due to bad power transmission lines or voltage sags due to excessive current draw when a large inductive load is turned on).

A BOR generates a Reset pulse, which resets the device. The BOR selects the clock source, based on the device Configuration bit values (FNOSC<2:0> and POSCMD<1:0>).

If an oscillator mode is selected, the BOR activates the Oscillator Start-up Timer (OST). The system clock is held until OST expires. If the PLL is used, the clock is held until the LOCK bit (OSCCON<5>) is '1'.

Concurrently, the PWRT Time-out (TPWRT) is applied before the internal Reset is released. If TPWRT = 0 and a crystal oscillator is being used, then a nominal delay of TFSCM is applied. The total delay in this case is TFSCM. Refer to Parameter SY35 in Table 30-22 of **Section 30.0 "Electrical Characteristics"** for specific TFSCM values.

The BOR status bit (RCON<1>) is set to indicate that a BOR has occurred. The BOR circuit continues to operate while in Sleep or Idle modes and resets the device should VDD fall below the BOR threshold voltage.



FIGURE 30-21: SPI2 SLAVE MODE (FULL-DUPLEX, CKE = 0, CKP = 0, SMP = 0) TIMING CHARACTERISTICS

TABLE 30-54: OP AMP/COMPARATOR VOLTAGE REFERENCE SETTLING TIME SPECIFICATIONS

AC CHARACTERISTICS			Standard Operating Conditions (see Note 2): 3.0V to 3.6V (unless otherwise stated) Operating temperature $-40^{\circ}C \le TA \le +85^{\circ}C$ for Industrial $-40^{\circ}C \le TA \le +125^{\circ}C$ for Extended				
Param.	Symbol	Characteristic	Min.	Тур.	Max. Units C		Conditions
VR310	TSET	Settling Time	_	1	10	μS	(Note 1)

Note 1: Settling time is measured while CVRR = 1 and CVR<3:0> bits transition from '0000' to '1111'.

2: Device is functional at VBORMIN < VDD < VDDMIN, but will have degraded performance. Device functionality is tested, but not characterized. Analog modules (ADC, op amp/comparator and comparator voltage reference) may have degraded performance. Refer to Parameter BO10 in Table 30-13 for the minimum and maximum BOR values.

TABLE 30-55: OP AMP/COMPARATOR VOLTAGE REFERENCE SPECIFICATIONS

DC CHARACTERISTICS			$\begin{array}{l} \mbox{Standard Operating Conditions (see Note 1): 3.0V to 3.6V} \\ \mbox{(unless otherwise stated)} \\ \mbox{Operating temperature} & -40^{\circ}C \leq TA \leq +85^{\circ}C \mbox{ for Industrial} \\ & -40^{\circ}C \leq TA \leq +125^{\circ}C \mbox{ for Extended} \end{array}$				
Param No.	Symbol	Characteristics	Min. Typ. Max. Units Condit				Conditions
VRD310	CVRES	Resolution	CVRSRC/24	_	CVRSRC/32	LSb	
VRD311	CVRAA	Absolute Accuracy ⁽²⁾	—	±25	—	mV	CVRSRC = 3.3V
VRD313	CVRSRC	Input Reference Voltage	0	_	AVDD + 0.3	V	
VRD314	CVROUT	Buffer Output Resistance ⁽²⁾	_	1.5k	_	Ω	

Note 1: Device is functional at VBORMIN < VDD < VDDMIN, but will have degraded performance. Device functionality is tested, but not characterized. Analog modules (ADC, op amp/comparator and comparator voltage reference) may have degraded performance. Refer to Parameter BO10 in Table 30-13 for the minimum and maximum BOR values.

2: Parameter is characterized but not tested in manufacturing.

dsPIC33EPXXXGP50X, dsPIC33EPXXXMC20X/50X AND PIC24EPXXXGP/MC20X

DC CHARACT	ERISTICS		Standard Operating Conditions: 3.0V to 3.6V (unless otherwise stated)Operating temperature $-40^{\circ}C \le TA \le +150^{\circ}C$				
Parameter Typical Max			Units	Conditions			
Power-Down	Current (IPD)						
HDC60e	1400	2500	μΑ	+150°C	3.3V	Base Power-Down Current (Notes 1, 3)	
HDC61c	15	—	μA	+150°C	3.3V	Watchdog Timer Current: ∆IWDT (Notes 2, 4)	

TABLE 31-4: DC CHARACTERISTICS: POWER-DOWN CURRENT (IPD)

Note 1: Base IPD is measured with all peripherals and clocks shut down. All I/Os are configured as inputs and pulled to Vss. WDT, etc., are all switched off and VREGS (RCON<8>) = 1.

2: The ∆ current is the additional current consumed when the module is enabled. This current should be added to the base IPD current.

3: These currents are measured on the device containing the most memory in this family.

4: These parameters are characterized, but are not tested in manufacturing.

TABLE 31-5: DC CHARACTERISTICS: IDLE CURRENT (IIDLE)

DC CHARAG	CTERISTICS		Standard Operating Conditions: 3.0V to 3.6V (unless otherwise stated) Operating temperature $-40^{\circ}C \le TA \le +150^{\circ}C$				
Parameter No.	Typical	Max	Units	Conditions			
HDC44e	12	30	mA	+150°C	3.3V	40 MIPS	

TABLE 31-6: DC CHARACTERISTICS: OPERATING CURRENT (IDD)

DC CHARA	CTERISTICS		Standard Op (unless other Operating ten	erating Condi rwise stated) nperature -40	tions: 3.0V to 0° C \leq TA \leq +15	9 3.6V 0°C
Parameter No.	Typical	Мах	Units		Condi	tions
HDC20	9	15	mA	+150°C	3.3V	10 MIPS
HDC22	16	25	mA	+150°C	3.3V	20 MIPS
HDC23	30	50	mA	+150°C	3.3V	40 MIPS

TABLE 31-7: DC CHARACTERISTICS: DOZE CURRENT (IDOZE)

DC CHARA	CTERISTICS	Standard Operating Conditions: 3.0V to 3.6V (unless otherwise stated) Operating temperature $-40^{\circ}C \le TA \le +150^{\circ}C$					
Parameter No.	Typical	Мах	Doze Ratio	Units		Condi	tions
HDC72a	24	35	1:2	mA			
HDC72f ⁽¹⁾	14	—	1:64	mA	+150°C	3.3V	40 MIPS
HDC72g ⁽¹⁾	12	_	1:128	mA			

Note 1: Parameters with Doze ratios of 1:64 and 1:128 are characterized, but are not tested in manufacturing.

64-Lead Plastic Thin Quad Flatpack (PT) 10x10x1 mm Body, 2.00 mm Footprint [TQFP]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



RECOMMENDED LAND PATTERN

	MILLIMETERS				
Dimensior	MIN	NOM	MAX		
Contact Pitch	E		0.50 BSC		
Contact Pad Spacing	C1		11.40		
Contact Pad Spacing	C2		11.40		
Contact Pad Width (X64)	X1			0.30	
Contact Pad Length (X64)	Y1			1.50	
Distance Between Pads	G	0.20			

Notes:

1. Dimensioning and tolerancing per ASME Y14.5M

BSC: Basic Dimension. Theoretically exact value shown without tolerances.

Microchip Technology Drawing No. C04-2085B

Section Name	Update Description
Section 30.0 "Electrical Characteristics"	 Throughout: qualifies all footnotes relating to the operation of analog modules below VDDMIN (replaces "will have" with "may have")
	 Throughout: changes all references of SPI timing parameter symbol "TscP" to "FscP" Table 30-1: changes VDD range to 3.0V to 3.6V
	Table 30-4: removes Parameter DC12 (RAM Retention Voltage)
	 Table 30-7: updates Maximum values at 10 and 20 MIPS
	 Table 30-8: adds Maximum IPD values, and removes all ∆IWDT entries
	 Adds new Table 30-9 (Watchdog Timer Delta Current) with consolidated values removed from Table 30-8. All subsequent tables are renumbered accordingly.
	Table 30-10: adds footnote for all parameters for 1:2 Doze ratio Table 30-11:
	- changes Minimum and Maximum values for D120 and D130
	 adds Minimum and Maximum values for D131
	 adds Minimum and Maximum values for D150 through D156, and removes Typical values
	• Table 30-12:
	- reformats table for readability
	- changes IOL conditions for DO10
	Iable 30-14: adds footnote to D135 Table 30-17: abangaa Minimum and Maximum values for OS20
	Table 30-17: changes minimum and maximum values for OS30 Table 30-19:
	- splits temperature range and adds new values for E20a
	 reduces temperature range for F20b to extended temperatures only
	• Table 30-20:
	 splits temperature range and adds new values for F21a
	- reduces temperature range for F20b to extended temperatures only
	Table 30-53:
	- adds footpote ("Parameter characterized") to multiple parameters
	 Table 30-55: adds Minimum and Maximum values for all CTMUI specifications, and removes Typical values
	 Table 30-57: adds new footnote to AD09 Table 30-58:
	 removes all specifications for accuracy with external voltage references removes Typical values for AD23a and AD24a
	 replaces Minimum and Maximum values for AD21a, AD22a, AD23a and AD24a with new values, split by Industrial and Extended temperatures
	- removes Maximum value of AD30
	- removes Minimum values from AD31a and AD32a
	- adds of changes Typical values for AD30, AD31a, AD32a and AD33a
	- removes all specifications for accuracy with external voltage references
	 removes Maximum value of AD30
	 removes Typical values for AD23b and AD24b
	- replaces Minimum and Maximum values for AD21b, AD22b, AD23b and AD24b
	with new values, split by Industrial and Extended temperatures
	 removes withintum and waximum values from AD310, AD320, AD330 and AD340 adds or changes Typical values for AD30, AD31a, AD32a and AD33a
	Table 30-61: Adds footnote to AD51
Section 32.0 "DC and AC	Updates Figure 32-6 (Typical IDD @ 3.3V) with individual current vs. processor speed
Device Characteristics	curves for the different program memory sizes
Graphs"	
Section 33.0 "Packaging	Replaces drawing C04-149C (64-pin QFN, 7.15 x 7.15 exposed pad) with C04-154A
Information"	(64-pin QFN, 5.4 x 5.4 exposed pad)

TABLE A-5: MAJOR SECTION UPDATES (CONTINUED)