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"**Embedded - Microcontrollers**" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "**Embedded - Microcontrollers**"

Details	
Product Status	Obsolete
Core Processor	PIC
Core Size	16-Bit
Speed	60 MIPs
Connectivity	I²C, IrDA, LINbus, QEI, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, DMA, Motor Control PWM, POR, PWM, WDT
Number of I/O	35
Program Memory Size	128KB (43K x 24)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	8K x 16
Voltage - Supply (Vcc/Vdd)	3V ~ 3.6V
Data Converters	A/D 9x10b/12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 125°C (TA)
Mounting Type	Surface Mount
Package / Case	44-VQFN Exposed Pad
Supplier Device Package	44-QFN (8x8)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/pic24ep128mc204t-e-ml

REGISTER 3-2:   CORCON: CORE CONTROL REGISTER (CONTINUED)

bit 2   **SFA:** Stack Frame Active Status bit

        1 = Stack frame is active; W14 and W15 address 0x0000 to 0xFFFF, regardless of DSRPAG and DSWPAG values

        0 = Stack frame is not active; W14 and W15 address of EDS or Base Data Space

bit 1   **RND:** Rounding Mode Select bit[1]

        1 = Biased (conventional) rounding is enabled

        0 = Unbiased (convergent) rounding is enabled

bit 0   **IF:** Integer or Fractional Multiplier Mode Select bit[1]

        1 = Integer mode is enabled for DSP multiply

        0 = Fractional mode is enabled for DSP multiply

Note 1:   This bit is available on dsPIC33EPXXXMC20X/50X and dsPIC33EPXXXGP50X devices only.

     2:   This bit is always read as '0'.

     3:   The IPL3 bit is concatenated with the IPL<2:0> bits (SR<7:5>) to form the CPU Interrupt Priority Level.

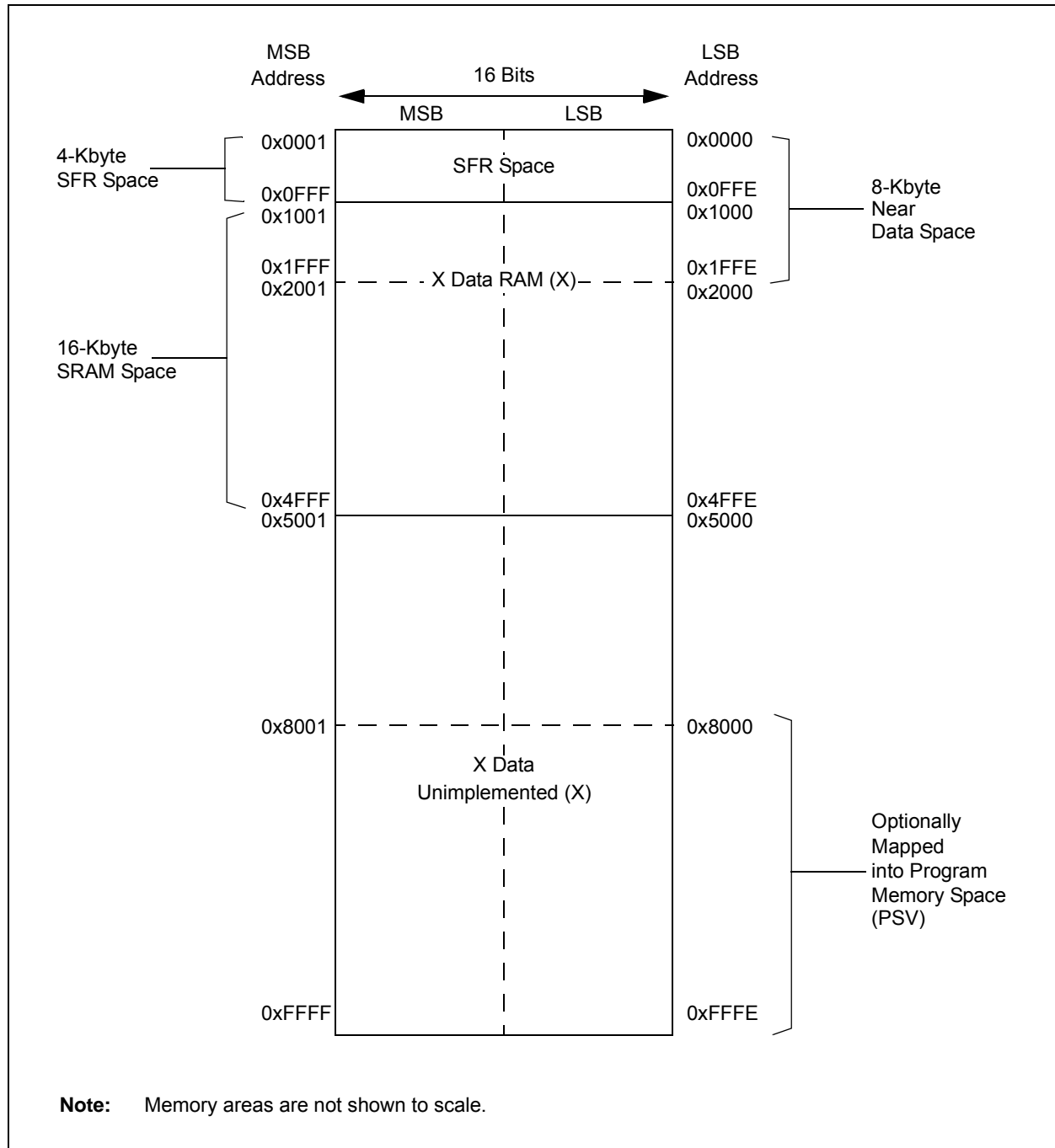**FIGURE 4-14:   DATA MEMORY MAP FOR PIC24EP128GP/MC20X/50X DEVICES**

TABLE 4-31: **PERIPHERAL PIN SELECT INPUT REGISTER MAP FOR dsPIC33EPXXXGP50X DEVICES ONLY**

File Name	Addr.	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	All Resets
RPINR0	06A0	—	INT1R<6:0>								—	—	—	—	—	—	—	—	0000
RPINR1	06A2	—	—	—	—	—	—	—	—	—	INT2R<6:0>							0000
RPINR3	06A6	—	—	—	—	—	—	—	—	—	T2CKR<6:0>							0000
RPINR7	06AE	—	IC2R<6:0>							—	IC1R<6:0>							0000
RPINR8	06B0	—	IC4R<6:0>							—	IC3R<6:0>							0000
RPINR11	06B6	—	—	—	—	—	—	—	—	—	OCFAR<6:0>							0000
RPINR18	06C4	—	—	—	—	—	—	—	—	—	U1RXR<6:0>							0000
RPINR19	06C6	—	—	—	—	—	—	—	—	—	U2RXR<6:0>							0000
RPINR22	06CC	—	SCK2INR<6:0>							—	SDI2R<6:0>							0000
RPINR23	06CE	—	—	—	—	—	—	—	—	—	SS2R<6:0>							0000
RPINR26	06D4	—	—	—	—	—	—	—	—	—	C1RXR<6:0>							0000

Legend: — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

TABLE 4-32: **PERIPHERAL PIN SELECT INPUT REGISTER MAP FOR dsPIC33EPXXXMC50X DEVICES ONLY**

File Name	Addr.	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	All Resets
RPINR0	06A0	—	INT1R<6:0>								—	—	—	—	—	—	—	—	0000
RPINR1	06A2	—	—	—	—	—	—	—	—	—	INT2R<6:0>							0000
RPINR3	06A6	—	—	—	—	—	—	—	—	—	T2CKR<6:0>							0000
RPINR7	06AE	—	IC2R<6:0>							—	IC1R<6:0>							0000
RPINR8	06B0	—	IC4R<6:0>							—	IC3R<6:0>							0000
RPINR11	06B6	—	—	—	—	—	—	—	—	—	OCFAR<6:0>							0000
RPINR12	06B8	—	FLT2R<6:0>							—	FLT1R<6:0>							0000
RPINR14	06BC	—	QEB1R<6:0>							—	QEA1R<6:0>							0000
RPINR15	06BE	—	HOME1R<6:0>							—	INDX1R<6:0>							0000
RPINR18	06C4	—	—	—	—	—	—	—	—	—	U1RXR<6:0>							0000
RPINR19	06C6	—	—	—	—	—	—	—	—	—	U2RXR<6:0>							0000
RPINR22	06CC	—	SCK2INR<6:0>							—	SDI2R<6:0>							0000
RPINR23	06CE	—	—	—	—	—	—	—	—	—	SS2R<6:0>							0000
RPINR26	06D4	—	—	—	—	—	—	—	—	—	C1RXR<6:0>							0000
RPINR37	06EA	—	SYNCI1R<6:0>							—	—	—	—	—	—	—	—	0000
RPINR38	06EC	—	DTCMP1R<6:0>							—	—	—	—	—	—	—	—	0000
RPINR39	06EE	—	DTCMP3R<6:0>							—	DTCMP2R<6:0>							0000

Legend: — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

5.0 FLASH PROGRAM MEMORY

> **Note 1:** This data sheet summarizes the features of the dsPIC33EPXXXGP50X, dsPIC33EPXXXMC20X/50X and PIC24EPXXXGP/MC20X families of devices. It is not intended to be a comprehensive reference source. To complement the information in this data sheet, refer to **"Flash Programming"** (DS70609) in the *"dsPIC33/PIC24 Family Reference Manual"*, which is available from the Microchip web site (www.microchip.com).
>
> **2:** Some registers and associated bits described in this section may not be available on all devices. Refer to **Section 4.0 "Memory Organization"** in this data sheet for device-specific register and bit information.

The dsPIC33EPXXXGP50X, dsPIC33EPXXXMC20X/50X and PIC24EPXXXGP/MC20X devices contain internal Flash program memory for storing and executing application code. The memory is readable, writable and erasable during normal operation over the entire VDD range.

Flash memory can be programmed in two ways:

• In-Circuit Serial Programming™ (ICSP™) programming capability
• Run-Time Self-Programming (RTSP)

ICSP allows for a dsPIC33EPXXXGP50X, dsPIC33EPXXXMC20X/50X and PIC24EPXXXGP/MC20X device to be serially programmed while in the end application circuit. This is done with two lines for programming clock and programming data (one of the alternate programming pin pairs: PGECx/PGEDx), and three other lines for power (VDD), ground (VSS) and Master Clear (MCLR). This allows customers to manufacture boards with unprogrammed devices and then program the device just before shipping the product. This also allows the most recent firmware or a custom firmware to be programmed.

RTSP is accomplished using TBLRD (Table Read) and TBLWT (Table Write) instructions. With RTSP, the user application can write program memory data a single program memory word, and erase program memory in blocks or 'pages' of 1024 instructions (3072 bytes) at a time.

5.1 Table Instructions and Flash Programming

Regardless of the method used, all programming of Flash memory is done with the Table Read and Table Write instructions. These allow direct read and write access to the program memory space from the data memory while the device is in normal operating mode. The 24-bit target address in the program memory is formed using bits<7:0> of the TBLPAG register and the Effective Address (EA) from a W register, specified in the table instruction, as shown in Figure 5-1.

The TBLRDL and the TBLWTL instructions are used to read or write to bits<15:0> of program memory. TBLRDL and TBLWTL can access program memory in both Word and Byte modes.

The TBLRDH and TBLWTH instructions are used to read or write to bits<23:16> of program memory. TBLRDH and TBLWTH can also access program memory in Word or Byte mode.

FIGURE 5-1: **ADDRESSING FOR TABLE REGISTERS**
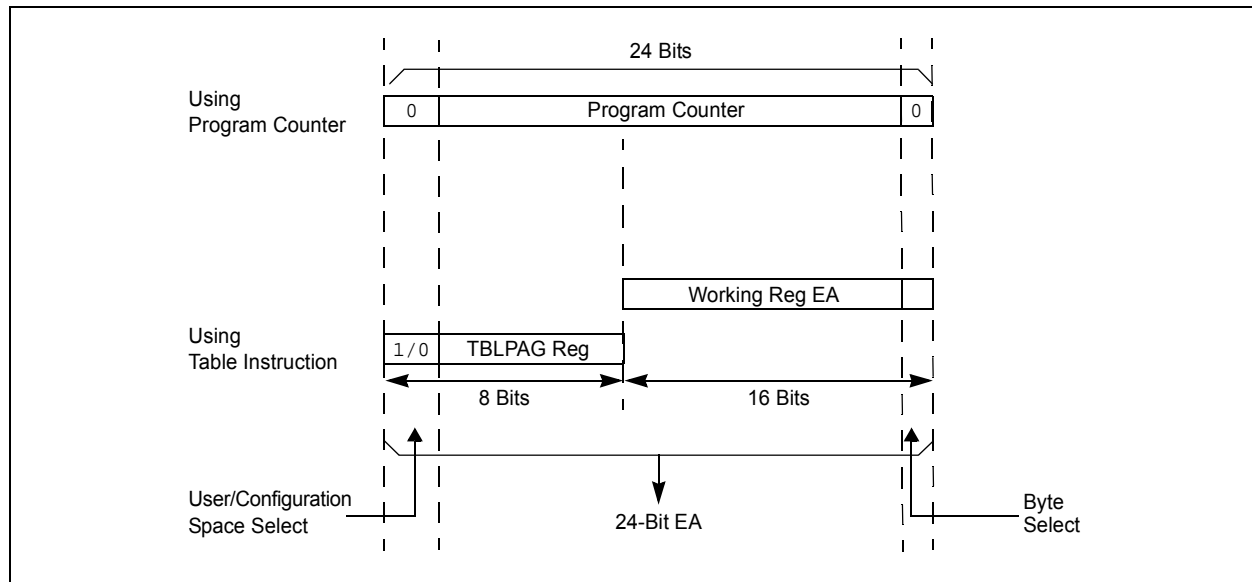
14.0 INPUT CAPTURE

> **Note 1:** This data sheet summarizes the features of the dsPIC33EPXXXGP50X, dsPIC33EPXXXMC20X/50X and PIC24EPXXXGP/MC20X families of devices. It is not intended to be a comprehensive reference source. To complement the information in this data sheet, refer to **"Input Capture"** (DS70352) in the "*dsPIC33/dsPIC24 Family Reference Manual*", which is available from the Microchip web site (www.microchip.com).
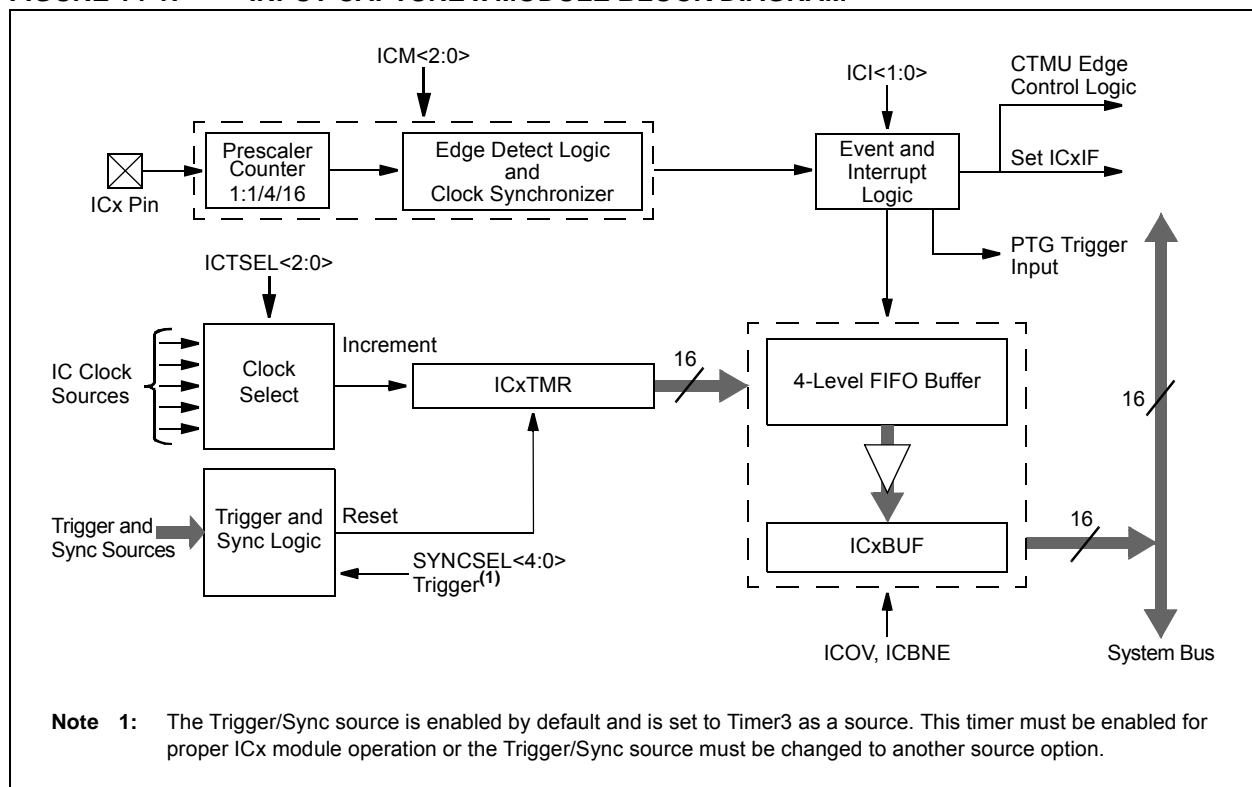>
> **2:** Some registers and associated bits described in this section may not be available on all devices. Refer to **Section 4.0 "Memory Organization"** in this data sheet for device-specific register and bit information.

The input capture module is useful in applications requiring frequency (period) and pulse measurement. The dsPIC33EPXXXGP50X, dsPIC33EPXXXMC20X/50X and PIC24EPXXXGP/MC20X devices support four input capture channels.

Key features of the input capture module include:

- Hardware-configurable for 32-bit operation in all modes by cascading two adjacent modules
- Synchronous and Trigger modes of output compare operation, with up to 19 user-selectable Trigger/Sync sources available
- A 4-level FIFO buffer for capturing and holding timer values for several events
- Configurable interrupt generation
- Up to six clock sources available for each module, driving a separate internal 16-bit counter

FIGURE 14-1: INPUT CAPTURE x MODULE BLOCK DIAGRAM

Note 1: The Trigger/Sync source is enabled by default and is set to Timer3 as a source. This timer must be enabled for proper ICx module operation or the Trigger/Sync source must be changed to another source option.

19.0 INTER-INTEGRATED CIRCUIT™ (I²C™)

> **Note 1:** This data sheet summarizes the features of the dsPIC33EPXXXGP50X, dsPIC33EPXXXMC20X/50X and PIC24EPXXXGP/MC20X families of devices. It is not intended to be a comprehensive reference source. To complement the information in this data sheet, refer to **"Inter-Integrated Circuit™ (I²C™)"** (DS70330) in the "*dsPIC33/PIC24 Family Reference Manual*", which is available from the Microchip web site (www.microchip.com).
>
> **2:** Some registers and associated bits described in this section may not be available on all devices. Refer to **Section 4.0 "Memory Organization"** in this data sheet for device-specific register and bit information.
>
> **3:** There are minimum bit rates of approximately $F_{CY}/512$. As a result, high processor speeds may not support 100 Kbit/second operation. See timing specifications, IM10 and IM11, and the **"Baud Rate Generator"** in the "*dsPIC33/PIC24 Family Reference Manual*".

The dsPIC33EPXXXGP50X, dsPIC33EPXXXMC20X/50X and PIC24EPXXXGP/MC20X family of devices contains two Inter-Integrated Circuit (I²C) modules: I2C1 and I2C2.

The I²C module provides complete hardware support for both Slave and Multi-Master modes of the I²C serial communication standard, with a 16-bit interface.

The I²C module has a 2-pin interface:

- The SCLx pin is clock
- The SDAx pin is data

The I²C module offers the following key features:

- I²C interface supporting both Master and Slave modes of operation
- I²C Slave mode supports 7 and 10-bit addressing
- I²C Master mode supports 7 and 10-bit addressing
- I²C port allows bidirectional transfers between master and slaves
- Serial clock synchronization for I²C port can be used as a handshake mechanism to suspend and resume serial transfer (SCLREL control)
- I²C supports multi-master operation, detects bus collision and arbitrates accordingly
- Intelligent Platform Management Interface (IPMI) support
- System Management Bus (SMBus) support

TABLE 24-1:   PTG STEP COMMAND FORMAT (CONTINUED)

bit 3-0 Step Command	OPTION<3:0>	Option Description
PTGCTRL[1]	0000	Reserved.
	0001	Reserved.
	0010	Disable Step Delay Timer (PTGSD).
	0011	Reserved.
	0100	Reserved.
	0101	Reserved.
	0110	Enable Step Delay Timer (PTGSD).
	0111	Reserved.
	1000	Start and wait for the PTG Timer0 to match the Timer0 Limit Register.
	1001	Start and wait for the PTG Timer1 to match the Timer1 Limit Register.
	1010	Reserved.
	1011	Wait for the software trigger bit transition from low-to-high before continuing (PTGSWT = 0 to 1).
	1100	Copy contents of the Counter 0 register to the AD1CHS0 register.
	1101	Copy contents of the Counter 1 register to the AD1CHS0 register.
	1110	Copy contents of the Literal 0 register to the AD1CHS0 register.
	1111	Generate triggers indicated in the Broadcast Trigger Enable register (PTGBTE).
PTGADD[1]	0000	Add contents of the PTGADJ register to the Counter 0 Limit register (PTGC0LIM).
	0001	Add contents of the PTGADJ register to the Counter 1 Limit register (PTGC1LIM).
	0010	Add contents of the PTGADJ register to the Timer0 Limit register (PTGT0LIM).
	0011	Add contents of the PTGADJ register to the Timer1 Limit register (PTGT1LIM).
	0100	Add contents of the PTGADJ register to the Step Delay Limit register (PTGSDLIM).
	0101	Add contents of the PTGADJ register to the Literal 0 register (PTGL0).
	0110	Reserved.
	0111	Reserved.
PTGCOPY[1]	1000	Copy contents of the PTGHOLD register to the Counter 0 Limit register (PTGC0LIM).
	1001	Copy contents of the PTGHOLD register to the Counter 1 Limit register (PTGC1LIM).
	1010	Copy contents of the PTGHOLD register to the Timer0 Limit register (PTGT0LIM).
	1011	Copy contents of the PTGHOLD register to the Timer1 Limit register (PTGT1LIM).
	1100	Copy contents of the PTGHOLD register to the Step Delay Limit register (PTGSDLIM).
	1101	Copy contents of the PTGHOLD register to the Literal 0 register (PTGL0).
	1110	Reserved.
	1111	Reserved.

Note 1: All reserved commands or options will execute but have no effect (i.e., execute as a NOP instruction).

2: Refer to Table 24-2 for the trigger output descriptions.

3: This feature is only available on dsPIC33EPXXXMC20X/50X and PIC24EPXXXMC20X devices.

NOTES:

REGISTER 25-4: **CMxMSKSRC: COMPARATOR x MASK SOURCE SELECT CONTROL REGISTER (CONTINUED)**

bit 3-0 **SELSRCA<3:0>:** Mask A Input Select bits

1111 = FLT4
1110 = FLT2
1101 = PTGO19
1100 = PTGO18
1011 = Reserved
1010 = Reserved
1001 = Reserved
1000 = Reserved
0111 = Reserved
0110 = Reserved
0101 = PWM3H
0100 = PWM3L
0011 = PWM2H
0010 = PWM2L
0001 = PWM1H
0000 = PWM1L

REGISTER 25-5: **CMxMSKCON: COMPARATOR x MASK GATING CONTROL REGISTER (CONTINUED)**

bit 3   **ABEN:** AND Gate B Input Enable bit

1 = MBI is connected to AND gate
0 = MBI is not connected to AND gate

bit 2   **ABNEN:** AND Gate B Input Inverted Enable bit

1 = Inverted MBI is connected to AND gate
0 = Inverted MBI is not connected to AND gate

bit 1   **AAEN:** AND Gate A Input Enable bit

1 = MAI is connected to AND gate
0 = MAI is not connected to AND gate

bit 0   **AANEN:** AND Gate A Input Inverted Enable bit

1 = Inverted MAI is connected to AND gate
0 = Inverted MAI is not connected to AND gate

REGISTER 25-7: CVRCON: COMPARATOR VOLTAGE REFERENCE CONTROL REGISTER

U-0	R/W-0	U-0	U-0	U-0	R/W-0	U-0	U-0
—	CVR2OE[1]	—	—	—	VREFSEL	—	—
bit 15							bit 8

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
CVREN	CVR1OE[1]	CVRR	CVRSS[2]	CVR3	CVR2	CVR1	CVR0
bit 7							bit 0

Legend:		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15 **Unimplemented:** Read as '0'

bit 14 **CVR2OE:** Comparator Voltage Reference 2 Output Enable bit[1]

1 = (AVDD – AVSS)/2 is connected to the CVREF2O pin
0 = (AVDD – AVSS)/2 is disconnected from the CVREF2O pin

bit 13-11 **Unimplemented:** Read as '0'

bit 10 **VREFSEL:** Comparator Voltage Reference Select bit

1 = CVREFIN = VREF+
0 = CVREFIN is generated by the resistor network

bit 9-8 **Unimplemented:** Read as '0'

bit 7 **CVREN:** Comparator Voltage Reference Enable bit

1 = Comparator voltage reference circuit is powered on
0 = Comparator voltage reference circuit is powered down

bit 6 **CVR1OE:** Comparator Voltage Reference 1 Output Enable bit[1]

1 = Voltage level is output on the CVREF1O pin
0 = Voltage level is disconnected from then CVREF1O pin

bit 5 **CVRR:** Comparator Voltage Reference Range Selection bit

1 = CVRSRC/24 step-size
0 = CVRSRC/32 step-size

bit 4 **CVRSS:** Comparator Voltage Reference Source Selection bit[2]

1 = Comparator voltage reference source, CVRSRC = (VREF+) – (AVSS)
0 = Comparator voltage reference source, CVRSRC = AVDD – AVSS

bit 3-0 **CVR<3:0>** Comparator Voltage Reference Value Selection $0 \leq$ CVR<3:0> $\leq$ 15 bits

When CVRR = 1:
CVREFIN = (CVR<3:0>/24) • (CVRSRC)

When CVRR = 0:
CVREFIN = (CVRSRC/4) + (CVR<3:0>/32) • (CVRSRC)

Note 1: CVRxOE overrides the TRISx and the ANSELx bit settings.

2: In order to operate with CVRSS = 1, at least one of the comparator modules must be enabled.

TABLE 30-12: DC CHARACTERISTICS: I/O PIN OUTPUT SPECIFICATIONS

DC CHARACTERISTICS			Standard Operating Conditions: 3.0V to 3.6V (unless otherwise stated) Operating temperature -40°C ≤ TA ≤ +85°C for Industrial -40°C ≤ TA ≤ +125°C for Extended				
Param.	Symbol	Characteristic	Min.	Typ.	Max.	Units	Conditions
DO10	VOL	Output Low Voltage 4x Sink Driver Pins[2]	—	—	0.4	V	VDD = 3.3V, IOL ≤ 6 mA, -40°C ≤ TA ≤ +85°C IOL ≤ 5 mA, +85°C < TA ≤ +125°C
		Output Low Voltage 8x Sink Driver Pins[3]	—	—	0.4	V	VDD = 3.3V, IOL ≤ 12 mA, -40°C ≤ TA ≤ +85°C IOL ≤ 8 mA, +85°C < TA ≤ +125°C
DO20	VOH	Output High Voltage 4x Source Driver Pins[2]	2.4	—	—	V	IOH ≥ -10 mA, VDD = 3.3V
		Output High Voltage 8x Source Driver Pins[3]	2.4	—	—	V	IOH ≥ -15 mA, VDD = 3.3V
DO20A	VOH1	Output High Voltage 4x Source Driver Pins[2]	1.5[1]	—	—	V	IOH ≥ -14 mA, VDD = 3.3V
			2.0[1]	—	—		IOH ≥ -12 mA, VDD = 3.3V
			3.0[1]	—	—		IOH ≥ -7 mA, VDD = 3.3V
		Output High Voltage 8x Source Driver Pins[3]	1.5[1]	—	—	V	IOH ≥ -22 mA, VDD = 3.3V
			2.0[1]	—	—		IOH ≥ -18 mA, VDD = 3.3V
			3.0[1]	—	—		IOH ≥ -10 mA, VDD = 3.3V

Note 1: Parameters are characterized but not tested.

2: Includes all I/O pins that are not 8x Sink Driver pins (see below).

3: Includes the following pins:
For devices with less than 64 pins: RA3, RA4, RA9, RB<7:15> and RC3
For 64-pin devices: RA4, RA9, RB<7:15>, RC3 and RC15
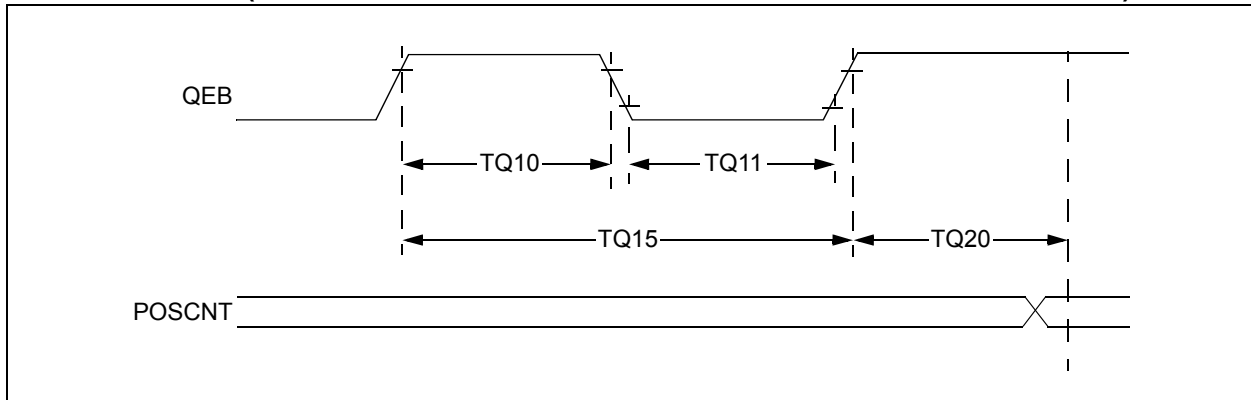
TABLE 30-13: ELECTRICAL CHARACTERISTICS: BOR

DC CHARACTERISTICS			Standard Operating Conditions: 3.0V to 3.6V (unless otherwise stated)[1] Operating temperature -40°C ≤ TA ≤ +85°C for Industrial -40°C ≤ TA ≤ +125°C for Extended				
Param No.	Symbol	Characteristic	Min.[2]	Typ.	Max.	Units	Conditions
BO10	VBOR	BOR Event on VDD Transition High-to-Low	2.65	—	2.95	V	VDD **(Notes 2 and 3)**

Note 1: Device is functional at VBORMIN < VDD < VDDMIN, but will have degraded performance. Device functionality is tested, but not characterized. Analog modules (ADC, op amp/comparator and comparator voltage reference) may have degraded performance.

2: Parameters are for design guidance only and are not tested in manufacturing.

3: The VBOR specification is relative to VDD.

FIGURE 30-11: TIMERQ (QEI MODULE) EXTERNAL CLOCK TIMING CHARACTERISTICS
(dsPIC33EPXXXMC20X/50X AND PIC24EPXXXMC20X DEVICES ONLY)

TABLE 30-30: QEI MODULE EXTERNAL CLOCK TIMING REQUIREMENTS
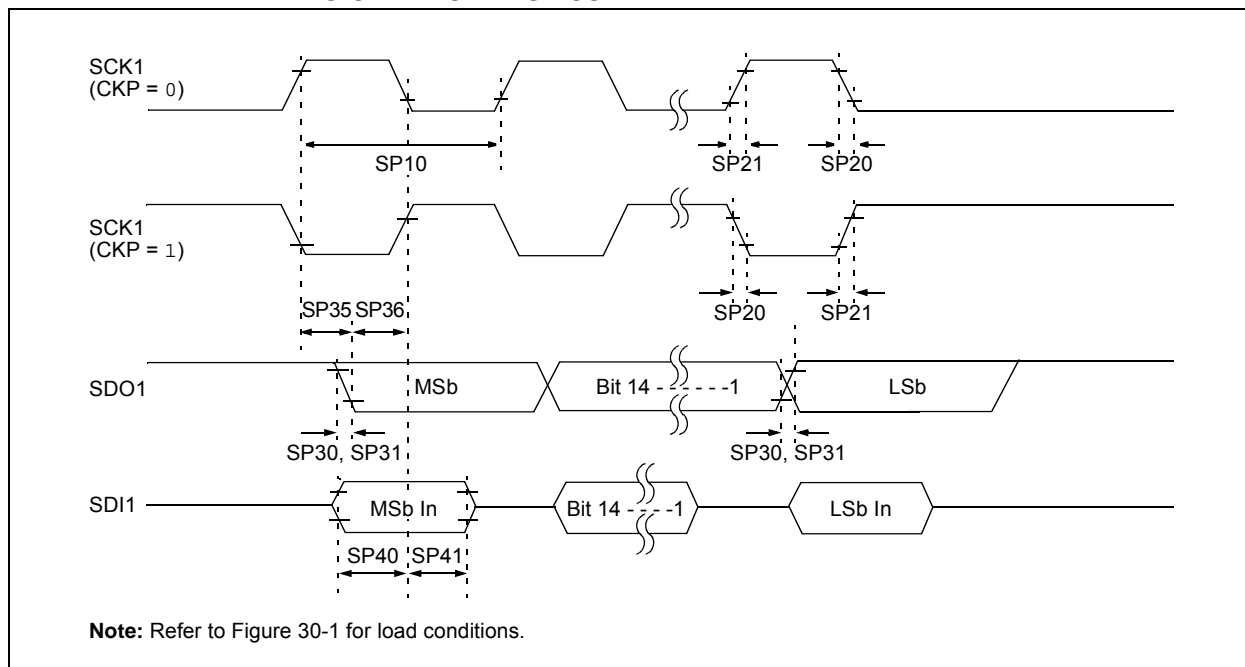(dsPIC33EPXXXMC20X/50X AND PIC24EPXXXMC20X DEVICES ONLY)

AC CHARACTERISTICS				Standard Operating Conditions: 3.0V to 3.6V (unless otherwise stated) Operating temperature -40°C ≤ TA ≤ +85°C for Industrial -40°C ≤ TA ≤ +125°C for Extended				
Param No.	Symbol	Characteristic[1]		Min.	Typ.	Max.	Units	Conditions
TQ10	TtQH	TQCK High Time	Synchronous, with prescaler	Greater of 12.5 + 25 or (0.5 TCY/N) + 25	—	—	ns	Must also meet Parameter TQ15
TQ11	TtQL	TQCK Low Time	Synchronous, with prescaler	Greater of 12.5 + 25 or (0.5 TCY/N) + 25	—	—	ns	Must also meet Parameter TQ15
TQ15	TtQP	TQCP Input Period	Synchronous, with prescaler	Greater of 25 + 50 or (1 TCY/N) + 50	—	—	ns	
TQ20	TCKEXTMRL	Delay from External TQCK Clock Edge to Timer Increment		—	1	TCY	—	

Note 1: These parameters are characterized but not tested in manufacturing.

FIGURE 30-20: **SPI2 SLAVE MODE (FULL-DUPLEX, CKE = 0, CKP = 1, SMP = 0) TIMING CHARACTERISTICS**
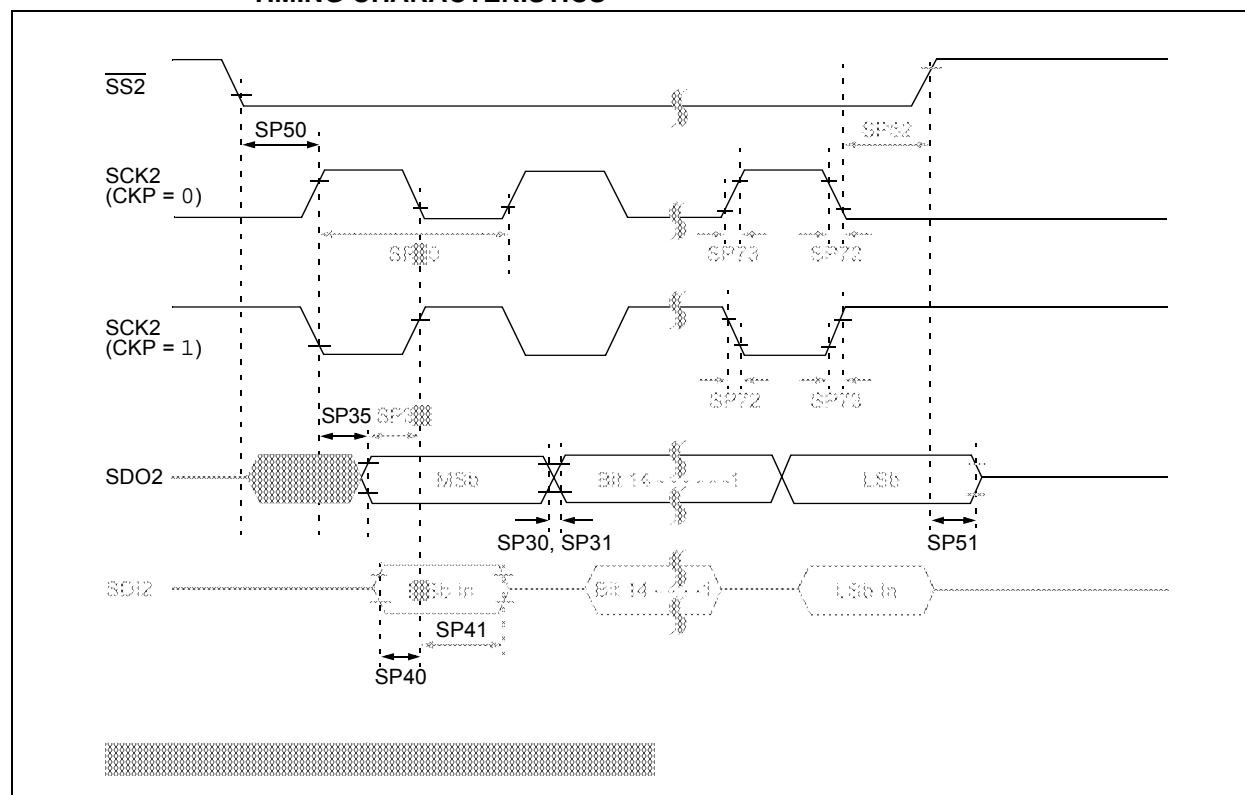
FIGURE 30-25: **SPI1 MASTER MODE (FULL-DUPLEX, CKE = 0, CKP = x, SMP = 1) TIMING CHARACTERISTICS**

Note: Refer to Figure 30-1 for load conditions.

TABLE 30-44: SPI1 MASTER MODE (FULL-DUPLEX, CKE = 0, CKP = x, SMP = 1) TIMING REQUIREMENTS

AC CHARACTERISTICS			Standard Operating Conditions: 3.0V to 3.6V (unless otherwise stated) Operating temperature -40°C ≤ TA ≤ +85°C for Industrial -40°C ≤ TA ≤ +125°C for Extended				
Param.	Symbol	Characteristic[1]	Min.	Typ.[2]	Max.	Units	Conditions
SP10	FscP	Maximum SCK1 Frequency	—	—	10	MHz	-40ºC to +125ºC **(Note 3)**
SP20	TscF	SCK1 Output Fall Time	—	—	—	ns	See Parameter DO32 **(Note 4)**
SP21	TscR	SCK1 Output Rise Time	—	—	—	ns	See Parameter DO31 **(Note 4)**
SP30	TdoF	SDO1 Data Output Fall Time	—	—	—	ns	See Parameter DO32 **(Note 4)**
SP31	TdoR	SDO1 Data Output Rise Time	—	—	—	ns	See Parameter DO31 **(Note 4)**
SP35	TscH2doV, TscL2doV	SDO1 Data Output Valid after SCK1 Edge	—	6	20	ns	
SP36	TdoV2scH, TdoV2scL	SDO1 Data Output Setup to First SCK1 Edge	30	—	—	ns	
SP40	TdiV2scH, TdiV2scL	Setup Time of SDI1 Data Input to SCK1 Edge	30	—	—	ns	
SP41	TscH2diL, TscL2diL	Hold Time of SDI1 Data Input to SCK1 Edge	30	—	—	ns	

Note 1: These parameters are characterized, but are not tested in manufacturing.

2: Data in "Typical" column is at 3.3V, +25°C unless otherwise stated.

3: The minimum clock period for SCK1 is 100 ns. The clock generated in Master mode must not violate this specification.

4: Assumes 50 pF load on all SPI1 pins.

TABLE 30-57: ADC MODULE SPECIFICATIONS

AC CHARACTERISTICS			**Standard Operating Conditions: 3.0V to 3.6V (unless otherwise stated)[1]** Operating temperature $-40°C \leq T_A \leq +85°C$ for Industrial $-40°C \leq T_A \leq +125°C$ for Extended				
Param No.	**Symbol**	**Characteristic**	**Min.**	**Typ.**	**Max.**	**Units**	**Conditions**
Device Supply							
AD01	AV$_{DD}$	Module V$_{DD}$ Supply	Greater of: V$_{DD}$ – 0.3 or 3.0	—	Lesser of: V$_{DD}$ + 0.3 or 3.6	V	
AD02	AV$_{SS}$	Module V$_{SS}$ Supply	V$_{SS}$ – 0.3	—	V$_{SS}$ + 0.3	V	
Reference Inputs							
AD05	V$_{REFH}$	Reference Voltage High	AV$_{SS}$ + 2.5	—	AV$_{DD}$	V	V$_{REFH}$ = V$_{REF+}$ V$_{REFL}$ = V$_{REF-}$ **(Note 1)**
AD05a			3.0	—	3.6	V	V$_{REFH}$ = AV$_{DD}$ V$_{REFL}$ = AV$_{SS}$ = 0
AD06	V$_{REFL}$	Reference Voltage Low	AV$_{SS}$	—	AV$_{DD}$ – 2.5	V	**(Note 1)**
AD06a			0	—	0	V	V$_{REFH}$ = AV$_{DD}$ V$_{REFL}$ = AV$_{SS}$ = 0
AD07	V$_{REF}$	Absolute Reference Voltage	2.5	—	3.6	V	V$_{REF}$ = V$_{REFH}$ - V$_{REFL}$
AD08	I$_{REF}$	Current Drain	— —	— —	10 600	µA µA	ADC off ADC on
AD09	I$_{AD}$	Operating Current[2]	—	5	—	mA	ADC operating in 10-bit mode **(Note 1)**
			—	2	—	mA	ADC operating in 12-bit mode **(Note 1)**
Analog Input							
AD12	V$_{INH}$	Input Voltage Range V$_{INH}$	V$_{INL}$	—	V$_{REFH}$	V	This voltage reflects Sample-and-Hold Channels 0, 1, 2 and 3 (CH0-CH3), positive input
AD13	V$_{INL}$	Input Voltage Range V$_{INL}$	V$_{REFL}$	—	AV$_{SS}$ + 1V	V	This voltage reflects Sample-and-Hold Channels 0, 1, 2 and 3 (CH0-CH3), negative input
AD17	R$_{IN}$	Recommended Impedance of Analog Voltage Source	—	—	200	Ω	Impedance to achieve maximum performance of ADC

Note 1: Device is functional at V$_{BORMIN}$ < V$_{DD}$ < V$_{DDMIN}$, but will have degraded performance. Device functionality is tested, but not characterized. Analog modules (ADC, op amp/comparator and comparator voltage reference) may have degraded performance. Refer to Parameter BO10 in Table 30-13 for the minimum and maximum BOR values.

   2: Parameter is characterized but not tested in manufacturing.

TABLE 31-8: DC CHARACTERISTICS: I/O PIN OUTPUT SPECIFICATIONS

\ DC CHARACTERISTICS			Standard Operating Conditions: 3.0V to 3.6V (unless otherwise stated) Operating temperature -40°C ≤ TA ≤ +150°C				
Param.	Symbol	Characteristic	Min.	Typ.	Max.	Units	Conditions
HDO10	VOL	**Output Low Voltage** 4x Sink Driver Pins[2]	—	—	0.4	V	IOL ≤ 5 mA, VDD = 3.3V **(Note 1)**
		Output Low Voltage 8x Sink Driver Pins[3]	—	—	0.4	V	IOL ≤ 8 mA, VDD = 3.3V **(Note 1)**
HDO20	VOH	**Output High Voltage** 4x Source Driver Pins[2]	2.4	—	—	V	IOH ≥ -10 mA, VDD = 3.3V **(Note 1)**
		Output High Voltage 8x Source Driver Pins[3]	2.4	—	—	V	IOH ≥ 15 mA, VDD = 3.3V **(Note 1)**
HDO20A	VOH1	**Output High Voltage** 4x Source Driver Pins[2]	1.5	—	—	V	IOH ≥ -3.9 mA, VDD = 3.3V **(Note 1)**
			2.0	—	—		IOH ≥ -3.7 mA, VDD = 3.3V **(Note 1)**
			3.0	—	—		IOH ≥ -2 mA, VDD = 3.3V **(Note 1)**
		Output High Voltage 8x Source Driver Pins[3]	1.5	—	—	V	IOH ≥ -7.5 mA, VDD = 3.3V **(Note 1)**
			2.0	—	—		IOH ≥ -6.8 mA, VDD = 3.3V **(Note 1)**
			3.0	—	—		IOH ≥ -3 mA, VDD = 3.3V **(Note 1)**

Note 1: Parameters are characterized, but not tested.

2: Includes all I/O pins that are not 8x Sink Driver pins (see below).
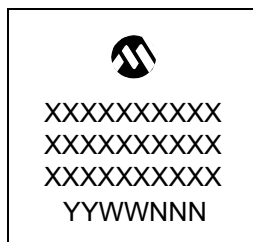
3: Includes the following pins:
For devices with less than 64 pins: RA3, RA4, RA9, RB<15:7> and RC3
For 64-pin devices: RA4, RA9, RB<15:7>, RC3 and RC15

NOTES:
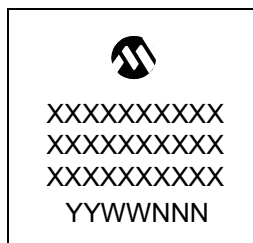
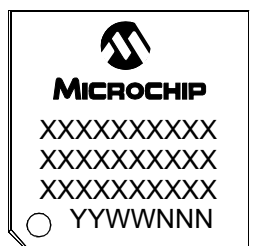## 33.1   Package Marking Information (Continued)
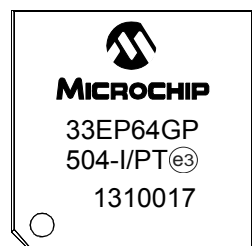
36-Lead VTLA (TLA)

```
        (M)
    XXXXXXXXX
    XXXXXXXXX
    XXXXXXXXX
     YYWWNNN
```

Example

```
        (M)
    33EP64GP
    504-I/TL(e3)
     1310017
```

44-Lead VTLA (TLA)

```
        (M)
    XXXXXXXXX
    XXXXXXXXX
    XXXXXXXXX
     YYWWNNN
```

Example

```
        (M)
    33EP64GP
    504-I/TL(e3)
     1310017
```

44-Lead TQFP

```
     (M) MICROCHIP
    XXXXXXXXX
    XXXXXXXXX
    XXXXXXXXX
  ◯  YYWWNNN
```

Example

```
     (M) MICROCHIP
    33EP64GP
    504-I/PT(e3)
  ◯   1310017
```

44-Lead QFN (8x8x0.9 mm)

```
        (M)
   XXXXXXXXXX
   XXXXXXXXXX
   XXXXXXXXXX
     YYWWNNN
```

Example

```
        (M)
   33EP64GP
   504-I/ML (e3)
     1310017
```
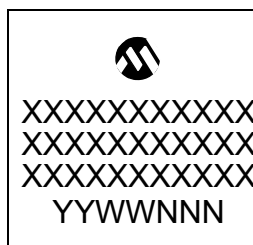
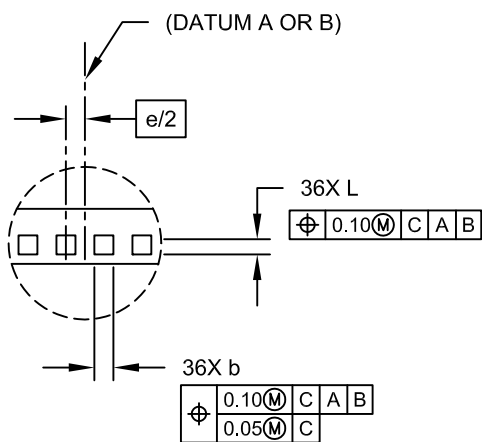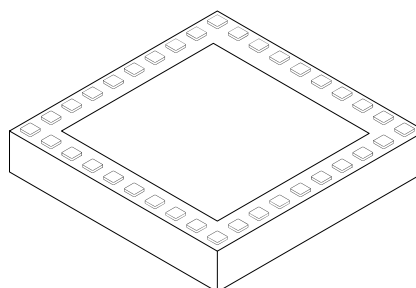## 36-Terminal Very Thin Thermal Leadless Array Package (TL) – 5x5x0.9 mm Body with Exposed Pad [VTLA]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging

(DATUM A OR B)

e/2

36X L
⊕ | 0.10 Ⓜ | C | A | B

36X b
⊕ | 0.10 Ⓜ | C | A | B
| 0.05 Ⓜ | C

DETAIL A

	Units	MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Number of Pins	N		36	
Number of Pins per Side	ND		10	
Number of Pins per Side	NE		8	
Pitch	e		0.50 BSC	
Overall Height	A	0.80	0.90	1.00
Standoff	A1	0.025	-	0.075
Overall Width	E		5.00 BSC	
Exposed Pad Width	E2	3.60	3.75	3.90
Overall Length	D		5.00 BSC	
Exposed Pad Length	D2	3.60	3.75	3.90
Contact Width	b	0.20	0.25	0.30
Contact Length	L	0.20	0.25	0.30
Contact-to-Exposed Pad	K	0.20	-	-

Notes:
1. Pin 1 visual index feature may vary, but must be located within the hatched area.
2. Package is saw singulated.
3. Dimensioning and tolerancing per ASME Y14.5M.
    BSC: Basic Dimension. Theoretically exact value shown without tolerances.
    REF: Reference Dimension, usually without tolerance, for information purposes only.

Microchip Technology Drawing C04-187C Sheet 2 of 2