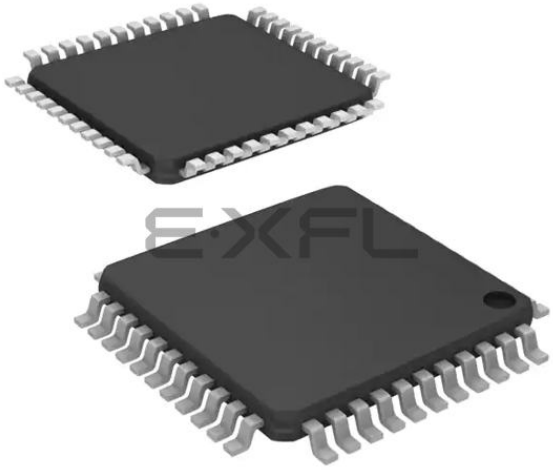

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## What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

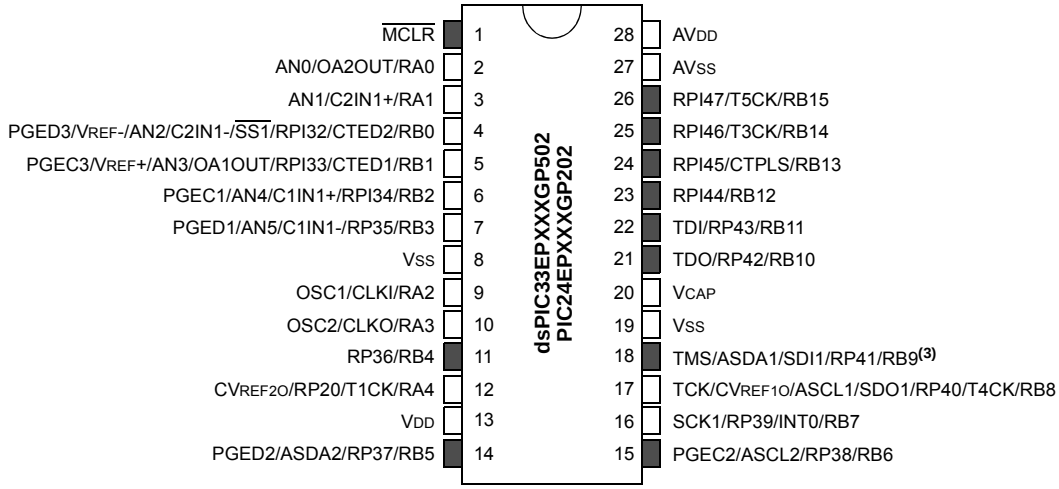
## Applications of "Embedded - Microcontrollers"

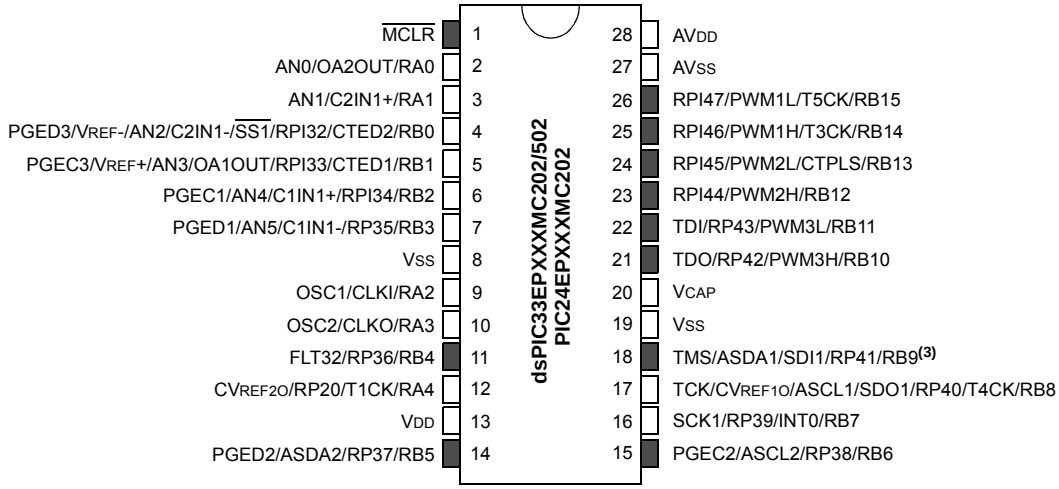
| Details | |
|---|---|
| Product Status | Active |
| Core Processor | PIC |
| Core Size | 16-Bit |
| Speed | 70 MIPs |
| Connectivity | I²C, IrDA, LINbus, QEI, SPI, UART/USART |
| Peripherals | Brown-out Detect/Reset, DMA, Motor Control PWM, POR, PWM, WDT |
| Number of I/O | 35 |
| Program Memory Size | 128KB (43K x 24) |
| Program Memory Type | FLASH |
| EEPROM Size | - |
| RAM Size | 8K x 16 |
| Voltage - Supply (Vcc/Vdd) | 3V ~ 3.6V |
| Data Converters | A/D 9x10b/12b |
| Oscillator Type | Internal |
| Operating Temperature | -40°C ~ 85°C (TA) |
| Mounting Type | Surface Mount |
| Package / Case | 44-TQFP |
| Supplier Device Package | 44-TQFP (10x10) |
| Purchase URL | https://www.e-xfl.com/product-detail/microchip-technology/pic24ep128mc204t-i-pt |

## Pin Diagrams

**28-Pin SPDIP/SOIC/SSOP(1,2)**

■ = Pins are up to 5V tolerant




**Note 1:** The RPn/RPIn pins can be used by any remappable peripheral with some limitation. See **Section 11.4 "Peripheral Pin Select (PPS)"** for available peripherals and for information on limitations.

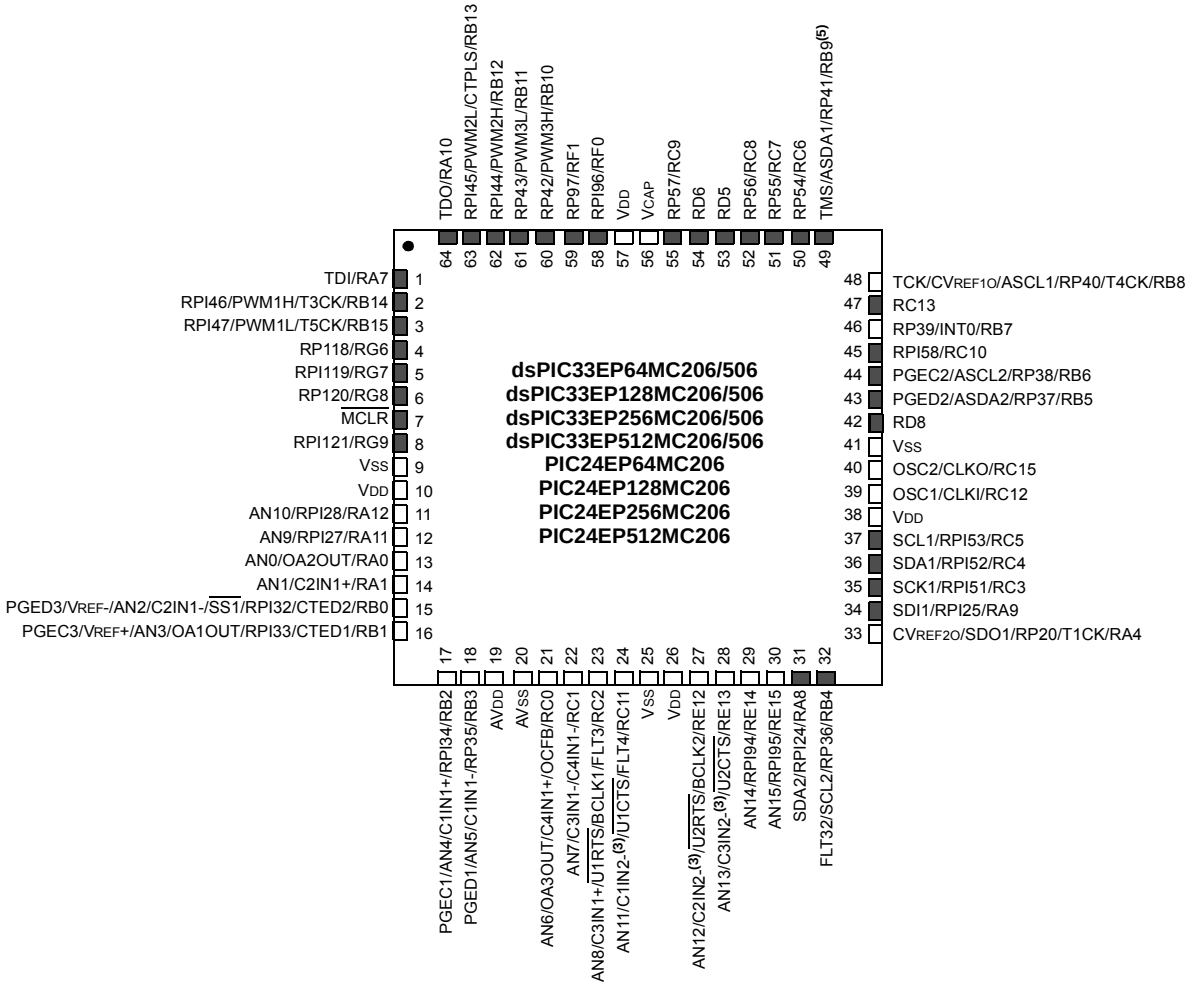
**2:** Every I/O port pin (RAx-RGx) can be used as a Change Notification pin (CNAx-CNGx). See **Section 11.0 "I/O Ports"** for more information.

**3:** There is an internal pull-up resistor connected to the TMS pin when the JTAG interface is active. See the JTAGEN bit field in Table 27-2.

## Pin Diagrams (Continued)

**64-Pin QFN(1,2,3,4)**

■ = Pins are up to 5V tolerant




**Note 1:** The RPn/RPIn pins can be used by any remappable peripheral with some limitation. See **Section 11.4 "Peripheral Pin Select (PPS)"** for available peripherals and for information on limitations.

**2:** Every I/O port pin (RAx-RGx) can be used as a Change Notification pin (CNAx-CNGx). See **Section 11.0 "I/O Ports"** for more information.

**3:** This pin is not available as an input when OPMODE (CMxCON<10>) = 1.

**4:** The metal pad at the bottom of the device is not connected to any pins and is recommended to be connected to VSS externally.

**5:** There is an internal pull-up resistor connected to the TMS pin when the JTAG interface is active. See the JTAGEN bit field in Table 27-2.

## 1.0 DEVICE OVERVIEW

**Note 1:** This data sheet summarizes the features of the dsPIC33EPXXXGP50X, dsPIC33EPXXXMC20X/50X and PIC24EPXXXGP/MC20X families of devices. It is not intended to be a comprehensive resource. To complement the information in this data sheet, refer to the related section of the "*dsPIC33/PIC24 Family Reference Manual*", which is available from the Microchip web site (www.microchip.com)

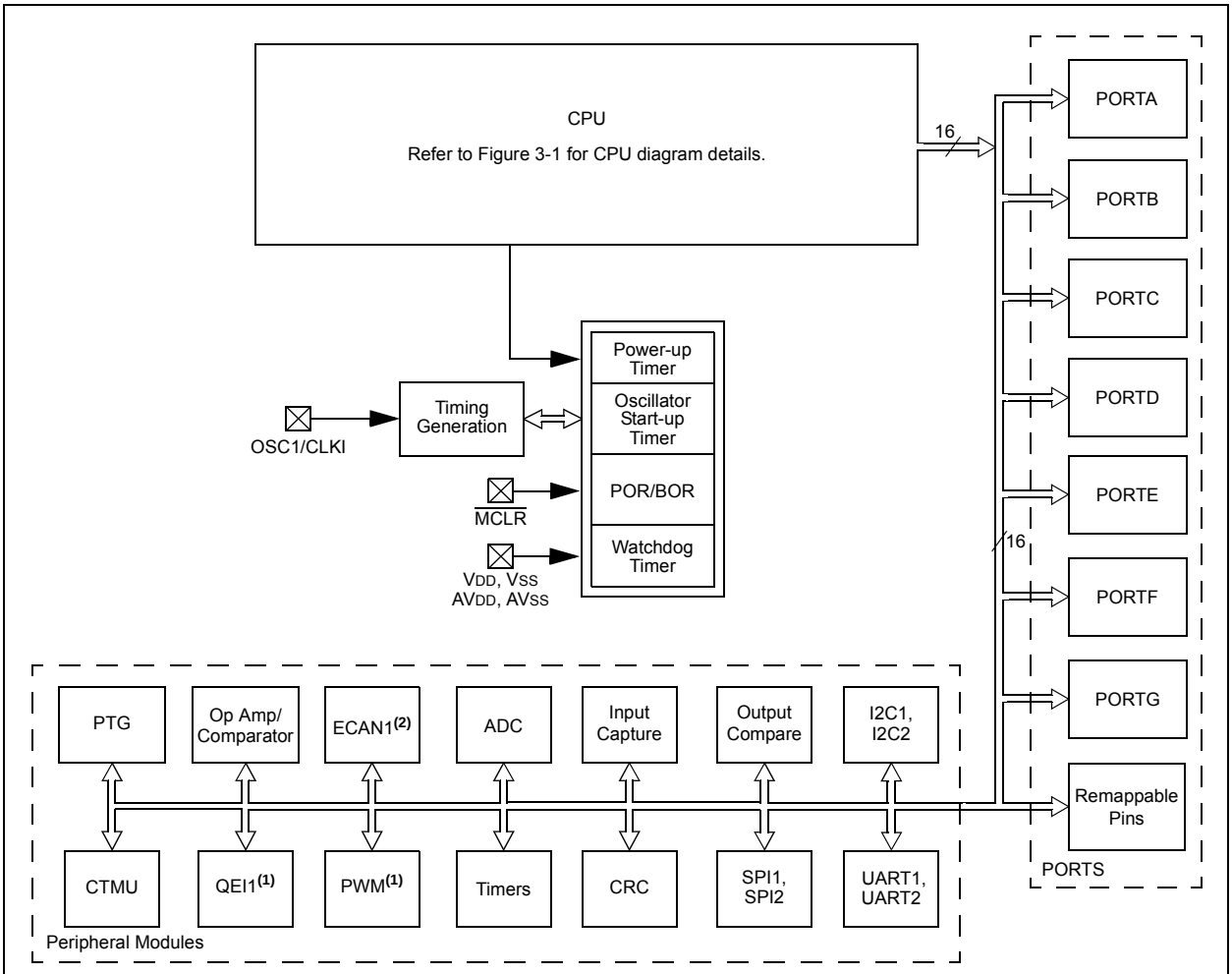
**2:** Some registers and associated bits described in this section may not be available on all devices. Refer to **Section 4.0 "Memory Organization"** in this data sheet for device-specific register and bit information.

This document contains device-specific information for the dsPIC33EPXXXGP50X, dsPIC33EPXXXMC20X/50X and PIC24EPXXXGP/MC20X Digital Signal Controller (DSC) and Microcontroller (MCU) devices.

dsPIC33EPXXXMC20X/50X and dsPIC33EPXXXGP50X devices contain extensive Digital Signal Processor (DSP) functionality with a high-performance, 16-bit MCU architecture.

Figure 1-1 shows a general block diagram of the core and peripheral modules. Table 1-1 lists the functions of the various pins shown in the pinout diagrams.

**FIGURE 1-1: dsPIC33EPXXXGP50X, dsPIC33EPXXXMC20X/50X AND PIC24EPXXXGP/MC20X BLOCK DIAGRAM**




**Note 1:** This feature or peripheral is only available on dsPIC33EPXXXMC20X/50X and PIC24EPXXXMC20X devices.

**2:** This feature or peripheral is only available on dsPIC33EPXXXGP/MC50X devices.

**FIGURE 2-7: INTERLEAVED PFC**

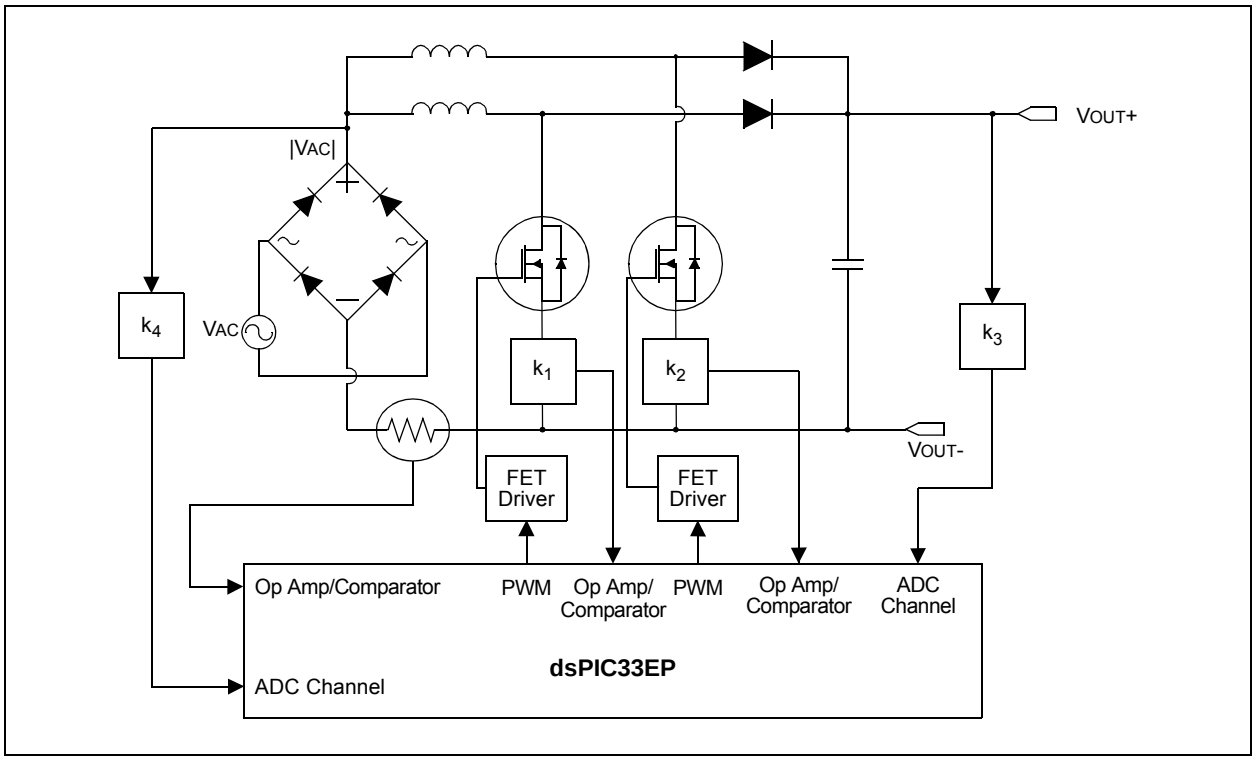



**FIGURE 2-8: BEMF VOLTAGE MEASURED USING THE ADC MODULE**

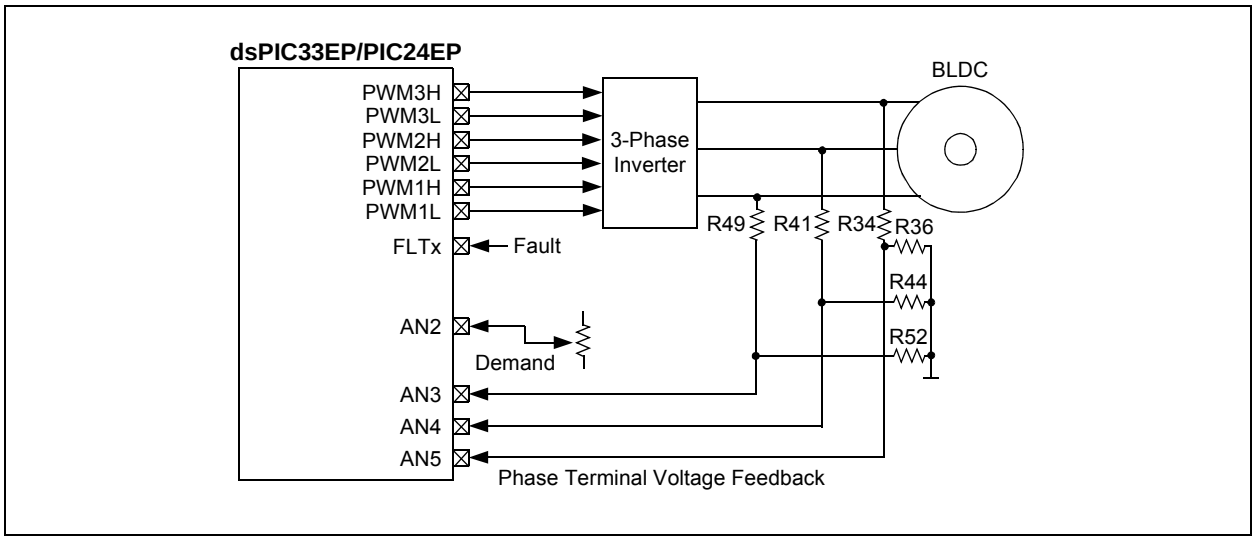


**TABLE 4-46: PORTA REGISTER MAP FOR PIC24EPXXXGP/MC206 AND dsPIC33EPXXXGP/MC206/506 DEVICES ONLY**

| File Name | Addr. | Bit 15 | Bit 14 | Bit 13 | Bit 12 | Bit 11 | Bit 10 | Bit 9 | Bit 8 | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 | All Resets |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| TRISA | 0E00 | — | — | — | TRISA12 | TRISA11 | TRISA10 | TRISA9 | TRISA8 | TRISA7 | — | — | TRISA4 | — | — | TRISA1 | TRISA0 | 1F93 |
| PORTA | 0E02 | — | — | — | RA12 | RA11 | RA10 | RA9 | RA8 | RA7 | — | — | RA4 | — | — | RA1 | RA0 | 0000 |
| LATA | 0E04 | — | — | — | LATA12 | LATA11 | LATA10 | LATA9 | LATA8 | LATA7 | — | — | LATA4 | — | — | LA1TA1 | LA0TA0 | 0000 |
| ODCA | 0E06 | — | — | — | ODCA12 | ODCA11 | ODCA10 | ODCA9 | ODCA8 | ODCA7 | — | — | ODCA4 | — | — | ODCA1 | ODCA0 | 0000 |
| CNENA | 0E08 | — | — | — | CNIEA12 | CNIEA11 | CNIEA10 | CNIEA9 | CNIEA8 | CNIEA7 | — | — | CNIEA4 | — | — | CNIEA1 | CNIEA0 | 0000 |
| CNPUA | 0E0A | — | — | — | CNPUA12 | CNPUA11 | CNPUA10 | CNPUA9 | CNPUA8 | CNPUA7 | — | — | CNPUA4 | — | — | CNPUA1 | CNPUA0 | 0000 |
| CNPDA | 0E0C | — | — | — | CNPDA12 | CNPDA11 | CNPDA10 | CNPDA9 | CNPDA8 | CNPDA7 | — | — | CNPDA4 | — | — | CNPDA1 | CNPDA0 | 0000 |
| ANSELA | 0E0E | — | — | — | ANSA12 | ANSA11 | — | — | — | — | — | — | ANSA4 | — | — | ANSA1 | ANSA0 | 1813 |

**Legend:** — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

**TABLE 4-47: PORTB REGISTER MAP FOR PIC24EPXXXGP/MC206 AND dsPIC33EPXXXGP/MC206/506 DEVICES ONLY**

| File Name | Addr. | Bit 15 | Bit 14 | Bit 13 | Bit 12 | Bit 11 | Bit 10 | Bit 9 | Bit 8 | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 | All Resets |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| TRISB | 0E10 | TRISB15 | TRISB14 | TRISB13 | TRISB12 | TRISB11 | TRISB10 | TRISB9 | TRISB8 | TRISB7 | TRISB6 | TRISB5 | TRISB4 | TRISB3 | TRISB2 | TRISB1 | TRISB0 | FFFF |
| PORTB | 0E12 | RB15 | RB14 | RB13 | RB12 | RB11 | RB10 | RB9 | RB8 | RB7 | RB6 | RB5 | RB4 | RB3 | RB2 | RB1 | RB0 | xxxx |
| LATB | 0E14 | LATB15 | LATB14 | LATB13 | LATB12 | LATB11 | LATB10 | LATB9 | LATB8 | LATB7 | LATB6 | LATB5 | LATB4 | LATB3 | LATB2 | LATB1 | LATB0 | xxxx |
| ODCB | 0E16 | ODCB15 | ODCB14 | ODCB13 | ODCB12 | ODCB11 | ODCB10 | ODCB9 | ODCB8 | ODCB7 | ODCB6 | ODCB5 | ODCB4 | ODCB3 | ODCB2 | ODCB1 | ODCB0 | 0000 |
| CNENB | 0E18 | CNIEB15 | CNIEB14 | CNIEB13 | CNIEB12 | CNIEB11 | CNIEB10 | CNIEB9 | CNIEB8 | CNIEB7 | CNIEB6 | CNIEB5 | CNIEB4 | CNIEB3 | CNIEB2 | CNIEB1 | CNIEB0 | 0000 |
| CNPUB | 0E1A | CNPUB15 | CNPUB14 | CNPUB13 | CNPUB12 | CNPUB11 | CNPUB10 | CNPUB9 | CNPUB8 | CNPUB7 | CNPUB6 | CNPUB5 | CNPUB4 | CNPUB3 | CNPUB2 | CNPUB1 | CNPUB0 | 0000 |
| CNPDB | 0E1C | CNPDB15 | CNPDB14 | CNPDB13 | CNPDB12 | CNPDB11 | CNPDB10 | CNPDB9 | CNPDB8 | CNPDB7 | CNPDB6 | CNPDB5 | CNPDB4 | CNPDB3 | CNPDB2 | CNPDB1 | CNPDB0 | 0000 |
| ANSELB | 0E1E | — | — | — | — | — | — | — | ANSB8 | — | — | — | — | ANSB3 | ANSB2 | ANSB1 | ANSB0 | 010F |

**Legend:** x = unknown value on Reset, — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

**TABLE 4-48: PORTC REGISTER MAP FOR PIC24EPXXXGP/MC206 AND dsPIC33EPXXXGP/MC206/506 DEVICES ONLY**

| File Name | Addr. | Bit 15 | Bit 14 | Bit 13 | Bit 12 | Bit 11 | Bit 10 | Bit 9 | Bit 8 | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 | All Resets |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| TRISC | 0E20 | TRISC15 | — | TRISC13 | TRISC12 | TRISC11 | TRISC10 | TRISC9 | TRISC8 | TRISC7 | TRISC6 | TRISC5 | TRISC4 | TRISC3 | TRISC2 | TRISC1 | TRISC0 | BFFF |
| PORTC | 0E22 | RC15 | — | RC13 | RC12 | RC11 | RC10 | RC9 | RC8 | RC7 | RC6 | RC5 | RC4 | RC3 | RC2 | RC1 | RC0 | xxxx |
| LATC | 0E24 | LATC15 | — | LATC13 | LATC12 | LATC11 | LATC10 | LATC9 | LATC8 | LATC7 | LATC6 | LATC5 | LATC4 | LATC3 | LATC2 | LATC1 | LATC0 | xxxx |
| ODCC | 0E26 | ODCC15 | — | ODCC13 | ODCC12 | ODCC11 | ODCC10 | ODCC9 | ODCC8 | ODCC7 | ODCC6 | ODCC5 | ODCC4 | ODCC3 | ODCC2 | ODCC1 | ODCC0 | 0000 |
| CNENC | 0E28 | CNIEC15 | — | CNIEC13 | CNIEC12 | CNIEC11 | CNIEC10 | CNIEC9 | CNIEC8 | CNIEC7 | CNIEC6 | CNIEC5 | CNIEC4 | CNIEC3 | CNIEC2 | CNIEC1 | CNIEC0 | 0000 |
| CNPUC | 0E2A | CNPUC15 | — | CNPUC13 | CNPUC12 | CNPUC11 | CNPUC10 | CNPUC9 | CNPUC8 | CNPUC7 | CNPUC6 | CNPUC5 | CNPUC4 | CNPUC3 | CNPUC2 | CNPUC1 | CNPUC0 | 0000 |
| CNPDC | 0E2C | CNPDC15 | — | CNPDC13 | CNPDC12 | CNPDC11 | CNPDC10 | CNPDC9 | CNPDC8 | CNPDC7 | CNPDC6 | CNPDC5 | CNPDC4 | CNPDC3 | CNPDC2 | CNPDC1 | CNPDC0 | 0000 |
| ANSELC | 0E2E | — | — | — | — | ANSC11 | — | — | — | — | — | — | — | — | ANSC2 | ANSC1 | ANSC0 | 0807 |

**Legend:** x = unknown value on Reset, — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

**REGISTER 9-1: OSCCON: OSCILLATOR CONTROL REGISTER(1) (CONTINUED)**

bit 4 **Unimplemented:** Read as '0'

bit 3 **CF:** Clock Fail Detect bit(3)
- 1 = FSCM has detected clock failure
- 0 = FSCM has not detected clock failure

bit 2-1 **Unimplemented:** Read as '0'

bit 0 **OSWEN:** Oscillator Switch Enable bit
- 1 = Requests oscillator switch to selection specified by the NOSC<2:0> bits
- 0 = Oscillator switch is complete

**Note 1:** Writes to this register require an unlock sequence. Refer to **"Oscillator"** (DS70580) in the *"dsPIC33/PIC24 Family Reference Manual"* (available from the Microchip web site) for details.

**2:** Direct clock switches between any primary oscillator mode with PLL and FRCPLL mode are not permitted. This applies to clock switches in either direction. In these instances, the application must switch to FRC mode as a transitional clock source between the two PLL modes.

**3:** This bit should only be cleared in software. Setting the bit in software (= 1) will have the same effect as an actual oscillator failure and trigger an oscillator failure trap.

**REGISTER 10-5: PMD6: PERIPHERAL MODULE DISABLE CONTROL REGISTER 6**

| U-0 | U-0 | U-0 | U-0 | U-0 | R/W-0 | R/W-0 | R/W-0 |
|---|---|---|---|---|---|---|---|
| — | — | — | — | — | PWM3MD(1) | PWM2MD(1) | PWM1MD(1) |
| bit 15 | | | | | | | bit 8 |

| U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 |
|---|---|---|---|---|---|---|---|
| — | — | — | — | — | — | — | — |
| bit 7 | | | | | | | bit 0 |

| **Legend:** | | | |
|---|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as '0' | |
| -n = Value at POR | '1' = Bit is set | '0' = Bit is cleared | x = Bit is unknown |

bit 15-11 **Unimplemented:** Read as '0'

bit 10 **PWM3MD:** PWM3 Module Disable bit(1)
1 = PWM3 module is disabled
0 = PWM3 module is enabled

bit 9 **PWM2MD:** PWM2 Module Disable bit(1)
1 = PWM2 module is disabled
0 = PWM2 module is enabled

bit 8 **PWM1MD:** PWM1 Module Disable bit(1)
1 = PWM1 module is disabled
0 = PWM1 module is enabled

bit 7-0 **Unimplemented:** Read as '0'

**Note 1:** This bit is available on dsPIC33EPXXXMC50X/20X and PIC24EPXXXMC20X devices only.

**NOTES:**

## 13.2 Timer Control Registers

**REGISTER 13-1: TxCON: (TIMER2 AND TIMER4) CONTROL REGISTER**

| R/W-0 | U-0 | R/W-0 | U-0 | U-0 | U-0 | U-0 | U-0 |
|---|---|---|---|---|---|---|---|
| TON | — | TSIDL | — | — | — | — | — |
| bit 15 | | | | | | | bit 8 |

| U-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | U-0 | R/W-0 | U-0 |
|---|---|---|---|---|---|---|---|
| — | TGATE | TCKPS1 | TCKPS0 | T32 | — | TCS | — |
| bit 7 | | | | | | | bit 0 |

| **Legend:** | | | |
|---|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as '0' | |
| -n = Value at POR | '1' = Bit is set | '0' = Bit is cleared | x = Bit is unknown |

bit 15 **TON:** Timerx On bit
When T32 = 1:
1 = Starts 32-bit Timerx/y
0 = Stops 32-bit Timerx/y
When T32 = 0:
1 = Starts 16-bit Timerx
0 = Stops 16-bit Timerx

bit 14 **Unimplemented:** Read as '0'

bit 13 **TSIDL:** Timerx Stop in Idle Mode bit
1 = Discontinues module operation when device enters Idle mode
0 = Continues module operation in Idle mode

bit 12-7 **Unimplemented:** Read as '0'

bit 6 **TGATE:** Timerx Gated Time Accumulation Enable bit
When TCS = 1:
This bit is ignored.
When TCS = 0:
1 = Gated time accumulation is enabled
0 = Gated time accumulation is disabled

bit 5-4 **TCKPS<1:0>:** Timerx Input Clock Prescale Select bits
11 = 1:256
10 = 1:64
01 = 1:8
00 = 1:1

bit 3 **T32:** 32-Bit Timer Mode Select bit
1 = Timerx and Timery form a single 32-bit timer
0 = Timerx and Timery act as two 16-bit timers

bit 2 **Unimplemented:** Read as '0'

bit 1 **TCS:** Timerx Clock Source Select bit
1 = External clock is from pin, TxCK (on the rising edge)
0 = Internal clock (FP)

bit 0 **Unimplemented:** Read as '0'

**REGISTER 16-12: TRGCONx: PWMx TRIGGER CONTROL REGISTER**

| R/W-0 | R/W-0 | R/W-0 | R/W-0 | U-0 | U-0 | U-0 | U-0 |
|---|---|---|---|---|---|---|---|
| TRGDIV<3:0> | | | | — | — | — | — |
| bit 15 | | | | | | | bit 8 |

| U-0 | U-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
|---|---|---|---|---|---|---|---|
| — | — | TRGSTRT<5:0>(1) | | | | | |
| bit 7 | | | | | | | bit 0 |

| **Legend:** | | | |
|---|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as '0' | |
| -n = Value at POR | '1' = Bit is set | '0' = Bit is cleared | x = Bit is unknown |

bit 15-12 **TRGDIV<3:0>:** Trigger # Output Divider bits

1111 = Trigger output for every 16th trigger event
1110 = Trigger output for every 15th trigger event
1101 = Trigger output for every 14th trigger event
1100 = Trigger output for every 13th trigger event
1011 = Trigger output for every 12th trigger event
1010 = Trigger output for every 11th trigger event
1001 = Trigger output for every 10th trigger event
1000 = Trigger output for every 9th trigger event
0111 = Trigger output for every 8th trigger event
0110 = Trigger output for every 7th trigger event
0101 = Trigger output for every 6th trigger event
0100 = Trigger output for every 5th trigger event
0011 = Trigger output for every 4th trigger event
0010 = Trigger output for every 3rd trigger event
0001 = Trigger output for every 2nd trigger event
0000 = Trigger output for every trigger event

bit 11-6 **Unimplemented:** Read as '0'

bit 5-0 **TRGSTRT<5:0>:** Trigger Postscaler Start Enable Select bits(1)

111111 = Waits 63 PWM cycles before generating the first trigger event after the module is enabled
•
•
•
000010 = Waits 2 PWM cycles before generating the first trigger event after the module is enabled
000001 = Waits 1 PWM cycle before generating the first trigger event after the module is enabled
000000 = Waits 0 PWM cycles before generating the first trigger event after the module is enabled

**Note 1:** The secondary PWM generator cannot generate PWMx trigger interrupts.

## 25.3 Op Amp/Comparator Registers

**REGISTER 25-1: CMSTAT: OP AMP/COMPARATOR STATUS REGISTER**

| R/W-0 | U-0 | U-0 | U-0 | R-0 | R-0 | R-0 | R-0 |
|---|---|---|---|---|---|---|---|
| PSIDL | — | — | — | C4EVT(1) | C3EVT(1) | C2EVT(1) | C1EVT(1) |
| bit 15 | | | | | | | bit 8 |

| U-0 | U-0 | U-0 | U-0 | R-0 | R-0 | R-0 | R-0 |
|---|---|---|---|---|---|---|---|
| — | — | — | — | C4OUT(2) | C3OUT(2) | C2OUT(2) | C1OUT(2) |
| bit 7 | | | | | | | bit 0 |

| **Legend:** | | | |
|---|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as '0' | |
| -n = Value at POR | '1' = Bit is set | '0' = Bit is cleared | x = Bit is unknown |

bit 15 **PSIDL:** Comparator Stop in Idle Mode bit
1 = Discontinues operation of all comparators when device enters Idle mode
0 = Continues operation of all comparators in Idle mode

bit 14-12 **Unimplemented:** Read as '0'

bit 11 **C4EVT:** Op Amp/Comparator 4 Event Status bit(1)
1 = Op amp/comparator event occurred
0 = Op amp/comparator event did not occur

bit 10 **C3EVT:** Comparator 3 Event Status bit(1)
1 = Comparator event occurred
0 = Comparator event did not occur

bit 9 **C2EVT:** Comparator 2 Event Status bit(1)
1 = Comparator event occurred
0 = Comparator event did not occur

bit 8 **C1EVT:** Comparator 1 Event Status bit(1)
1 = Comparator event occurred
0 = Comparator event did not occur

bit 7-4 **Unimplemented:** Read as '0'

bit 3 **C4OUT:** Comparator 4 Output Status bit(2)
When CPOL = 0:
1 = VIN+ > VIN-
0 = VIN+ < VIN-
When CPOL = 1:
1 = VIN+ < VIN-
0 = VIN+ > VIN-

bit 2 **C3OUT:** Comparator 3 Output Status bit(2)
When CPOL = 0:
1 = VIN+ > VIN-
0 = VIN+ < VIN-
When CPOL = 1:
1 = VIN+ < VIN-
0 = VIN+ > VIN-

**Note 1:** Reflects the value of the of the CEVT bit in the respective Op Amp/Comparator Control register, CMxCON<9>.

**2:** Reflects the value of the COUT bit in the respective Op Amp/Comparator Control register, CMxCON<8>.

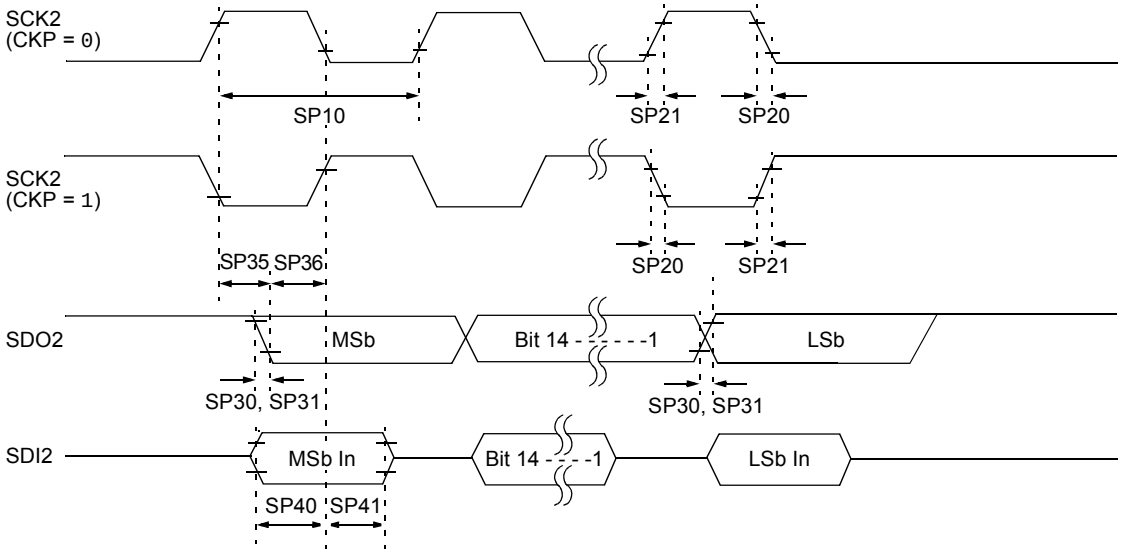
**TABLE 27-2: CONFIGURATION BITS DESCRIPTION (CONTINUED)**

| Bit Field | Description |
|---|---|
| WDTPRE | Watchdog Timer Prescaler bit<br>1 = 1:128<br>0 = 1:32 |
| WDTPOST<3:0> | Watchdog Timer Postscaler bits<br>1111 = 1:32,768<br>1110 = 1:16,384<br>•<br>•<br>•<br>0001 = 1:2<br>0000 = 1:1 |
| WDTWIN<1:0> | Watchdog Window Select bits<br>11 = WDT window is 25% of WDT period<br>10 = WDT window is 37.5% of WDT period<br>01 = WDT window is 50% of WDT period<br>00 = WDT window is 75% of WDT period |
| ALTI2C1 | Alternate I2C1 pin<br>1 = I2C1 is mapped to the SDA1/SCL1 pins<br>0 = I2C1 is mapped to the ASDA1/ASCL1 pins |
| ALTI2C2 | Alternate I2C2 pin<br>1 = I2C2 is mapped to the SDA2/SCL2 pins<br>0 = I2C2 is mapped to the ASDA2/ASCL2 pins |
| JTAGEN(2) | JTAG Enable bit<br>1 = JTAG is enabled<br>0 = JTAG is disabled |
| ICS<1:0> | ICD Communication Channel Select bits<br>11 = Communicate on PGEC1 and PGED1<br>10 = Communicate on PGEC2 and PGED2<br>01 = Communicate on PGEC3 and PGED3<br>00 = Reserved, do not use |

**Note 1:** This bit is only available on dsPIC33EPXXXMC20X/50X and PIC24EPXXXMC20X devices.

**2:** When JTAGEN = 1, an internal pull-up resistor is enabled on the TMS pin. Erased devices default to JTAGEN = 1. Applications requiring I/O pins in a high-impedance state (tri-state) in Reset should use pins other than TMS for this purpose.

**FIGURE 30-17: SPI2 MASTER MODE (FULL-DUPLEX, CKE = 0, CKP = x, SMP = 1) TIMING CHARACTERISTICS**




**Note:** Refer to Figure 30-1 for load conditions.

**TABLE 30-36: SPI2 MASTER MODE (FULL-DUPLEX, CKE = 0, CKP = x, SMP = 1) TIMING REQUIREMENTS**

| AC CHARACTERISTICS | | | Standard Operating Conditions: 3.0V to 3.6V (unless otherwise stated)<br>Operating temperature -40°C ≤ TA ≤ +85°C for Industrial<br>-40°C ≤ TA ≤ +125°C for Extended | | | | |
|---|---|---|---|---|---|---|---|
| **Param.** | **Symbol** | **Characteristic(1)** | **Min.** | **Typ.(2)** | **Max.** | **Units** | **Conditions** |
| SP10 | FscP | Maximum SCK2 Frequency | — | — | 9 | MHz | -40ºC to +125ºC **(Note 3)** |
| SP20 | TscF | SCK2 Output Fall Time | — | — | — | ns | See Parameter DO32 **(Note 4)** |
| SP21 | TscR | SCK2 Output Rise Time | — | — | — | ns | See Parameter DO31 **(Note 4)** |
| SP30 | TdoF | SDO2 Data Output Fall Time | — | — | — | ns | See Parameter DO32 **(Note 4)** |
| SP31 | TdoR | SDO2 Data Output Rise Time | — | — | — | ns | See Parameter DO31 **(Note 4)** |
| SP35 | TscH2doV, TscL2doV | SDO2 Data Output Valid after SCK2 Edge | — | 6 | 20 | ns | |
| SP36 | TdoV2scH, TdoV2scL | SDO2 Data Output Setup to First SCK2 Edge | 30 | — | — | ns | |
| SP40 | TdiV2scH, TdiV2scL | Setup Time of SDI2 Data Input to SCK2 Edge | 30 | — | — | ns | |
| SP41 | TscH2diL, TscL2diL | Hold Time of SDI2 Data Input to SCK2 Edge | 30 | — | — | ns | |

**Note 1:** These parameters are characterized, but are not tested in manufacturing.

**2:** Data in "Typical" column is at 3.3V, +25°C unless otherwise stated.

**3:** The minimum clock period for SCK2 is 111 ns. The clock generated in Master mode must not violate this specification.

**4:** Assumes 50 pF load on all SPI2 pins.

**FIGURE 30-26: SPI1 SLAVE MODE (FULL-DUPLEX, CKE = 1, CKP = 0, SMP = 0) TIMING CHARACTERISTICS**

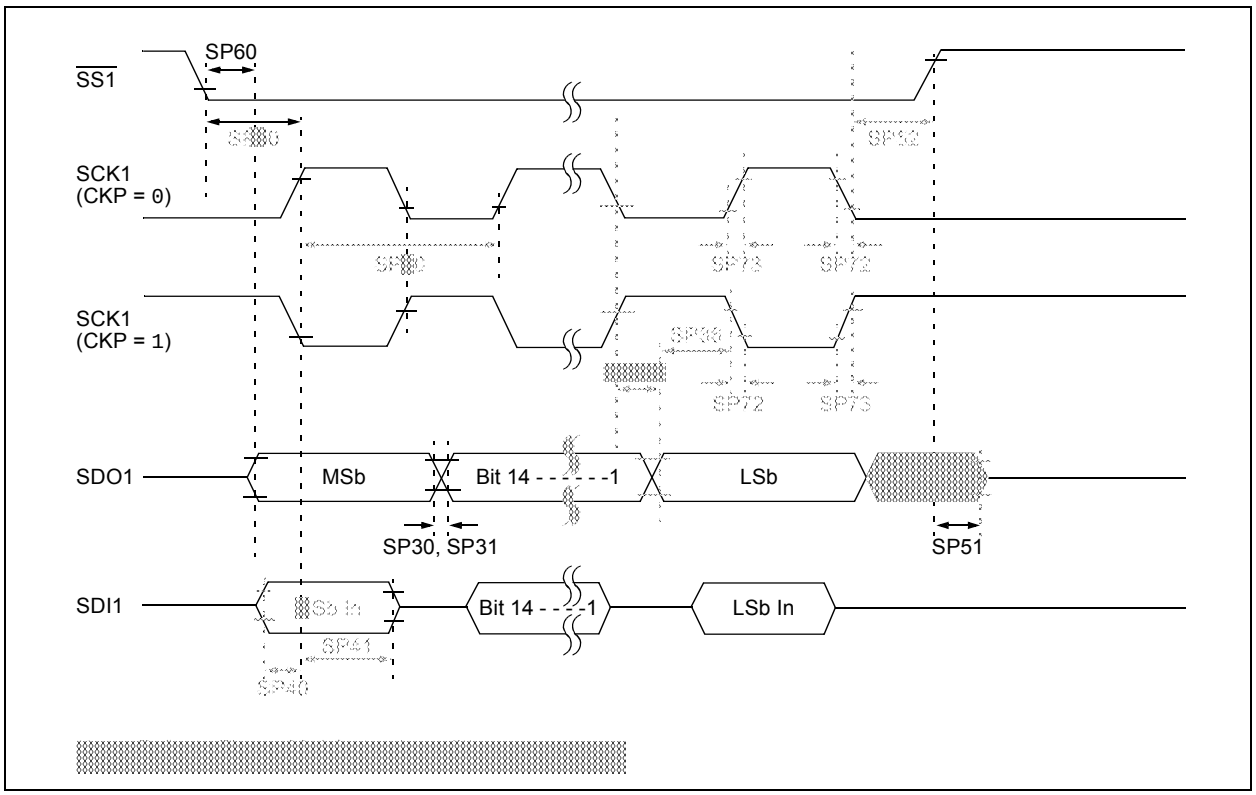


**TABLE 30-49: I2Cx BUS DATA TIMING REQUIREMENTS (MASTER MODE)**

| AC CHARACTERISTICS | | | | Standard Operating Conditions: 3.0V to 3.6V (unless otherwise stated)<br>Operating temperature -40°C ≤ TA ≤ +85°C for Industrial<br>-40°C ≤ TA ≤ +125°C for Extended | | | |
|---|---|---|---|---|---|---|---|
| **Param No.** | **Symbol** | **Characteristic(4)** | | **Min.(1)** | **Max.** | **Units** | **Conditions** |
| IM10 | TLO:SCL | Clock Low Time | 100 kHz mode | TCY/2 (BRG + 2) | — | µs | |
| | | | 400 kHz mode | TCY/2 (BRG + 2) | — | µs | |
| | | | 1 MHz mode(2) | TCY/2 (BRG + 2) | — | µs | |
| IM11 | THI:SCL | Clock High Time | 100 kHz mode | TCY/2 (BRG + 2) | — | µs | |
| | | | 400 kHz mode | TCY/2 (BRG + 2) | — | µs | |
| | | | 1 MHz mode(2) | TCY/2 (BRG + 2) | — | µs | |
| IM20 | TF:SCL | SDAx and SCLx Fall Time | 100 kHz mode | — | 300 | ns | CB is specified to be from 10 to 400 pF |
| | | | 400 kHz mode | 20 + 0.1 CB | 300 | ns | |
| | | | 1 MHz mode(2) | — | 100 | ns | |
| IM21 | TR:SCL | SDAx and SCLx Rise Time | 100 kHz mode | — | 1000 | ns | CB is specified to be from 10 to 400 pF |
| | | | 400 kHz mode | 20 + 0.1 CB | 300 | ns | |
| | | | 1 MHz mode(2) | — | 300 | ns | |
| IM25 | TSU:DAT | Data Input Setup Time | 100 kHz mode | 250 | — | ns | |
| | | | 400 kHz mode | 100 | — | ns | |
| | | | 1 MHz mode(2) | 40 | — | ns | |
| IM26 | THD:DAT | Data Input Hold Time | 100 kHz mode | 0 | — | µs | |
| | | | 400 kHz mode | 0 | 0.9 | µs | |
| | | | 1 MHz mode(2) | 0.2 | — | µs | |
| IM30 | TSU:STA | Start Condition Setup Time | 100 kHz mode | TCY/2 (BRG + 2) | — | µs | Only relevant for Repeated Start condition |
| | | | 400 kHz mode | TCY/2 (BRG + 2) | — | µs | |
| | | | 1 MHz mode(2) | TCY/2 (BRG + 2) | — | µs | |
| IM31 | THD:STA | Start Condition Hold Time | 100 kHz mode | TCY/2 (BRG + 2) | — | µs | After this period, the first clock pulse is generated |
| | | | 400 kHz mode | TCY/2 (BRG +2) | — | µs | |
| | | | 1 MHz mode(2) | TCY/2 (BRG + 2) | — | µs | |
| IM33 | TSU:STO | Stop Condition Setup Time | 100 kHz mode | TCY/2 (BRG + 2) | — | µs | |
| | | | 400 kHz mode | TCY/2 (BRG + 2) | — | µs | |
| | | | 1 MHz mode(2) | TCY/2 (BRG + 2) | — | µs | |
| IM34 | THD:STO | Stop Condition Hold Time | 100 kHz mode | TCY/2 (BRG + 2) | — | µs | |
| | | | 400 kHz mode | TCY/2 (BRG + 2) | — | µs | |
| | | | 1 MHz mode(2) | TCY/2 (BRG + 2) | — | µs | |
| IM40 | TAA:SCL | Output Valid From Clock | 100 kHz mode | — | 3500 | ns | |
| | | | 400 kHz mode | — | 1000 | ns | |
| | | | 1 MHz mode(2) | — | 400 | ns | |
| IM45 | TBF:SDA | Bus Free Time | 100 kHz mode | 4.7 | — | µs | Time the bus must be free before a new transmission can start |
| | | | 400 kHz mode | 1.3 | — | µs | |
| | | | 1 MHz mode(2) | 0.5 | — | µs | |
| IM50 | CB | Bus Capacitive Loading | | — | 400 | pF | |
| IM51 | TPGD | Pulse Gobbler Delay | | 65 | 390 | ns | **(Note 3)** |

**Note 1:** BRG is the value of the $I^2C$™ Baud Rate Generator. Refer to **"Inter-Integrated Circuit ($I^2C$™)"** (DS70330) in the "*dsPIC33/PIC24 Family Reference Manual*". Please see the Microchip web site for the latest family reference manual sections.

**2:** Maximum pin capacitance = 10 pF for all I2Cx pins (for 1 MHz mode only).

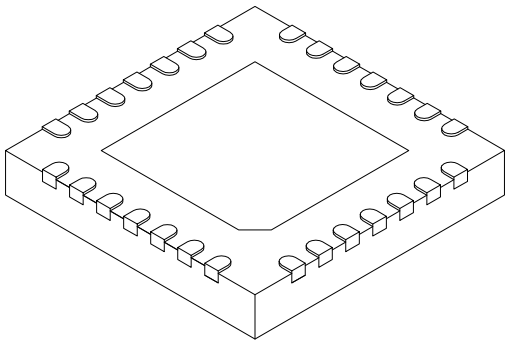
**3:** Typical value for this parameter is 130 ns.

**4:** These parameters are characterized, but not tested in manufacturing.

**NOTES:**

## 28-Lead Plastic Quad Flat, No Lead Package (MM) - 6x6x0.9mm Body [QFN-S] With 0.40 mm Terminal Length

**Note:** For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



| Units | | MILLIMETERS | | |
|---|---|---|---|---|
| Dimension Limits | | MIN | NOM | MAX |
| Number of Pins | N | | 28 | |
| Pitch | e | | 0.65 BSC | |
| Overall Height | A | 0.80 | 0.90 | 1.00 |
| Standoff | A1 | 0.00 | 0.02 | 0.05 |
| Terminal Thickness | A3 | | 0.20 REF | |
| Overall Width | E | | 6.00 BSC | |
| Exposed Pad Width | E2 | 3.65 | 3.70 | 4.70 |
| Overall Length | D | | 6.00 BSC | |
| Exposed Pad Length | D2 | 3.65 | 3.70 | 4.70 |
| Terminal Width | b | 0.23 | 0.30 | 0.35 |
| Terminal Length | L | 0.30 | 0.40 | 0.50 |
| Terminal-to-Exposed Pad | K | 0.20 | - | - |

Notes:

1. Pin 1 visual index feature may vary, but must be located within the hatched area.
2. Package is saw singulated
3. Dimensioning and tolerancing per ASME Y14.5M

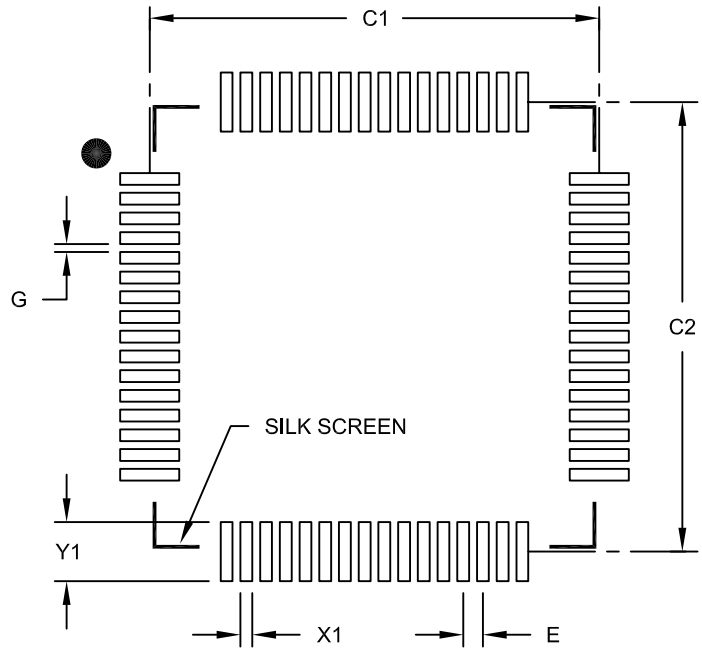
BSC: Basic Dimension. Theoretically exact value shown without tolerances.

REF: Reference Dimension, usually without tolerance, for information purposes only.

Microchip Technology Drawing C04-124C Sheet 2 of 2

64-Lead Plastic Thin Quad Flatpack (PT) 10x10x1 mm Body, 2.00 mm Footprint [TQFP]

**Note:** For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging




RECOMMENDED LAND PATTERN

| Units | | MILLIMETERS | | |
|---|---|---|---|---|
| Dimension Limits | | MIN | NOM | MAX |
| Contact Pitch | E | | 0.50 BSC | |
| Contact Pad Spacing | C1 | | 11.40 | |
| Contact Pad Spacing | C2 | | 11.40 | |
| Contact Pad Width (X64) | X1 | | | 0.30 |
| Contact Pad Length (X64) | Y1 | | | 1.50 |
| Distance Between Pads | G | 0.20 | | |

Notes:

1. Dimensioning and tolerancing per ASME Y14.5M

BSC: Basic Dimension. Theoretically exact value shown without tolerances.

Microchip Technology Drawing No. C04-2085B

**TABLE A-1: MAJOR SECTION UPDATES (CONTINUED)**

| Section Name | Update Description |
|---|---|
| **Section 30.0 "Electrical Characteristics"** | Removed Voltage on VCAP with respect to Vss and added Note 5 in Absolute Maximum Ratings(1).<br><br>Removed Parameter DC18 (VCORE) and Note 3 from the DC Temperature and Voltage Specifications (see Table 30-4).<br><br>Updated Note 1 in the DC Characteristics: Operating Current (IDD) (see Table 30-6).<br><br>Updated Note 1 in the DC Characteristics: Idle Current (IIDLE) (see Table 30-7).<br><br>Changed the Typical values for Parameters DC60a-DC60d and updated Note 1 in the DC Characteristics: Power-down Current (IPD) (see Table 30-8).<br><br>Updated Note 1 in the DC Characteristics: Doze Current (IDOZE) (see Table 30-9).<br><br>Updated Note 2 in the Electrical Characteristics: BOR (see Table 30-12).<br><br>Updated Parameters CM20 and CM31, and added Parameters CM44 and CM45 in the AC/DC Characteristics: Op amp/Comparator (see Table 30-14).<br><br>Added the Op amp/Comparator Reference Voltage Settling Time Specifications (see Table 30-15).<br><br>Added Op amp/Comparator Voltage Reference DC Specifications (see Table 30-16).<br><br>Updated Internal FRC Accuracy Parameter F20a (see Table 30-21).<br><br>Updated the Typical value and Units for Parameter CTMUI1, and added Parameters CTMUI4, CTMUFV1, and CTMUFV2 to the CTMU Current Source Specifications (see Table 30-55). |
| **Section 31.0 "Packaging Information"** | Updated packages by replacing references of VLAP with TLA. |
| **"Product Identification System"** | Changed VLAP to TLA. |

**NOTES:**