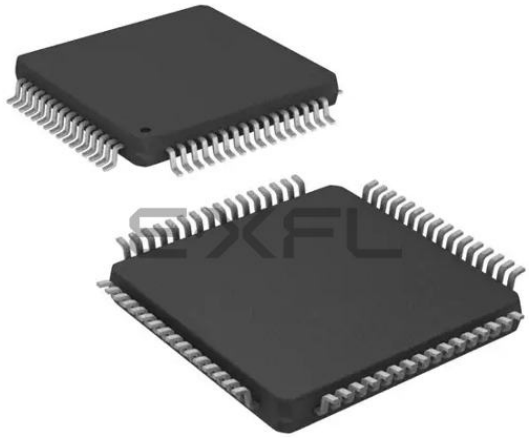
Microchip Technology - PIC24EP128MC206T-E/PT Datasheet



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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	PIC
Core Size	16-Bit
Speed	60 MIPs
Connectivity	I²C, IrDA, LINbus, QEI, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, DMA, Motor Control PWM, POR, PWM, WDT
Number of I/O	53
Program Memory Size	128KB (43K x 24)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	8K x 16
Voltage - Supply (Vcc/Vdd)	3V ~ 3.6V
Data Converters	A/D 16x10b/12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 125°C (TA)
Mounting Type	Surface Mount
Package / Case	64-TQFP
Supplier Device Package	64-TQFP (10x10)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/pic24ep128mc206t-e-pt

2.0 GUIDELINES FOR GETTING STARTED WITH 16-BIT DIGITAL SIGNAL CONTROLLERS AND MICROCONTROLLERS

Note 1: This data sheet summarizes the features of the dsPIC33EPXXXGP50X, dsPIC33EPXXXMC20X/50X and PIC24EPXXXGP/MC20X families of devices. It is not intended to be a comprehensive reference source. To complement the information in this data sheet, refer to the related section of the "*dsPIC33/PIC24 Family Reference Manual*", which is available from the Microchip web site (www.microchip.com)

2: Some registers and associated bits described in this section may not be available on all devices. Refer to **Section 4.0 "Memory Organization"** in this data sheet for device-specific register and bit information.

2.1 Basic Connection Requirements

Getting started with the dsPIC33EPXXXGP50X, dsPIC33EPXXXMC20X/50X and PIC24EPXXXGP/MC20X families requires attention to a minimal set of device pin connections before proceeding with development. The following is a list of pin names, which must always be connected:

- All VDD and VSS pins
  (see **Section 2.2 "Decoupling Capacitors"**)
- All AVDD and AVSS pins (regardless if ADC module is not used)
  (see **Section 2.2 "Decoupling Capacitors"**)
- VCAP
  (see **Section 2.3 "CPU Logic Filter Capacitor Connection (VCAP)"**)
- $\overline{\text{MCLR}}$ pin
  (see **Section 2.4 "Master Clear (MCLR) Pin"**)
- PGECx/PGEDx pins used for In-Circuit Serial Programming™ (ICSP™) and debugging purposes
  (see **Section 2.5 "ICSP Pins"**)
- OSC1 and OSC2 pins when external oscillator source is used
  (see **Section 2.6 "External Oscillator Pins"**)

Additionally, the following pins may be required:

- VREF+/VREF- pins are used when external voltage reference for the ADC module is implemented

Note: The AVDD and AVSS pins must be connected, independent of the ADC voltage reference source.

2.2 Decoupling Capacitors

The use of decoupling capacitors on every pair of power supply pins, such as VDD, VSS, AVDD and AVSS is required.

Consider the following criteria when using decoupling capacitors:

- **Value and type of capacitor:** Recommendation of 0.1 µF (100 nF), 10-20V. This capacitor should be a low-ESR and have resonance frequency in the range of 20 MHz and higher. It is recommended to use ceramic capacitors.
- **Placement on the printed circuit board:** The decoupling capacitors should be placed as close to the pins as possible. It is recommended to place the capacitors on the same side of the board as the device. If space is constricted, the capacitor can be placed on another layer on the PCB using a via; however, ensure that the trace length from the pin to the capacitor is within one-quarter inch (6 mm) in length.
- **Handling high-frequency noise:** If the board is experiencing high-frequency noise, above tens of MHz, add a second ceramic-type capacitor in parallel to the above described decoupling capacitor. The value of the second capacitor can be in the range of 0.01 µF to 0.001 µF. Place this second capacitor next to the primary decoupling capacitor. In high-speed circuit designs, consider implementing a decade pair of capacitances as close to the power and ground pins as possible. For example, 0.1 µF in parallel with 0.001 µF.
- **Maximizing performance:** On the board layout from the power supply circuit, run the power and return traces to the decoupling capacitors first, and then to the device pins. This ensures that the decoupling capacitors are first in the power chain. Equally important is to keep the trace length between the capacitor and the power pins to a minimum, thereby reducing PCB track inductance.

TABLE 4-4: INTERRUPT CONTROLLER REGISTER MAP FOR PIC24EPXXXMC20X DEVICES ONLY

File Name	Addr.	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	All Resets
IFS0	0800	—	DMA1IF	AD1IF	U1TXIF	U1RXIF	SPI1IF	SPI1EIF	T3IF	T2IF	OC2IF	IC2IF	DMA0IF	T1IF	OC1IF	IC1IF	INT0IF	0000
IFS1	0802	U2TXIF	U2RXIF	INT2IF	T5IF	T4IF	OC4IF	OC3IF	DMA2IF	—	—	—	INT1IF	CNIF	CMIF	MI2C1IF	SI2C1IF	0000
IFS2	0804	—	—	—	—	—	—	—	—	—	IC4IF	IC3IF	DMA3IF	—	—	SPI2IF	SPI2EIF	0000
IFS3	0806	—	—	—	—	—	QEI1IF	PSEMIF	—	—	—	—	—	—	MI2C2IF	SI2C2IF	—	0000
IFS4	0808	—	—	CTMUIF	—	—	—	—	—	—	—	—	—	CRCIF	U2EIF	U1EIF	—	0000
IFS5	080A	PWM2IF	PWM1IF	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
IFS6	080C	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	PWM3IF	0000
IFS8	0810	JTAGIF	ICDIF	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
IFS9	0812	—	—	—	—	—	—	—	—	—	PTG3IF	PTG2IF	PTG1IF	PTG0IF	PTGWDTIF	PTGSTEPIF	—	0000
IEC0	0820	—	DMA1IE	AD1IE	U1TXIE	U1RXIE	SPI1IE	SPI1EIE	T3IE	T2IE	OC2IE	IC2IE	DMA0IE	T1IE	OC1IE	IC1IE	INT0IE	0000
IEC1	0822	U2TXIE	U2RXIE	INT2IE	T5IE	T4IE	OC4IE	OC3IE	DMA2IE	—	—	—	INT1IE	CNIE	CMIE	MI2C1IE	SI2C1IE	0000
IEC2	0824	—	—	—	—	—	—	—	—	—	IC4IE	IC3IE	DMA3IE	—	—	SPI2IE	SPI2EIE	0000
IEC3	0826	—	—	—	—	—	QEI1IE	PSEMIE	—	—	—	—	—	—	MI2C2IE	SI2C2IE	—	0000
IEC4	0828	—	—	CTMUIE	—	—	—	—	—	—	—	—	—	CRCIE	U2EIE	U1EIE	—	0000
IEC5	082A	PWM2IE	PWM1IE	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
IEC6	082C	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	PWM3IE	0000
IEC8	0830	JTAGIE	ICDIE	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
IEC9	0832	—	—	—	—	—	—	—	—	—	PTG3IE	PTG2IE	PTG1IE	PTG0IE	PTGWDTIE	PTGSTEPIE	—	0000
IPC0	0840	—	T1IP<2:0>			—	OC1IP<2:0>			—	IC1IP<2:0>			—	INT0IP<2:0>			4444
IPC1	0842	—	T2IP<2:0>			—	OC2IP<2:0>			—	IC2IP<2:0>			—	DMA0IP<2:0>			4444
IPC2	0844	—	U1RXIP<2:0>			—	SPI1IP<2:0>			—	SPI1EIP<2:0>			—	T3IP<2:0>			4444
IPC3	0846	—	—	—	—	—	DMA1IP<2:0>			—	AD1IP<2:0>			—	U1TXIP<2:0>			0444
IPC4	0848	—	CNIP<2:0>			—	CMIP<2:0>			—	MI2C1IP<2:0>			—	SI2C1IP<2:0>			4444
IPC5	084A	—	—	—	—	—	—	—	—	—	—	—	—	—	INT1IP<2:0>			0004
IPC6	084C	—	T4IP<2:0>			—	OC4IP<2:0>			—	OC3IP<2:0>			—	DMA2IP<2:0>			4444
IPC7	084E	—	U2TXIP<2:0>			—	U2RXIP<2:0>			—	INT2IP<2:0>			—	T5IP<2:0>			4444
IPC8	0850	—	—	—	—	—	—	—	—	—	SPI2IP<2:0>			—	SPI2EIP<2:0>			0044
IPC9	0852	—	—	—	—	—	IC4IP<2:0>			—	IC3IP<2:0>			—	DMA3IP<2:0>			0444
IPC12	0858	—	—	—	—	—	MI2C2IP<2:0>			—	SI2C2IP<2:0>			—	—	—	—	0440
IPC14	085C	—	—	—	—	—	QEI1IP<2:0>			—	PSEMIP<2:0>			—	—	—	—	0440
IPC16	0860	—	CRCIP<2:0>			—	U2EIP<2:0>			—	U1EIP<2:0>			—	—	—	—	4440
IPC19	0866	—	—	—	—	—	—	—	—	—	CTMUIP<2:0>			—	—	—	—	0040
IPC23	086E	—	PWM2IP<2:0>			—	PWM1IP<2:0>			—	—	—	—	—	—	—	—	4400
IPC24	0870	—	—	—	—	—	—	—	—	—	—	—	—	—	PWM3IP<2:0>			4004

Legend: — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

TABLE 4-5: INTERRUPT CONTROLLER REGISTER MAP FOR dsPIC33EPXXXGP50X DEVICES ONLY (CONTINUED)

File Name	Addr.	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	All Resets
INTCON1	08C0	NSTDIS	OVAERR	OVBERR	COVAERR	COVBERR	OVATE	OVBTE	COVTE	SFTACERR	DIV0ERR	DMACERR	MATHERR	ADDRERR	STKERR	OSCFAIL	—	0000
INTCON2	08C2	GIE	DISI	SWTRAP	—	—	—	—	—	—	—	—	—	—	INT2EP	INT1EP	INT0EP	8000
INTCON3	08C4	—	—	—	—	—	—	—	—	—	—	DAE	DOOVR	—	—	—	—	0000
INTCON4	08C6	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	SGHT	0000
INTTREG	08C8	—	—	—	—	ILR<3:0>				VECNUM<7:0>								0000

Legend: — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

REGISTER 6-1: RCON: RESET CONTROL REGISTER(1) (CONTINUED)

bit 3 **SLEEP:** Wake-up from Sleep Flag bit
1 = Device has been in Sleep mode
0 = Device has not been in Sleep mode

bit 2 **IDLE:** Wake-up from Idle Flag bit
1 = Device was in Idle mode
0 = Device was not in Idle mode

bit 1 **BOR:** Brown-out Reset Flag bit
1 = A Brown-out Reset has occurred
0 = A Brown-out Reset has not occurred

bit 0 **POR:** Power-on Reset Flag bit
1 = A Power-on Reset has occurred
0 = A Power-on Reset has not occurred

Note 1: All of the Reset status bits can be set or cleared in software. Setting one of these bits in software does not cause a device Reset.

2: If the FWDTEN Configuration bit is '1' (unprogrammed), the WDT is always enabled, regardless of the SWDTEN bit setting.

REGISTER 8-13: DMALCA: DMA LAST CHANNEL ACTIVE STATUS REGISTER

U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
—	—	—	—	—	—	—	—
bit 15							bit 8

U-0	U-0	U-0	U-0	R-1	R-1	R-1	R-1
—	—	—	—	LSTCH<3:0>			
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 15-4 **Unimplemented:** Read as ‘0’

bit 3-0 **LSTCH<3:0>:** Last DMAC Channel Active Status bits

1111 = No DMA transfer has occurred since system Reset
1110 = Reserved
•
•
•
0100 = Reserved
0011 = Last data transfer was handled by Channel 3
0010 = Last data transfer was handled by Channel 2
0001 = Last data transfer was handled by Channel 1
0000 = Last data transfer was handled by Channel 0

16.1.2 WRITE-PROTECTED REGISTERS

On dsPIC33EPXXXMC20X/50X and PIC24EPXXXMC20X devices, write protection is implemented for the IOCONx and FCLCONx registers. The write protection feature prevents any inadvertent writes to these registers. This protection feature can be controlled by the PWMLOCK Configuration bit (FOSCSEL<6>). The default state of the write protection feature is enabled (PWMLOCK = 1). The write protection feature can be disabled by configuring, PWMLOCK = 0.

To gain write access to these locked registers, the user application must write two consecutive values of (0xABCD and 0x4321) to the PWMKEY register to perform the unlock operation. The write access to the IOCONx or FCLCONx registers must be the next SFR access following the unlock process. There can be no other SFR accesses during the unlock process and subsequent write access. To write to both the IOCONx and FCLCONx registers requires two unlock operations.

The correct unlocking sequence is described in Example 16-1.

EXAMPLE 16-1: PWMx WRITE-PROTECTED REGISTER UNLOCK SEQUENCE

```
; FLT32 pin must be pulled low externally in order to clear and disable the fault
; Writing to FCLCON1 register requires unlock sequence

mov #0xabcd,w10       ; Load first unlock key to w10 register
mov #0x4321,w11       ; Load second unlock key to w11 register
mov #0x0000,w0        ; Load desired value of FCLCON1 register in w0
mov w10, PWMKEY       ; Write first unlock key to PWMKEY register
mov w11, PWMKEY       ; Write second unlock key to PWMKEY register
mov w0,FCLCON1        ; Write desired value to FCLCON1 register

; Set PWM ownership and polarity using the IOCON1 register
; Writing to IOCON1 register requires unlock sequence

mov #0xabcd,w10       ; Load first unlock key to w10 register
mov #0x4321,w11       ; Load second unlock key to w11 register
mov #0xF000,w0        ; Load desired value of IOCON1 register in w0
mov w10, PWMKEY       ; Write first unlock key to PWMKEY register
mov w11, PWMKEY       ; Write second unlock key to PWMKEY register
mov w0,IOCON1         ; Write desired value to IOCON1 register
```

21.2 Modes of Operation

The ECAN module can operate in one of several operation modes selected by the user. These modes include:

- Initialization mode
- Disable mode
- Normal Operation mode
- Listen Only mode
- Listen All Messages mode
- Loopback mode

Modes are requested by setting the REQOP<2:0> bits (CxCTRL1<10:8>). Entry into a mode is Acknowledged by monitoring the OPMODE<2:0> bits (CxCTRL1<7:5>). The module does not change the mode and the OPMODEx bits until a change in mode is acceptable, generally during bus Idle time, which is defined as at least 11 consecutive recessive bits.

21.3 ECAN Resources

Many useful resources are provided on the main product page of the Microchip web site for the devices listed in this data sheet. This product page, which can be accessed using this link, contains the latest updates and additional information.

Note:	In the event you are not able to access the product page using the link above, enter this URL in your browser: http://www.microchip.com/wwwproducts/Devices.aspx?dDocName=en555464

21.3.1 KEY RESOURCES

- **"Enhanced Controller Area Network (ECAN™)"** (DS70353) in the *"dsPIC33/PIC24 Family Reference Manual"*
- Code Samples
- Application Notes
- Software Libraries
- Webinars
- All Related *"dsPIC33/PIC24 Family Reference Manual"* Sections
- Development Tools

REGISTER 21-2: CxCTRL2: ECANx CONTROL REGISTER 2

U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
—	—	—	—	—	—	—	—
bit 15							bit 8

U-0	U-0	U-0	R-0	R-0	R-0	R-0	R-0
—	—	—	DNCNT4	DNCNT3	DNCNT2	DNCNT1	DNCNT0
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 15-5 **Unimplemented:** Read as ‘0’

bit 4-0 **DNCNT<4:0>:** DeviceNet™ Filter Bit Number bits

10010-11111 = Invalid selection
10001 = Compares up to Data Byte 3, bit 6 with EID<17>
•
•
•
00001 = Compares up to Data Byte 1, bit 7 with EID<0>
00000 = Does not compare data bytes

REGISTER 21-4: CxFCTRL: ECANx FIFO CONTROL REGISTER

R/W-0	R/W-0	R/W-0	U-0	U-0	U-0	U-0	U-0
DMABS2	DMABS1	DMABS0	—	—	—	—	—
bit 15							bit 8

U-0	U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
—	—	—	FSA4	FSA3	FSA2	FSA1	FSA0
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 15-13 **DMABS<2:0>:** DMA Buffer Size bits
111 = Reserved
110 = 32 buffers in RAM
101 = 24 buffers in RAM
100 = 16 buffers in RAM
011 = 12 buffers in RAM
010 = 8 buffers in RAM
001 = 6 buffers in RAM
000 = 4 buffers in RAM

bit 12-5 **Unimplemented:** Read as ‘0’

bit 4-0 **FSA<4:0>:** FIFO Area Starts with Buffer bits
11111 = Read Buffer RB31
11110 = Read Buffer RB30
•
•
•
00001 = TX/RX Buffer TRB1
00000 = TX/RX Buffer TRB0

REGISTER 21-10: CxCFG2: ECANx BAUD RATE CONFIGURATION REGISTER 2

U-0	R/W-x	U-0	U-0	U-0	R/W-x	R/W-x	R/W-x
—	WAKFIL	—	—	—	SEG2PH2	SEG2PH1	SEG2PH0
bit 15							bit 8

R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x
SEG2PHTS	SAM	SEG1PH2	SEG1PH1	SEG1PH0	PRSEG2	PRSEG1	PRSEG0
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15 **Unimplemented:** Read as '0'

bit 14 **WAKFIL:** Select CAN Bus Line Filter for Wake-up bit
1 = Uses CAN bus line filter for wake-up
0 = CAN bus line filter is not used for wake-up

bit 13-11 **Unimplemented:** Read as '0'

bit 10-8 **SEG2PH<2:0>:** Phase Segment 2 bits
111 = Length is 8 x TQ
•
•
•
000 = Length is 1 x TQ

bit 7 **SEG2PHTS:** Phase Segment 2 Time Select bit
1 = Freely programmable
0 = Maximum of SEG1PHx bits or Information Processing Time (IPT), whichever is greater

bit 6 **SAM:** Sample of the CAN Bus Line bit
1 = Bus line is sampled three times at the sample point
0 = Bus line is sampled once at the sample point

bit 5-3 **SEG1PH<2:0>:** Phase Segment 1 bits
111 = Length is 8 x TQ
•
•
•
000 = Length is 1 x TQ

bit 2-0 **PRSEG<2:0>:** Propagation Time Segment bits
111 = Length is 8 x TQ
•
•
•
000 = Length is 1 x TQ

BUFFER 21-5: ECAN™ MESSAGE BUFFER WORD 4

R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x
Byte 3							
bit 15							bit 8

R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x
Byte 2							
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15-8 **Byte 3<15:8>:** ECAN Message Byte 3 bits

bit 7-0 **Byte 2<7:0>:** ECAN Message Byte 2 bits

BUFFER 21-6: ECAN™ MESSAGE BUFFER WORD 5

R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x
Byte 5							
bit 15							bit 8

R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x
Byte 4							
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15-8 **Byte 5<15:8>:** ECAN Message Byte 5 bits

bit 7-0 **Byte 4<7:0>:** ECAN Message Byte 4 bits

TABLE 24-2: PTG OUTPUT DESCRIPTIONS

PTG Output Number	PTG Output Description
PTGO0	Trigger/Synchronization Source for OC1
PTGO1	Trigger/Synchronization Source for OC2
PTGO2	Trigger/Synchronization Source for OC3
PTGO3	Trigger/Synchronization Source for OC4
PTGO4	Clock Source for OC1
PTGO5	Clock Source for OC2
PTGO6	Clock Source for OC3
PTGO7	Clock Source for OC4
PTGO8	Trigger/Synchronization Source for IC1
PTGO9	Trigger/Synchronization Source for IC2
PTGO10	Trigger/Synchronization Source for IC3
PTGO11	Trigger/Synchronization Source for IC4
PTGO12	Sample Trigger for ADC
PTGO13	Sample Trigger for ADC
PTGO14	Sample Trigger for ADC
PTGO15	Sample Trigger for ADC
PTGO16	PWM Time Base Synchronous Source for PWM(1)
PTGO17	PWM Time Base Synchronous Source for PWM(1)
PTGO18	Mask Input Select for Op Amp/Comparator
PTGO19	Mask Input Select for Op Amp/Comparator
PTGO20	Reserved
PTGO21	Reserved
PTGO22	Reserved
PTGO23	Reserved
PTGO24	Reserved
PTGO25	Reserved
PTGO26	Reserved
PTGO27	Reserved
PTGO28	Reserved
PTGO29	Reserved
PTGO30	PTG Output to PPS Input Selection
PTGO31	PTG Output to PPS Input Selection

Note 1: This feature is only available on dsPIC33EPXXXMC20X/50X and PIC24EPXXXMC20X devices.

REGISTER 25-7: CVRCON: COMPARATOR VOLTAGE REFERENCE CONTROL REGISTER

U-0	R/W-0	U-0	U-0	U-0	R/W-0	U-0	U-0
—	CVR2OE(1)	—	—	—	VREFSEL	—	—
bit 15							bit 8

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
CVREN	CVR1OE(1)	CVRR	CVRSS(2)	CVR3	CVR2	CVR1	CVR0
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15 **Unimplemented:** Read as '0'

bit 14 **CVR2OE:** Comparator Voltage Reference 2 Output Enable bit(1)
1 = (AVDD – AVSS)/2 is connected to the CVREF2O pin
0 = (AVDD – AVSS)/2 is disconnected from the CVREF2O pin

bit 13-11 **Unimplemented:** Read as '0'

bit 10 **VREFSEL:** Comparator Voltage Reference Select bit
1 = CVREFIN = VREF+
0 = CVREFIN is generated by the resistor network

bit 9-8 **Unimplemented:** Read as '0'

bit 7 **CVREN:** Comparator Voltage Reference Enable bit
1 = Comparator voltage reference circuit is powered on
0 = Comparator voltage reference circuit is powered down

bit 6 **CVR1OE:** Comparator Voltage Reference 1 Output Enable bit(1)
1 = Voltage level is output on the CVREF1O pin
0 = Voltage level is disconnected from then CVREF1O pin

bit 5 **CVRR:** Comparator Voltage Reference Range Selection bit
1 = CVRSRC/24 step-size
0 = CVRSRC/32 step-size

bit 4 **CVRSS:** Comparator Voltage Reference Source Selection bit(2)
1 = Comparator voltage reference source, CVRSRC = (VREF+) – (AVSS)
0 = Comparator voltage reference source, CVRSRC = AVDD – AVSS

bit 3-0 **CVR<3:0>** Comparator Voltage Reference Value Selection 0 ≤ CVR<3:0> ≤ 15 bits
When CVRR = 1:
CVREFIN = (CVR<3:0>/24) • (CVRSRC)
When CVRR = 0:
CVREFIN = (CVRSRC/4) + (CVR<3:0>/32) • (CVRSRC)

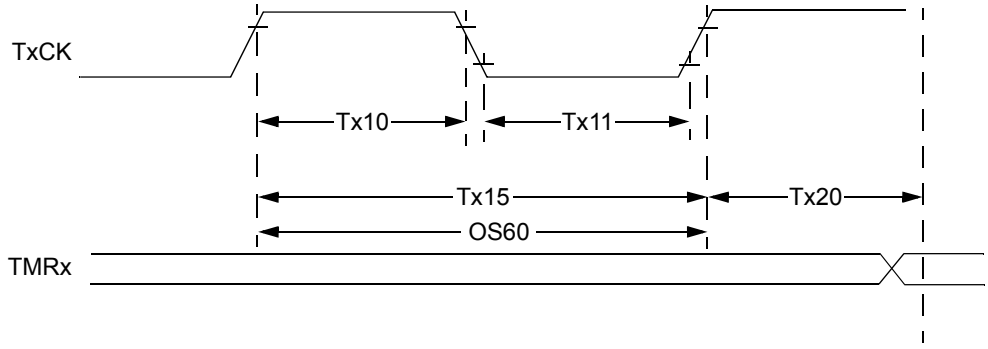
Note 1: CVRxOE overrides the TRISx and the ANSELx bit settings.
2: In order to operate with CVRSS = 1, at least one of the comparator modules must be enabled.

TABLE 28-2: INSTRUCTION SET OVERVIEW (CONTINUED)

Base Instr #	Assembly Mnemonic	Assembly Syntax	Description	# of Words	# of Cycles(2)	Status Flags Affected
46	MOV	MOV f,Wn	Move f to Wn	1	1	None
		MOV f	Move f to f	1	1	None
		MOV f,WREG	Move f to WREG	1	1	None
		MOV #lit16,Wn	Move 16-bit literal to Wn	1	1	None
		MOV.b #lit8,Wn	Move 8-bit literal to Wn	1	1	None
		MOV Wn,f	Move Wn to f	1	1	None
		MOV Wso,Wdo	Move Ws to Wd	1	1	None
		MOV WREG,f	Move WREG to f	1	1	None
		MOV.D Wns,Wd	Move Double from W(ns):W(ns + 1) to Wd	1	2	None
		MOV.D Ws,Wnd	Move Double from Ws to W(nd + 1):W(nd)	1	2	None
47	MOVPAG	MOVPAG #lit10,DSRPAG	Move 10-bit literal to DSRPAG	1	1	None
		MOVPAG #lit9,DSWPAG	Move 9-bit literal to DSWPAG	1	1	None
		MOVPAG #lit8,TBLPAG	Move 8-bit literal to TBLPAG	1	1	None
		MOVPAG Ws, DSRPAG	Move Ws<9:0> to DSRPAG	1	1	None
		MOVPAG Ws, DSWPAG	Move Ws<8:0> to DSWPAG	1	1	None
		MOVPAG Ws, TBLPAG	Move Ws<7:0> to TBLPAG	1	1	None
48	MOVSAC	MOVSAC Acc,Wx,Wxd,Wy,Wyd,AWB(1)	Prefetch and store accumulator	1	1	None
49	MPY	MPY Wm*Wn,Acc,Wx,Wxd,Wy,Wyd(1)	Multiply Wm by Wn to Accumulator	1	1	OA,OB,OAB, SA,SB,SAB
		MPY Wm*Wm,Acc,Wx,Wxd,Wy,Wyd(1)	Square Wm to Accumulator	1	1	OA,OB,OAB, SA,SB,SAB
50	MPY.N	MPY.N Wm*Wn,Acc,Wx,Wxd,Wy,Wyd(1)	-(Multiply Wm by Wn) to Accumulator	1	1	None
51	MSC	MSC Wm*Wm,Acc,Wx,Wxd,Wy,Wyd,AWB(1)	Multiply and Subtract from Accumulator	1	1	OA,OB,OAB, SA,SB,SAB

Note 1: These instructions are available in dsPIC33EPXXXMC20X/50X and PIC24EPXXXMC20X devices only.
2: Read and Read-Modify-Write (e.g., bit operations and logical operations) on non-CPU SFRs incur an additional instruction cycle.

FIGURE 30-5: TIMER1-TIMER5 EXTERNAL CLOCK TIMING CHARACTERISTICS



Note: Refer to Figure 30-1 for load conditions.

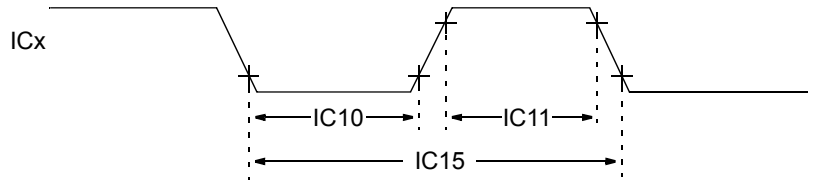
TABLE 30-23: TIMER1 EXTERNAL CLOCK TIMING REQUIREMENTS(1)

AC CHARACTERISTICS				Standard Operating Conditions: 3.0V to 3.6V (unless otherwise stated) Operating temperature -40°C ≤ TA ≤ +85°C for Industrial -40°C ≤ TA ≤ +125°C for Extended				
Param No.	**Symbol**	**Characteristic(2)**		**Min.**	**Typ.**	**Max.**	**Units**	**Conditions**
TA10	TTXH	T1CK High Time	Synchronous mode	Greater of: 20 or (TCY + 20)/N	—	—	ns	Must also meet Parameter TA15, N = prescaler value (1, 8, 64, 256)
			Asynchronous	35	—	—	ns	
TA11	TTXL	T1CK Low Time	Synchronous mode	Greater of: 20 or (TCY + 20)/N	—	—	ns	Must also meet Parameter TA15, N = prescaler value (1, 8, 64, 256)
			Asynchronous	10	—	—	ns	
TA15	TTXP	T1CK Input Period	Synchronous mode	Greater of: 40 or (2 TCY + 40)/N	—	—	ns	N = prescale value (1, 8, 64, 256)
OS60	Ft1	T1CK Oscillator Input Frequency Range (oscillator enabled by setting bit, TCS (T1CON<1>))		DC	—	50	kHz	
TA20	TCKEXTMRL	Delay from External T1CK Clock Edge to Timer Increment		0.75 TCY + 40	—	1.75 TCY + 40	ns	

Note 1: Timer1 is a Type A.

2: These parameters are characterized, but are not tested in manufacturing.

FIGURE 30-6: INPUT CAPTURE x (ICx) TIMING CHARACTERISTICS



Note: Refer to Figure 30-1 for load conditions.

TABLE 30-26: INPUT CAPTURE x MODULE TIMING REQUIREMENTS

AC CHARACTERISTICS			Standard Operating Conditions: 3.0V to 3.6V (unless otherwise stated) Operating temperature -40°C ≤ TA ≤ +85°C for Industrial -40°C ≤ TA ≤ +125°C for Extended				
Param. No.	**Symbol**	**Characteristics(1)**	**Min.**	**Max.**	**Units**	**Conditions**	
IC10	TccL	ICx Input Low Time	Greater of 12.5 + 25 or (0.5 TCY/N) + 25	—	ns	Must also meet Parameter IC15	N = prescale value (1, 4, 16)
IC11	TccH	ICx Input High Time	Greater of 12.5 + 25 or (0.5 TCY/N) + 25	—	ns	Must also meet Parameter IC15	
IC15	TccP	ICx Input Period	Greater of 25 + 50 or (1 TCY/N) + 50	—	ns		

Note 1: These parameters are characterized, but not tested in manufacturing.

TABLE 30-60: ADC CONVERSION (12-BIT MODE) TIMING REQUIREMENTS

AC CHARACTERISTICS			Standard Operating Conditions: 3.0V to 3.6V (unless otherwise stated)[1] Operating temperature -40°C ≤ TA ≤ +85°C for Industrial -40°C ≤ TA ≤ +125°C for Extended				
Param No.	**Symbol**	**Characteristic**	**Min.**	**Typ.**	**Max.**	**Units**	**Conditions**
Clock Parameters							
AD50	TAD	ADC Clock Period	117.6	—	—	ns	
AD51	tRC	ADC Internal RC Oscillator Period[2]	—	250	—	ns	
Conversion Rate							
AD55	tCONV	Conversion Time	—	14 TAD		ns	
AD56	FCNV	Throughput Rate	—	—	500	ksps	
AD57a	TSAMP	Sample Time when Sampling any ANx Input	3 TAD	—	—	—	
AD57b	TSAMP	Sample Time when Sampling the Op Amp Outputs (Configuration A and Configuration B)[4,5]	3 TAD	—	—	—	
Timing Parameters							
AD60	tPCS	Conversion Start from Sample Trigger[2,3]	2 TAD	—	3 TAD	—	Auto-convert trigger is not selected
AD61	tPSS	Sample Start from Setting Sample (SAMP) bit[2,3]	2 TAD	—	3 TAD	—	
AD62	tCSS	Conversion Completion to Sample Start (ASAM = 1)[2,3]	—	0.5 TAD	—	—	
AD63	tDPU	Time to Stabilize Analog Stage from ADC Off to ADC On[2,3]	—	—	20	μs	**(Note 6)**

Note 1: Device is functional at VBORMIN < VDD < VDDMIN, but will have degraded performance. Device functionality is tested, but not characterized. Analog modules (ADC, op amp/comparator and comparator voltage reference) may have degraded performance. Refer to Parameter BO10 in Table 30-13 for the minimum and maximum BOR values.

2: Parameters are characterized but not tested in manufacturing.

3: Because the sample caps will eventually lose charge, clock rates below 10 kHz may affect linearity performance, especially at elevated temperatures.

4: See Figure 25-6 for configuration information.

5: See Figure 25-7 for configuration information.

6: The parameter, tDPU, is the time required for the ADC module to stabilize at the appropriate level when the module is turned on (ADON (AD1CON1<15>) = 1). During this time, the ADC result is indeterminate.

TABLE 31-12: ADC MODULE SPECIFICATIONS (12-BIT MODE)

AC CHARACTERISTICS			Standard Operating Conditions: 3.0V to 3.6V (unless otherwise stated) Operating temperature -40°C ≤ TA ≤ +150°C				
Param No.	Symbol	Characteristic	Min	Typ	Max	Units	Conditions
ADC Accuracy (12-Bit Mode)(1)							
HAD20a	Nr	Resolution(3)	12 Data Bits			bits	
HAD21a	INL	Integral Nonlinearity	-5.5	—	5.5	LSb	VINL = AVSS = VREFL = 0V, AVDD = VREFH = 3.6V
HAD22a	DNL	Differential Nonlinearity	-1	—	1	LSb	VINL = AVSS = VREFL = 0V, AVDD = VREFH = 3.6V
HAD23a	GERR	Gain Error	-10	—	10	LSb	VINL = AVSS = VREFL = 0V, AVDD = VREFH = 3.6V
HAD24a	EOFF	Offset Error	-5	—	5	LSb	VINL = AVSS = VREFL = 0V, AVDD = VREFH = 3.6V
Dynamic Performance (12-Bit Mode)(2)							
HAD33a	FNYQ	Input Signal Bandwidth	—	—	200	kHz	

Note 1: These parameters are characterized, but are tested at 20 ksps only.

2: These parameters are characterized by similarity, but are not tested in manufacturing.

3: Injection currents > | 0 | can affect the ADC results by approximately 4-6 counts.

TABLE 31-13: ADC MODULE SPECIFICATIONS (10-BIT MODE)

AC CHARACTERISTICS			Standard Operating Conditions: 3.0V to 3.6V (unless otherwise stated) Operating temperature -40°C ≤ TA ≤ +150°C				
Param No.	Symbol	Characteristic	Min	Typ	Max	Units	Conditions
ADC Accuracy (10-Bit Mode)(1)							
HAD20b	Nr	Resolution(3)	10 Data Bits			bits	
HAD21b	INL	Integral Nonlinearity	-1.5	—	1.5	LSb	VINL = AVSS = VREFL = 0V, AVDD = VREFH = 3.6V
HAD22b	DNL	Differential Nonlinearity	-0.25	—	0.25	LSb	VINL = AVSS = VREFL = 0V, AVDD = VREFH = 3.6V
HAD23b	GERR	Gain Error	-2.5	—	2.5	LSb	VINL = AVSS = VREFL = 0V, AVDD = VREFH = 3.6V
HAD24b	EOFF	Offset Error	-1.25	—	1.25	LSb	VINL = AVSS = VREFL = 0V, AVDD = VREFH = 3.6V
Dynamic Performance (10-Bit Mode)(2)							
HAD33b	FNYQ	Input Signal Bandwidth	—	—	400	kHz	

Note 1: These parameters are characterized, but are tested at 20 ksps only.

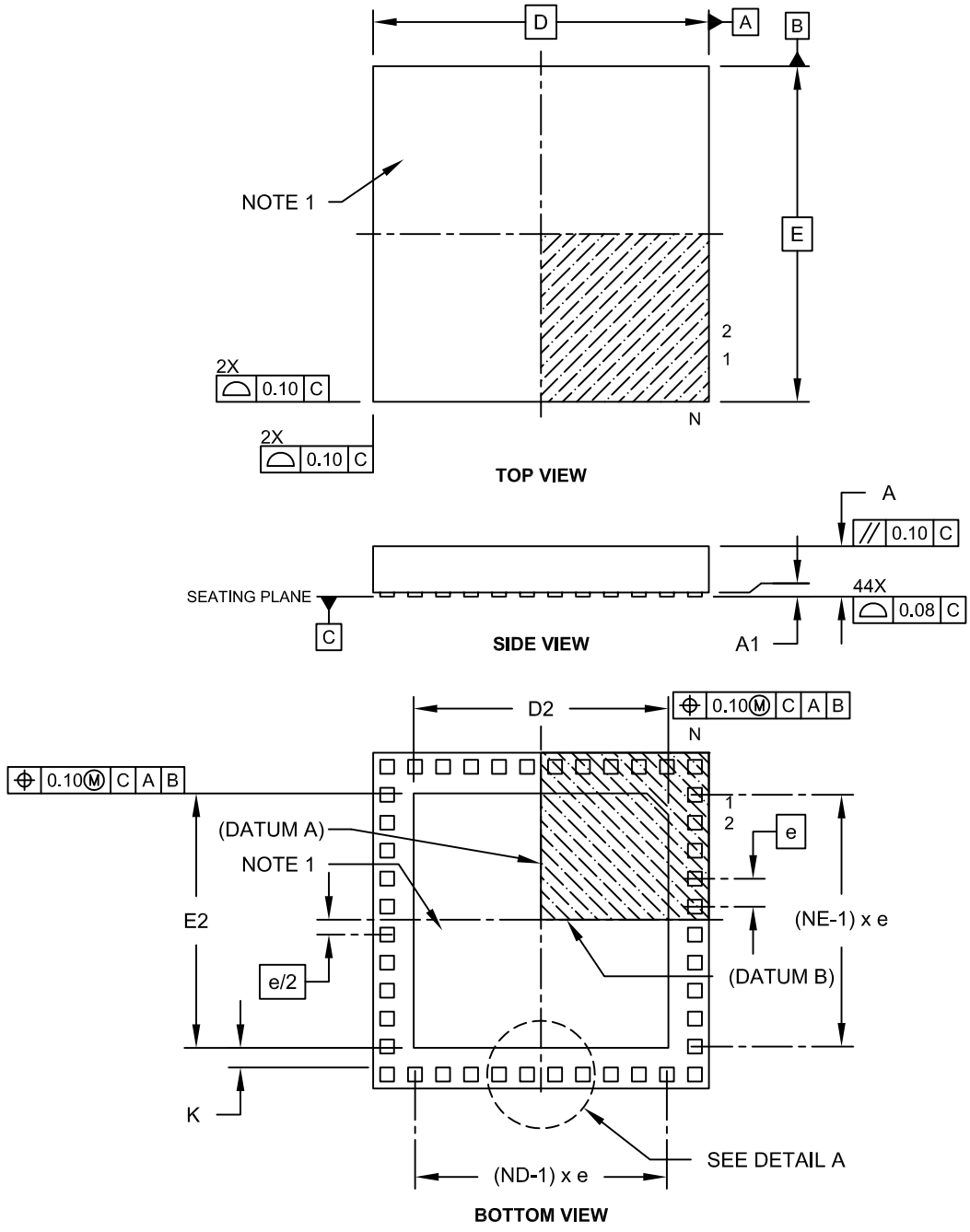
2: These parameters are characterized by similarity, but are not tested in manufacturing.

3: Injection currents > | 0 | can affect the ADC results by approximately 4-6 counts.

NOTES:

44-Terminal Very Thin Leadless Array Package (TL) – 6x6x0.9 mm Body With Exposed Pad [VTLA]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



Microchip Technology Drawing C04-157C Sheet 1 of 2