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Applications of "<u>Embedded -</u> <u>Microcontrollers</u>"

Details

E·XFI

Product Status	Active
Core Processor	PIC
Core Size	16-Bit
Speed	70 MIPs
Connectivity	I ² C, IrDA, LINbus, QEI, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, DMA, Motor Control PWM, POR, PWM, WDT
Number of I/O	53
Program Memory Size	128KB (43K x 24)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	8K x 16
Voltage - Supply (Vcc/Vdd)	3V ~ 3.6V
Data Converters	A/D 16x10b/12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	64-TQFP
Supplier Device Package	64-TQFP (10x10)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/pic24ep128mc206t-i-pt

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4.4.3 DATA MEMORY ARBITRATION AND BUS MASTER PRIORITY

EDS accesses from bus masters in the system are arbitrated.

The arbiter for data memory (including EDS) arbitrates between the CPU, the DMA and the ICD module. In the event of coincidental access to a bus by the bus masters, the arbiter determines which bus master access has the highest priority. The other bus masters are suspended and processed after the access of the bus by the bus master with the highest priority.

By default, the CPU is Bus Master 0 (M0) with the highest priority and the ICD is Bus Master 4 (M4) with the lowest priority. The remaining bus master (DMA Controller) is allocated to M3 (M1 and M2 are reserved and cannot be used). The user application may raise or lower the priority of the DMA Controller to be above that of the CPU by setting the appropriate bits in the EDS Bus Master Priority Control (MSTRPR) register. All bus masters with raised priorities will maintain the same priority relationship relative to each other (i.e., M1 being highest and M3 being lowest, with M2 in between). Also, all the bus masters with priorities below

FIGURE 4-18: ARBITER ARCHITECTURE

that of the CPU maintain the same priority relationship relative to each other. The priority schemes for bus masters with different MSTRPR values are tabulated in Table 4-62.

This bus master priority control allows the user application to manipulate the real-time response of the system, either statically during initialization or dynamically in response to real-time events.

TABLE 4-62:	DATA MEMORY BUS
	ARBITER PRIORITY

Briority	MSTRPR<15:0> Bit Setting ⁽¹⁾				
Phoney	0x0000	0x0020			
M0 (highest)	CPU	DMA			
M1	Reserved	CPU			
M2	Reserved	Reserved			
M3	DMA	Reserved			
M4 (lowest)	ICD	ICD			

Note 1: All other values of MSTRPR<15:0> are reserved.



4.5 Instruction Addressing Modes

The addressing modes shown in Table 4-63 form the basis of the addressing modes optimized to support the specific features of individual instructions. The addressing modes provided in the MAC class of instructions differ from those in the other instruction types.

4.5.1 FILE REGISTER INSTRUCTIONS

Most file register instructions use a 13-bit address field (f) to directly address data present in the first 8192 bytes of data memory (Near Data Space). Most file register instructions employ a working register, W0, which is denoted as WREG in these instructions. The destination is typically either the same file register or WREG (with the exception of the MUL instruction), which writes the result to a register or register pair. The MOV instruction allows additional flexibility and can access the entire Data Space.

4.5.2 MCU INSTRUCTIONS

The three-operand MCU instructions are of the form:

Operand 3 = Operand 1 <function> Operand 2

where Operand 1 is always a working register (that is, the addressing mode can only be Register Direct), which is referred to as Wb. Operand 2 can be a W register fetched from data memory or a 5-bit literal. The result location can either be a W register or a data memory location. The following addressing modes are supported by MCU instructions:

- Register Direct
- · Register Indirect
- · Register Indirect Post-Modified
- Register Indirect Pre-Modified
- 5-Bit or 10-Bit Literal
- Note: Not all instructions support all the addressing modes given above. Individual instructions can support different subsets of these addressing modes.

TABLE 4-63: FUNDAMENTAL ADDRESSING MODES SUPPORTED

Addressing Mode	Description
File Register Direct	The address of the file register is specified explicitly.
Register Direct	The contents of a register are accessed directly.
Register Indirect	The contents of Wn form the Effective Address (EA).
Register Indirect Post-Modified	The contents of Wn form the EA. Wn is post-modified (incremented or decremented) by a constant value.
Register Indirect Pre-Modified	Wn is pre-modified (incremented or decremented) by a signed constant value to form the EA.
Register Indirect with Register Offset (Register Indexed)	The sum of Wn and Wb forms the EA.
Register Indirect with Literal Offset	The sum of Wn and a literal forms the EA.

				(,			
R/SO-0 ⁽¹	⁾ R/W-0 ⁽¹⁾	R/W-0 ⁽¹⁾	R/W-0	U-0	U-0	U-0	U-0
WR	WREN	WRERR	NVMSIDL ⁽²⁾			—	—
bit 15							bit 8
U-0	U-0	U-0	U-0	R/W-0 ⁽¹⁾	R/W-0 ⁽¹⁾	R/W-0 ⁽¹⁾	R/W-0 ⁽¹⁾
	—	—	<u> </u>	NVMOP3 ^(3,4)	NVMOP2 ^(3,4)	NVMOP1 ^(3,4)	NVMOP0 ^(3,4)
bit 7							bit 0
						_	
Legend:		SO = Settab	le Only bit				
R = Reada	ble bit	W = Writable	e bit	U = Unimplem	ented bit, read	as '0'	
-n = Value	at POR	'1' = Bit is se	t	'0' = Bit is clea	ired	x = Bit is unkn	iown
bit 15	 bit 15 WR: Write Control bit⁽¹⁾ 1 = Initiates a Flash memory program or erase operation; the operation is self-timed and the bit i cleared by hardware once the operation is complete 0 = Program or erase operation is complete and inactive 						
bit 14	WREN: Write 1 = Enables F 0 = Inhibits Fl	Enable bit ⁽¹⁾ ⁻ lash program ash program/	n/erase operati ⁄erase operatio	ons			
bit 13	WRERR: Writ 1 = An improp on any se 0 = The progr	e Sequence E per program of t attempt of th ram or erase	Error Flag bit ⁽¹⁾ rerase sequence e WR bit) operation comp	ce attempt or ter	mination has oc	curred (bit is se	t automatically
bit 12	NVMSIDL: N\ 1 = Flash volt 0 = Flash volt	/M Stop in Idl age regulator age regulator	e Control bit ⁽²⁾ goes into Star is active durin	ndby mode duri g Idle mode	ng Idle mode		
bit 11-4	Unimplement	ted: Read as	'0'	-			
bit 11-4 Unimplemented: Read as '0' bit 3-0 NVMOP<3:0>: NVM Operation Select bits ^(1,3,4) 1111 = Reserved 1100 = Reserved 1101 = Reserved 1001 = Reserved 1011 = Reserved 1010 = Reserved 0011 = Memory page erase operation 0010 = Reserved 0011 = Memory double-word program operation ⁽⁵⁾ 0000 = Reserved							
Note 1: 2: 3: 4: 5:	These bits can only If this bit is set, the (TVREG) before Fla All other combination Execution of the PV Two adjacent word	/ be reset on a re will be mini sh memory be ons of NVMO wRSAV instruct s on a 4-word	a POR. mal power sav ecomes operat P<3:0> are uni tion is ignored I boundary are	rings (IIDLE) and ional. implemented. while any of the programmed d	d upon exiting lo e NVM operatio uring execution	the mode, there ns are in progra	is a delay ess. on.

REGISTER 5-1: NVMCON: NONVOLATILE MEMORY (NVM) CONTROL REGISTER

R/W-0	R/W-0	R/W-0	R/W-0	R/C-0	R/C-0	R-0	R/W-0	
OA	OB	SA	SB	OAB	SAB	DA	DC	
bit 15							bit 8	
R/W-0 ⁽³⁾	R/W-0 ⁽³⁾	R/W-0 ⁽³⁾	R-0	R/W-0	R/W-0	R/W-0	R/W-0	
	IPL<2:0> ⁽²⁾		RA	Ν	OV	Z	С	
bit 7						-	bit 0	
								1

REGISTER 7-1: SR: CPU STATUS REGISTER⁽¹⁾

Legend:	C = Clearable bit		-		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'			
-n = Value at POR	'1'= Bit is set	'0' = Bit is cleared	x = Bit is unknown		

bit 7-5	IPL<2:0>: CPU Interrupt Priority Level Status bits ^(2,3)
	111 = CPU Interrupt Priority Level is 7 (15); user interrupts are disabled
	110 = CPU Interrupt Priority Level is 6 (14)
	101 = CPU Interrupt Priority Level is 5 (13)
	100 = CPU Interrupt Priority Level is 4 (12)
	011 = CPU Interrupt Priority Level is 3 (11)
	010 = CPU Interrupt Priority Level is 2 (10)
	001 = CPU Interrupt Priority Level is 1 (9)
	000 = CPU Interrupt Priority Level is 0 (8)

- **Note 1:** For complete register details, see Register 3-1.
 - 2: The IPL<2:0> bits are concatenated with the IPL<3> bit (CORCON<3>) to form the CPU Interrupt Priority Level. The value in parentheses indicates the IPL, if IPL<3> = 1. User interrupts are disabled when IPL<3> = 1.
 - **3:** The IPL<2:0> Status bits are read-only when the NSTDIS bit (INTCON1<15>) = 1.

R/W-0	R/W-0	R/W-1	R/W-1	R/W-0	R/W-0	R/W-0	R/W-0
ROI	DOZE2 ⁽¹⁾	DOZE1 ⁽¹⁾	DOZE0 ⁽¹⁾	DOZEN ^(2,3)	FRCDIV2	FRCDIV1	FRCDIV0
bit 15							bit 8
R/W-0	R/W-1	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
PLLPOST	1 PLLPOST0	—	PLLPRE4	PLLPRE3	PLLPRE2	PLLPRE1	PLLPRE0
bit 7							bit 0
Legend:						<i>(</i> -)	
R = Readat	ble bit	W = Writable	bit	U = Unimpler	nented bit, read	as '0'	
-n = Value a	at POR	'1' = Bit is set		'0' = Bit is cle	ared	x = Bit is unkr	IOWN
bit 1E		on Interrupt b	.+				
	1 = Interrunte	will clear the	NOZEN bit				
	0 = Interrupts	s have no effect	t on the DOZE	EN bit			
bit 14-12	DOZE<2:0>:	Processor Clo	ck Reduction S	Select bits ⁽¹⁾			
	111 = Fcy div	vided by 128					
	110 = Fcy div	vided by 64					
	101 = FCY div 100 = FCY div	/ided by 32					
	011 = FCY div	vided by 8 (defa	ault)				
	010 = FCY div	vided by 4					
	001 = FCY div	/ided by 2					
bit 11		e Mode Enable	. _{hit} (2,3)				
	1 = DOZER. DOZE < 2:0	0> field specifi	es the ratio be	tween the peri	pheral clocks a	nd the process	or clocks
	0 = Processor	r clock and per	ipheral clock r	atio is forced t	o 1:1		
bit 10-8	FRCDIV<2:0>	Internal Fast	RC Oscillator	Postscaler bit	S		
	111 = FRC di	vided by 256					
	110 = FRC di	vided by 64					
	100 = FRC d i	vided by 32 vided by 16					
	011 = FRC di	vided by 8					
	010 = FRC di	vided by 4					
	001 = FRC di 000 = FRC di	vided by 2 vided by 1 (de	fault)				
bit 7-6	PLLPOST<1:	0>: PLL VCO	Output Divider	r Select bits (al	so denoted as '	N2', PLL posts	caler)
	11 = Output d	livided by 8	,	,		<i>,</i> ,	,
	10 = Reserve	d					
	01 = Output d	livided by 4 (de	etault)				
bit 5	Unimplement	ted: Read as '	0'				
5110	emplement		•				
Note 1:	The DOZE<2:0> bi DOZE<2:0> are igi	its can only be nored.	written to whe	en the DOZEN	bit is clear. If D	OZEN = 1, any	writes to
2:	This bit is cleared v	when the ROI I	oit is set and a	an interrupt occ	urs.		

REGISTER 9-2: CLKDIV: CLOCK DIVISOR REGISTER

The DOZEN bit cannot be set if DOZE<2:0> = 000. If DOZE<2:0> = 000, any attempt by user software to set the DOZEN bit is ignored.

REGISTER 11-17: RPINR39: PERIPHERAL PIN SELECT INPUT REGISTER 39 (dsPIC33EPXXXMC20X/50X AND PIC24EPXXXMC20X DEVICES ONLY)

	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0			
—				DTCMP3R<6:0)>					
bit 15							bit 8			
U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0			
	DTCMP2R<6:0>									
bit 7							bit 0			
Legend:										
R = Readab	le bit	W = Writable I	oit	U = Unimplen	nented bit, rea	ad as '0'				
-n = Value a	t POR	'1' = Bit is set		'0' = Bit is clea	ared	x = Bit is unkr	nown			
bit 14-8	DTCMP3R< (see Table 1 1111001 =	6:0>: Assign PW 1-2 for input pin nput tied to RPI	/M Dead-Tim selection nun 121	e Compensatio nbers)	n Input 3 to th	ne Corresponding	g RPn Pin bits			
	0000001 = 0000000 =	nput tied to CMI nput tied to Vss	P1							
bit 7	0000001 = 0000000 = Unimpleme	nput tied to CMI nput tied to Vss nted: Read as '0	21)'							



FIGURE 16-2: HIGH-SPEED PWMx MODULE REGISTER INTERCONNECTION DIAGRAM

REGISTER 16-8: PDCx: PWMx GENERATOR DUTY CYCLE REGISTER

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
			PDC	x<15:8>			
bit 15							bit 8
R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
			PDC	x<7:0>			
bit 7							bit 0
Legend:							
R = Readable	bit	W = Writable	bit	U = Unimpler	mented bit, rea	id as '0'	
-n = Value at P	OR	'1' = Bit is set		'0' = Bit is cleared x = Bit is unknown			nown

bit 15-0 **PDCx<15:0>:** PWMx Generator # Duty Cycle Value bits

REGISTER 16-9: PHASEx: PWMx PRIMARY PHASE-SHIFT REGISTER

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
			PHAS	Ex<15:8>			
bit 15							bit 8
R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
			PHAS	SEx<7:0>			
bit 7							bit 0
Legend:							
R = Readable I	bit	W = Writable b	it	U = Unimpler	mented bit, rea	ad as '0'	
-n = Value at P	OR	'1' = Bit is set		'0' = Bit is cleared x = Bit is unknown			nown

bit 15-0 PHASEx<15:0>: PWMx Phase-Shift Value or Independent Time Base Period for the PWM Generator bits

Note 1: If ITB (PWMCONx<9>) = 0, the following applies based on the mode of operation: Complementary, Redundant and Push-Pull Output mode (PMOD<1:0> (IOCON<11:10>) = 00, 01 or 10), PHASEx<15:0> = Phase-shift value for PWMxH and PWMxL outputs

 If ITB (PWMCONx<9>) = 1, the following applies based on the mode of operation: Complementary, Redundant and Push-Pull Output mode (PMOD<1:0> (IOCONx<11:10>) = 00, 01 or 10), PHASEx<15:0> = Independent time base period value for PWMxH and PWMxL

REGISTER 17-3: QEI1STAT: QEI1 STATUS REGISTER (CONTINUED)

bit 2	HOMIEN: Home Input Event Interrupt Enable bit 1 = Interrupt is enabled 0 = Interrupt is disabled
bit 1	IDXIRQ: Status Flag for Index Event Status bit 1 = Index event has occurred 0 = No Index event has occurred
bit 0	IDXIEN: Index Input Event Interrupt Enable bit 1 = Interrupt is enabled 0 = Interrupt is disabled

Note 1: This status bit is only applicable to PIMOD<2:0> modes, '011' and '100'.

REGISTER 17-17: INT1TMRH: INTERVAL 1 TIMER HIGH WORD REGISTER

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0		
			INTTM	R<31:24>					
bit 15							bit 8		
R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0		
	INTTMR<23:16>								
bit 7							bit 0		
Legend:									
R = Readable bit W = Writable bit U = Unimplemented bit, read as '0'									
-n = Value at P	POR'1' = Bit is set'0' = Bit is clearedx = Bit is unknown			nown					

bit 15-0 INTTMR<31:16>: High Word Used to Form 32-Bit Interval Timer Register (INT1TMR) bits

REGISTER 17-18: INT1TMRL: INTERVAL 1 TIMER LOW WORD REGISTER

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0		
			INTTM	1R<15:8>					
bit 15							bit 8		
R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0		
	INTTMR<7:0>								
bit 7							bit 0		
Legend:									
R = Readable bitW = Writable bitU = Unimplemented bit, read as			d as '0'						
-n = Value at P	= Value at POR '1' = Bit is set '0' = Bit is cleared x = Bit is unknow			nown					

bit 15-0 INTTMR<15:0>: Low Word Used to Form 32-Bit Interval Timer Register (INT1TMR) bits

18.3 SPIx Control Registers

R/W-0 U-0 R/W-0 U-0 R/W-0 R/W-0 R/W-0 U-0 SPIEN SPISIDL SPIBEC<2:0> _____ bit 15 R/W-0 R/W-0 R/W-0 R/C-0, HS R/W-0 R/W-0 R-0, HS, HC R-0, HS, HC SRMPT SPIROV SRXMPT SISEL2 SISEL1 SISEL0 SPITBF SPIRBF bit 7 bit 0 Legend: C = Clearable bit HS = Hardware Settable bit HC = Hardware Clearable bit R = Readable bit W = Writable bit U = Unimplemented bit, read as '0' -n = Value at POR '1' = Bit is set '0' = Bit is cleared x = Bit is unknown bit 15 SPIEN: SPIx Enable bit 1 = Enables the module and configures SCKx, SDOx, SDIx and \overline{SSx} as serial port pins 0 = Disables the module bit 14 Unimplemented: Read as '0' bit 13 SPISIDL: SPIx Stop in Idle Mode bit 1 = Discontinues the module operation when device enters Idle mode 0 = Continues the module operation in Idle mode bit 12-11 Unimplemented: Read as '0' bit 10-8 SPIBEC<2:0>: SPIx Buffer Element Count bits (valid in Enhanced Buffer mode) Master mode: Number of SPIx transfers that are pending. Slave mode: Number of SPIx transfers that are unread. **SRMPT:** SPIx Shift Register (SPIxSR) Empty bit (valid in Enhanced Buffer mode) bit 7 1 = SPIx Shift register is empty and Ready-To-Send or receive the data 0 = SPIx Shift register is not empty bit 6 SPIROV: SPIx Receive Overflow Flag bit 1 = A new byte/word is completely received and discarded; the user application has not read the previous data in the SPIxBUF register

REGISTER 18-1: SPIxSTAT: SPIx STATUS AND CONTROL REGISTER

0 = No overflow has occurred SRXMPT: SPIx Receive FIFO Empty bit (valid in Enhanced Buffer mode) bit 5 1 = RX FIFO is empty 0 = RX FIFO is not empty bit 4-2 SISEL<2:0>: SPIx Buffer Interrupt Mode bits (valid in Enhanced Buffer mode) 111 = Interrupt when the SPIx transmit buffer is full (SPITBF bit is set) 110 = Interrupt when last bit is shifted into SPIxSR and as a result, the TX FIFO is empty 101 = Interrupt when the last bit is shifted out of SPIxSR and the transmit is complete 100 = Interrupt when one data is shifted into the SPIxSR and as a result, the TX FIFO has one open memory location

- 011 = Interrupt when the SPIx receive buffer is full (SPIRBF bit is set)
- 010 = Interrupt when the SPIx receive buffer is 3/4 or more full
- 001 = Interrupt when data is available in the receive buffer (SRMPT bit is set)
- 000 = Interrupt when the last data in the receive buffer is read and as a result, the buffer is empty (SRXMPT bit is set)

bit 8

					_		
R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
EDG1MOD	EDG1POL	EDG1SEL3	EDG1SEL2	EDG1SEL1	EDG1SEL0	EDG2STAT	EDG1STAT
bit 15							bit 8
R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	U-0	U-0
EDG2MOD	EDG2POL	EDG2SEL3	EDG2SEL2	EDG2SEL1	EDG2SEL0		—
bit 7							bit 0
Legend:							
R = Readable	e bit	W = Writable	bit	U = Unimplen	nented bit, read	l as '0'	
-n = Value at	POR	'1' = Bit is set		'0' = Bit is clea	ared	x = Bit is unkr	nown
bit 15	EDG1MOD: E	Edge 1 Edge Sa	ampling Mode	Selection bit			
	1 = Edge 1 is	edge-sensitive	9				
h:+ 4 4		s level-sensitive					
DIT 14	EDG1POL: E	dge 1 Polarity	Select Dit	dao roopopoo			
	1 = Edge 1 is $0 = Edge 1$ is	s programmed f	or a positive e	edae response			
bit 13-10	EDG1SEL<3:	:0>: Edae 1 So	urce Select bits	3			
	1xxx = Rese	rved					
	01xx = Reser	rved					
	0011 = CTED)1 pin					
	00010 = CTEL	module					
	0000 = Timer	1 module					
bit 9	EDG2STAT: E	Edge 2 Status b	it				
	Indicates the	status of Edge	2 and can be v	vritten to contro	ol the edge sou	rce.	
	1 = Edge 2h	as occurred	J				
hit Q] ;+				
DILO	EDGISIAI: E	status of Edge	il 1 and can be y	written to contro	the edge sou	rce	
	1 = Edge 1 h	as occurred			i the edge sou	ice.	
	0 = Edge 1 h	as not occurred	t				
bit 7	EDG2MOD: E	Edge 2 Edge Sa	ampling Mode	Selection bit			
	1 = Edge 2 is	edge-sensitive	9				
	0 = Edge 2 is	s level-sensitive					
bit 6	EDG2POL: E	dge 2 Polarity	Select bit				
	1 = Edge 2 Is 0 = Edge 2 is	s programmed i	or a positive e	age response			
bit 5-2	EDG2SEL<3:	:0>: Edge 2 So	urce Select bits	8			
	1111 = Reser	rved		-			
	01xx = Reser	rved					
	0100 = CMP1	1 module					
	0011 = CIEL 0010 = CTFF	o∠ pin)1 pin					
	0001 = OC1	module					
	0000 = IC1 m	nodule					
bit 1-0	Unimplemen	ted: Read as ')'				

REGISTER 22-2: CTMUCON2: CTMU CONTROL REGISTER 2



TADLE 30-23. THVIER I EATERINAL CLOCK THVIING REQUIREIVIEN 13	TABLE 30-23:	TIMER1 EXTERNAL	CLOCK TIMING	REQUIREMENTS ⁽¹⁾
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AC CHARACTERISTICS			Standard Ope (unless other) Operating tem	rating C vise sta perature	conditions: 3.0 ted) -40°C ≤ TA ≤ -40°C ≤ TA ≤	V to 3.6 +85°C +125°C	V for Industrial C for Extended	
Param No.	Symbol	Characteristic ⁽²⁾		Min.	Тур.	Max.	Units	Conditions
TA10	ТтхН	T1CK High Time	Synchronous mode	Greater of: 20 or (Tcy + 20)/N	_	—	ns	Must also meet Parameter TA15, N = prescaler value (1, 8, 64, 256)
			Asynchronous	35		—	ns	
TA11	ΤτxL	T1CK Low Time	Synchronous mode	Greater of: 20 or (Tcy + 20)/N	_	_	ns	Must also meet Parameter TA15, N = prescaler value (1, 8, 64, 256)
			Asynchronous	10	—	—	ns	
TA15	ΤτχΡ	T1CK Input Period	Synchronous mode	Greater of: 40 or (2 Tcy + 40)/N	_		ns	N = prescale value (1, 8, 64, 256)
OS60	Ft1	T1CK Oscillator Input Frequency Range (oscillator enabled by setting bit, TCS (T1CON<1>))		DC		50	kHz	
TA20	TCKEXTMRL	Delay from E Clock Edge t Increment	Delay from External T1CK Clock Edge to Timer Increment			1.75 Tcy + 40	ns	

Note 1: Timer1 is a Type A.

2: These parameters are characterized, but are not tested in manufacturing.



FIGURE 30-36: ADC CONVERSION (12-BIT MODE) TIMING CHARACTERISTICS (ASAM = 0, SSRC<2:0> = 000, SSRCG = 0)

31.1 High-Temperature DC Characteristics

TABLE 31-1: OPERATING MIPS VS. VOLTAGE

			Max MIPS			
Characteristic VDD Range (in Volts)		Temperature Range (in °C)	dsPIC33EPXXXGP50X, dsPIC33EPXXXMC20X/50X and PIC24EPXXXGP/MC20X			
HDC5	3.0 to 3.6V ⁽¹⁾	-40°C to +150°C	40			

Note 1: Device is functional at VBORMIN < VDD < VDDMIN. Analog modules, such as the ADC, may have degraded performance. Device functionality is tested but not characterized.

TABLE 31-2: THERMAL OPERATING CONDITIONS

Rating	Symbol	Min	Тур	Max	Unit
High-Temperature Devices					
Operating Junction Temperature Range	TJ	-40		+155	°C
Operating Ambient Temperature Range	TA	-40	—	+150	°C
Power Dissipation: Internal Chip Power Dissipation: $PINT = VDD x (IDD - \Sigma IOH)$ PDPINT + PI/OI/O Pin Power Dissipation: $I/O = \Sigma (\{VDD - VOH\} x IOH) + \Sigma (VOL x IOL)$ PDPINT + PI/O)	W
Maximum Allowed Power Dissipation	PDMAX	(TJ – TA)/θJ	IA	W

TABLE 31-3: DC TEMPERATURE AND VOLTAGE SPECIFICATIONS

DC CHARACTERISTICS			Standard Operating Conditions: 3.0V to 3.6V(unless otherwise stated)Operating temperature $-40^{\circ}C \le TA \le +150^{\circ}C$				
Parameter No.	Symbol	Characteristic	Min Typ Max Units Condition				Conditions
Operating Voltage							
HDC10	CC10 Supply Voltage						
	Vdd	_	3.0	3.3	3.6	V	-40°C to +150°C

33.2 Package Details

28-Lead Skinny Plastic Dual In-Line (SP) – 300 mil Body [SPDIP]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



	Units		INCHES	
Dimensio	n Limits	MIN	NOM	MAX
Number of Pins	Ν		28	
Pitch	е		.100 BSC	
Top to Seating Plane	А	-	-	.200
Molded Package Thickness	A2	.120	.135	.150
Base to Seating Plane	A1	.015	-	-
Shoulder to Shoulder Width	E	.290	.310	.335
Molded Package Width	E1	.240	.285	.295
Overall Length	D	1.345	1.365	1.400
Tip to Seating Plane	L	.110	.130	.150
Lead Thickness	С	.008	.010	.015
Upper Lead Width	b1	.040	.050	.070
Lower Lead Width	b	.014	.018	.022
Overall Row Spacing §	eB	_	_	.430

Notes:

1. Pin 1 visual index feature may vary, but must be located within the hatched area.

2. § Significant Characteristic.

3. Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed .010" per side.

4. Dimensioning and tolerancing per ASME Y14.5M.

BSC: Basic Dimension. Theoretically exact value shown without tolerances.

Microchip Technology Drawing C04-070B

28-Lead Plastic Small Outline (SO) - Wide, 7.50 mm Body [SOIC]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging





Microchip Technology Drawing C04-052C Sheet 1 of 2

Section Name	Update Description
Section 16.0 "High-Speed PWM Module (dsPIC33EPXXXMC20X/50X and PIC24EPXXXMC20X Devices Only)"	Updated the High-Speed PWM Module Register Interconnection Diagram (see Figure 16-2). Added the TRGCONx and TRIGx registers (see Register 16-12 and Register 16-14, respectively).
Section 21.0 "Enhanced CAN (ECAN™) Module (dsPIC33EPXXXGP/MC50X Devices Only)"	Updated the CANCKS bit value definitions in CiCTRL1: ECAN Control Register 1 (see Register 21-1).
Section 22.0 "Charge Time Measurement Unit (CTMU)"	Updated the IRNG<1:0> bit value definitions and added Note 2 in the CTMU Current Control Register (see Register 22-3).
Section 25.0 "Op amp/ Comparator Module"	Updated the Op amp/Comparator I/O Operating Modes Diagram (see Figure 25-1). Updated the User-programmable Blanking Function Block Diagram (see Figure 25-3). Updated the Digital Filter Interconnect Block Diagram (see Figure 25-4). Added Section 25.1 "Op amp Application Considerations" . Added Note 2 to the Comparator Control Register (see Register 25-2). Updated the bit definitions in the Comparator Mask Gating Control Register (see Register 25-5).
Section 27.0 "Special Features"	Updated the FICD Configuration Register, updated Note 1, and added Note 3 in the Configuration Byte Register Map (see Table 27-1). Added Section 27.2 "User ID Words" .
Section 30.0 "Electrical Characteristics"	 Updated the following Absolute Maximum Ratings: Maximum current out of Vss pin Maximum current into VDD pin Added Note 1 to the Operating MIPS vs. Voltage (see Table 30-1).
	Updated all Idle Current (IIDLE) Typical and Maximum DC Characteristics values (see Table 30-7).
	Updated all Doze Current (IDOZE) Typical and Maximum DC Characteristics values (see Table 30-9).
	Added Note 2, removed Parameter CM24, updated the Typical values Parameters CM10, CM20, CM21, CM32, CM41, CM44, and CM45, and updated the Minimum values for CM40 and CM41, and the Maximum value for CM40 in the AC/DC Characteristics: Op amp/Comparator (see Table 30-14).
	Updated Note 2 and the Typical value for Parameter VR310 in the Op amp/ Comparator Reference Voltage Settling Time Specifications (see Table 30-15).
	Added Note 1, removed Parameter VRD312, and added Parameter VRD314 to the Op amp/Comparator Voltage Reference DC Specifications (see Table 30-16).
	Updated the Minimum, Typical, and Maximum values for Internal LPRC Accuracy (see Table 30-22).
	Updated the Minimum, Typical, and Maximum values for Parameter SY37 in the Reset, Watchdog Timer, Oscillator Start-up Timer, Power-up Timer Timing Requirements (see Table 30-24).
	The Maximum Data Rate values were updated for the SPI2 Maximum Data/Clock Rate Summary (see Table 30-35)

TABLE A-2: MAJOR SECTION UPDATES (CONTINUED)

Revision D (December 2011)

This revision includes typographical and formatting changes throughout the data sheet text.

All other major changes are referenced by their respective section in Table A-3.

TABLE A-3: MAJOR SECTION UPDATES

Section Name	Update Description
"16-bit Microcontrollers and Digital Signal Controllers (up to 512-Kbyte Flash and 48-Kbyte SRAM) with High- Speed PWM, Op amps, and Advanced Analog"	Removed the Analog Comparators column and updated the Op amps/Comparators column in Table 1 and Table 2.
Section 21.0 "Enhanced CAN (ECAN™) Module (dsPIC33EPXXXGP/MC50X Devices Only)"	Updated the CANCKS bit value definitions in CiCTRL1: ECAN Control Register 1 (see Register 21-1).
Section 30.0 "Electrical Characteristics"	Updated the VBOR specifications and/or its related note in the following electrical characteristics tables: • Table 30-1 • Table 30-4 • Table 30-12 • Table 30-14 • Table 30-15 • Table 30-16 • Table 30-56 • Table 30-57 • Table 30-58 • Table 30-59 • Table 30-60