



Welcome to [E-XFL.COM](#)

What is "[Embedded - Microcontrollers](#)"?

"[Embedded - Microcontrollers](#)" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "[Embedded - Microcontrollers](#)"

Details

Product Status	Active
Core Processor	PIC
Core Size	16-Bit
Speed	60 MIPS
Connectivity	I ² C, IrDA, LINbus, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, DMA, POR, PWM, WDT
Number of I/O	21
Program Memory Size	256KB (85.5K x 24)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	16K x 16
Voltage - Supply (Vcc/Vdd)	3V ~ 3.6V
Data Converters	A/D 6x10b/12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 125°C (TA)
Mounting Type	Surface Mount
Package / Case	28-SSOP (0.209", 5.30mm Width)
Supplier Device Package	28-SSOP
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/pic24ep256gp202-e-ss

Table of Contents

1.0	Device Overview	25
2.0	Guidelines for Getting Started with 16-bit Digital Signal Controllers and Microcontrollers	29
3.0	CPU	35
4.0	Memory Organization	45
5.0	Flash Program Memory	119
6.0	Resets	123
7.0	Interrupt Controller	127
8.0	Direct Memory Access (DMA)	139
9.0	Oscillator Configuration	153
10.0	Power-Saving Features	163
11.0	I/O Ports	173
12.0	Timer1	203
13.0	Timer2/3 and Timer4/5	207
14.0	Input Capture	213
15.0	Output Compare	219
16.0	High-Speed PWM Module (dsPIC33EPXXXMC20X/50X and PIC24EPXXXMC20X Devices Only)	225
17.0	Quadrature Encoder Interface (QEI) Module (dsPIC33EPXXXMC20X/50X and PIC24EPXXXMC20X Devices Only)	249
18.0	Serial Peripheral Interface (SPI)	265
19.0	Inter-Integrated Circuit™ (I ² C™)	273
20.0	Universal Asynchronous Receiver Transmitter (UART)	281
21.0	Enhanced CAN (ECAN™) Module (dsPIC33EPXXXGP/MC50X Devices Only)	287
22.0	Charge Time Measurement Unit (CTMU)	315
23.0	10-Bit/12-Bit Analog-to-Digital Converter (ADC)	321
24.0	Peripheral Trigger Generator (PTG) Module	337
25.0	Op Amp/Comparator Module	355
26.0	Programmable Cyclic Redundancy Check (CRC) Generator	373
27.0	Special Features	379
28.0	Instruction Set Summary	387
29.0	Development Support	397
30.0	Electrical Characteristics	401
31.0	High-Temperature Electrical Characteristics	467
32.0	DC and AC Device Characteristics Graphs	475
33.0	Packaging Information	479
	Appendix A: Revision History	507
	Index	517
	The Microchip Web Site	525
	Customer Change Notification Service	525
	Customer Support	525
	Product Identification System	527

FIGURE 4-2: PROGRAM MEMORY MAP FOR dsPIC33EP64GP50X, dsPIC33EP64MC20X/50X AND PIC24EP64GP/MC20X DEVICES

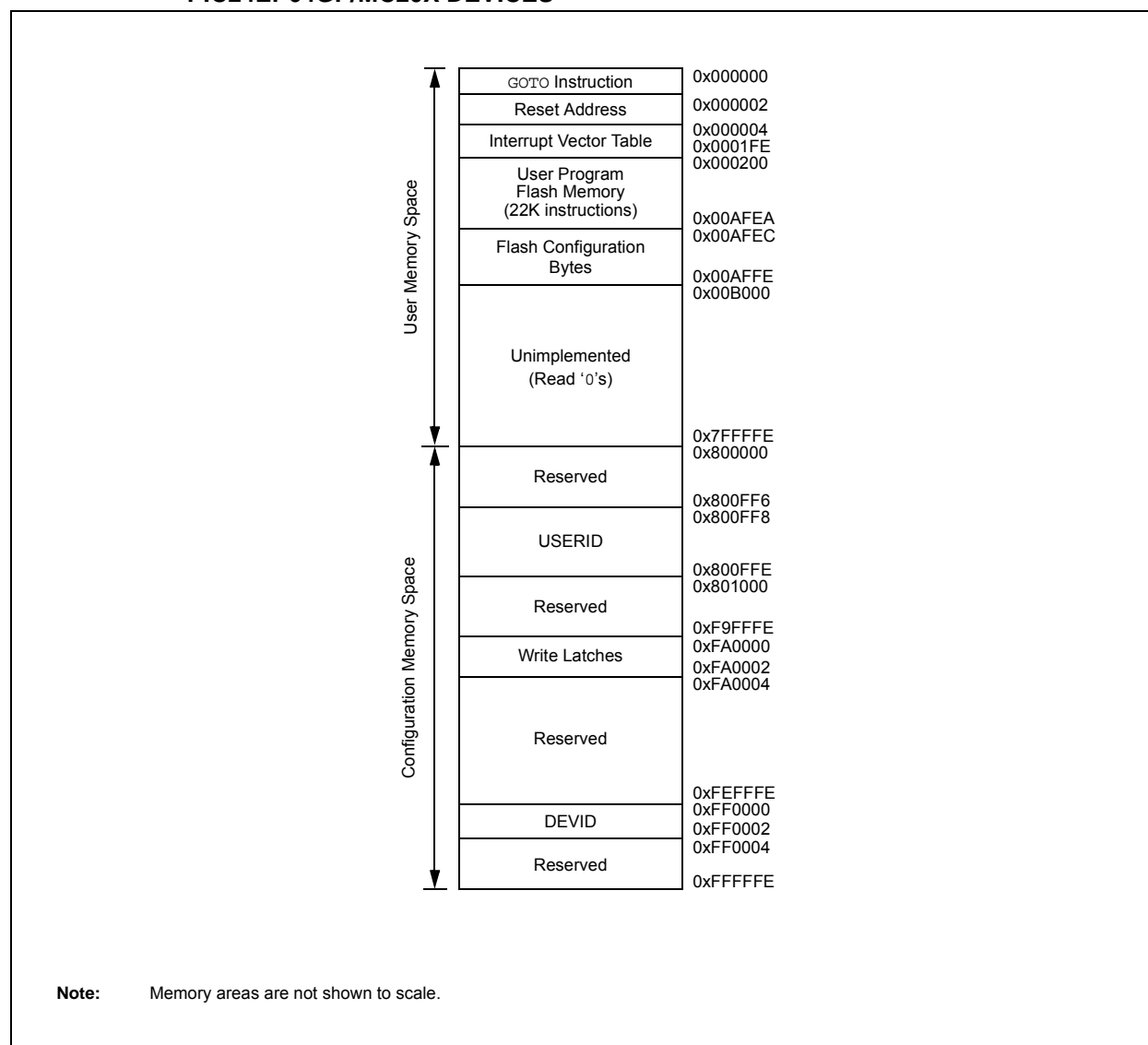


FIGURE 4-15: DATA MEMORY MAP FOR PIC24EP256GP/MC20X/50X DEVICES

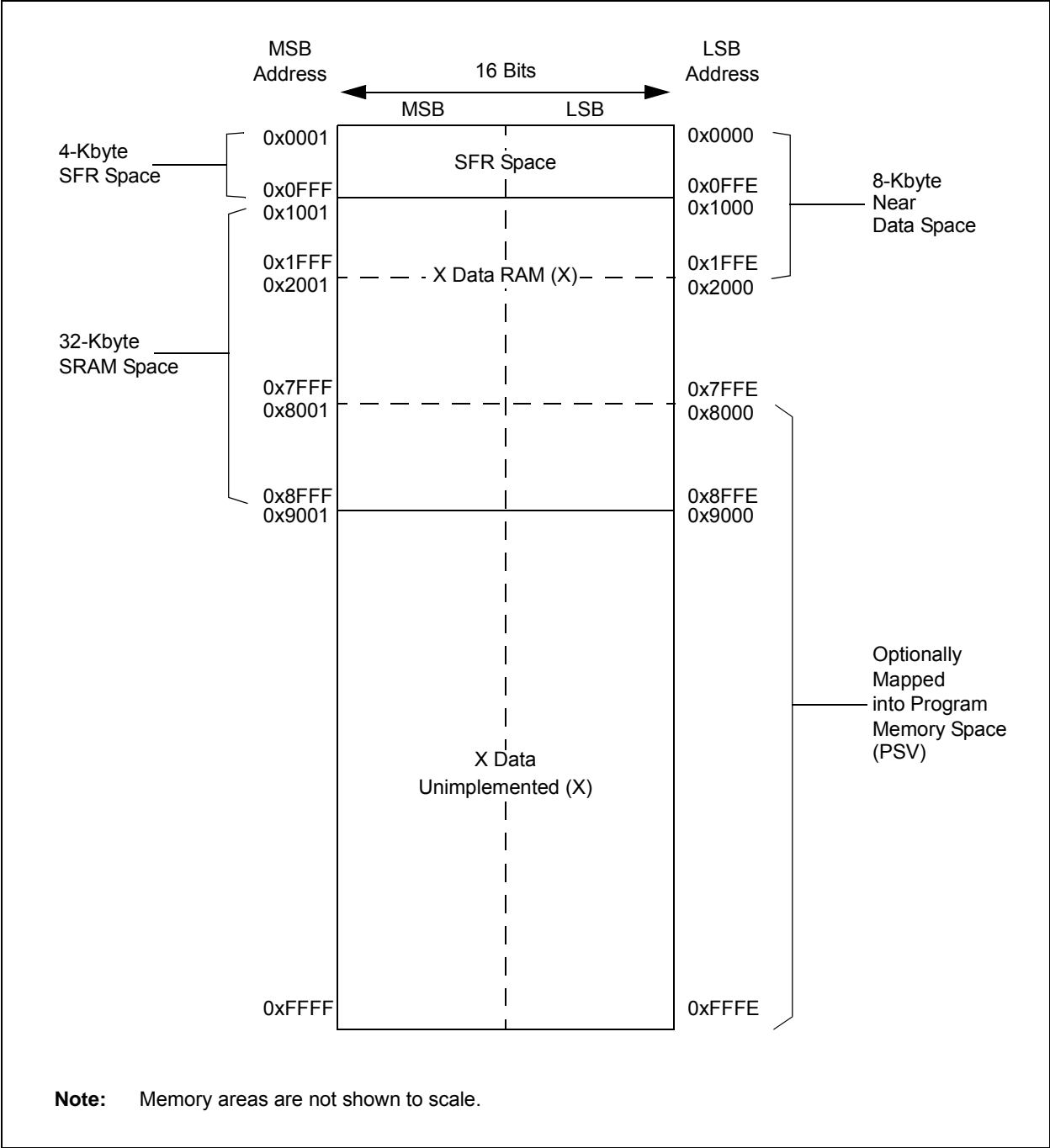


TABLE 4-20: ADC1 REGISTER MAP

File Name	Addr.	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	All Resets	
ADC1BUF0	0300	ADC1 Data Buffer 0																xxxx	
ADC1BUF1	0302	ADC1 Data Buffer 1																xxxx	
ADC1BUF2	0304	ADC1 Data Buffer 2																xxxx	
ADC1BUF3	0306	ADC1 Data Buffer 3																xxxx	
ADC1BUF4	0308	ADC1 Data Buffer 4																xxxx	
ADC1BUF5	030A	ADC1 Data Buffer 5																xxxx	
ADC1BUF6	030C	ADC1 Data Buffer 6																xxxx	
ADC1BUF7	030E	ADC1 Data Buffer 7																xxxx	
ADC1BUF8	0310	ADC1 Data Buffer 8																xxxx	
ADC1BUF9	0312	ADC1 Data Buffer 9																xxxx	
ADC1BUFA	0314	ADC1 Data Buffer 10																xxxx	
ADC1BUFB	0316	ADC1 Data Buffer 11																xxxx	
ADC1BUFC	0318	ADC1 Data Buffer 12																xxxx	
ADC1BUFD	031A	ADC1 Data Buffer 13																xxxx	
ADC1BUFE	031C	ADC1 Data Buffer 14																xxxx	
ADC1BUFF	031E	ADC1 Data Buffer 15																xxxx	
AD1CON1	0320	ADON	—	ADSIDL	ADDMABM	—	AD12B	FORM<1:0>		SSRC<2:0>			SSRCG	SIMSAM	ASAM	SAMP	DONE	0000	
AD1CON2	0322	VCFG<2:0>			—	—	CSCNA	CHPS<1:0>		BUFS	SMPI<4:0>					BUFM	ALTS	0000	
AD1CON3	0324	ADRC	—	—	SAMC<4:0>				ADCS<7:0>										0000
AD1CHS123	0326	—	—	—	—	—	CH123NB<1:0>		CH123SB	—	—	—	—	—	CH123NA<1:0>		CH123SA	0000	
AD1CHS0	0328	CH0NB	—	—	CH0SB<4:0>				CH0NA	—	—	CH0SA<4:0>						0000	
AD1CSSH	032E	CSS31	CSS30	—	—	—	CSS26	CSS25	CSS24	—	—	—	—	—	—	—	—	0000	
AD1CSSL	0330	CSS15	CSS14	CSS13	CSS12	CSS11	CSS10	CSS9	CSS8	CSS7	CSS6	CSS5	CSS4	CSS3	CSS2	CSS1	CSS0	0000	
AD1CON4	0332	—	—	—	—	—	—	—	ADDMAEN	—	—	—	—	—	DMABL<2:0>			0000	

Legend: x = unknown value on Reset, — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

TABLE 4-37: PMD REGISTER MAP FOR PIC24EPXXXGP20X DEVICES ONLY

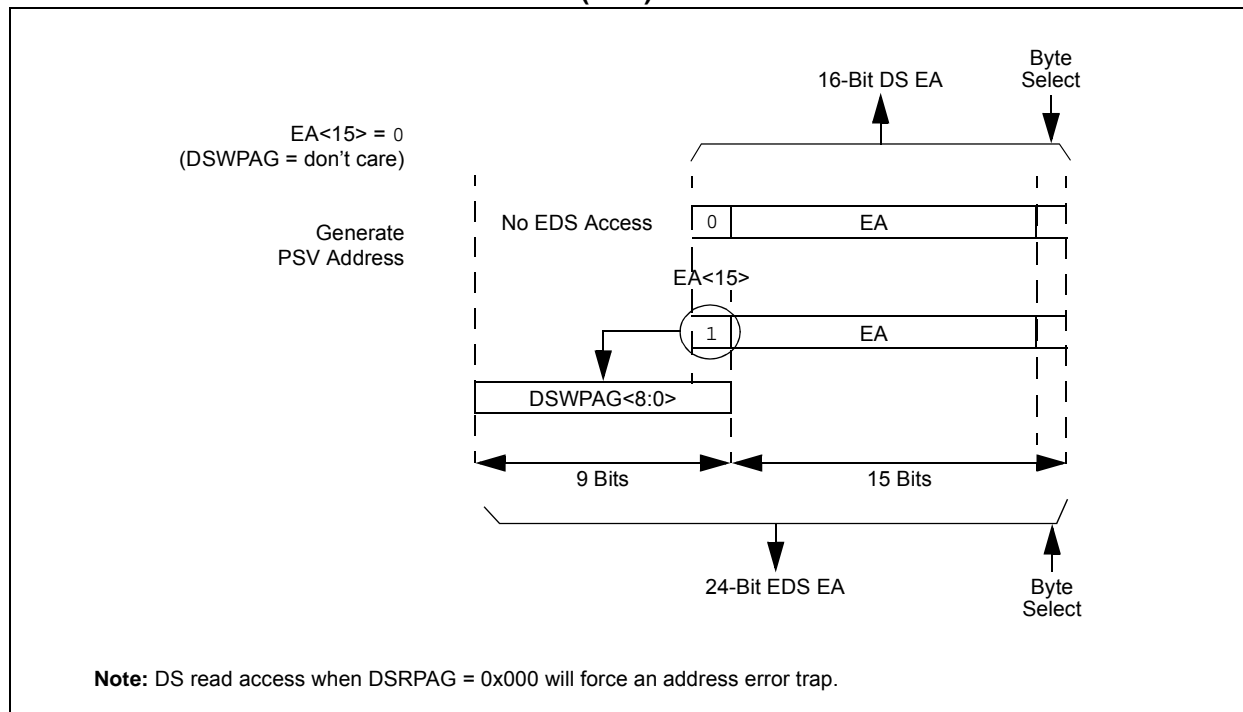
File Name	Addr.	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	All Resets
PMD1	0760	T5MD	T4MD	T3MD	T2MD	T1MD	—	—	—	I2C1MD	U2MD	U1MD	SPI2MD	SPI1MD	—	—	AD1MD	0000
PMD2	0762	—	—	—	—	IC4MD	IC3MD	IC2MD	IC1MD	—	—	—	—	OC4MD	OC3MD	OC2MD	OC1MD	0000
PMD3	0764	—	—	—	—	—	CMPMD	—	—	CRCMD	—	—	—	—	—	I2C2MD	—	0000
PMD4	0766	—	—	—	—	—	—	—	—	—	—	—	—	REFOMD	CTMUMD	—	—	0000
PMD6	076A	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
PMD7	076C	—	—	—	—	—	—	—	—	—	—	—	DMA0MD	PTGMD	—	—	—	0000
													DMA1MD					
													DMA2MD					
													DMA3MD					

Legend: — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

TABLE 4-38: PMD REGISTER MAP FOR PIC24EPXXXMC20X DEVICES ONLY

File Name	Addr.	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	All Resets
PMD1	0760	T5MD	T4MD	T3MD	T2MD	T1MD	QE11MD	PWMMD	—	I2C1MD	U2MD	U1MD	SPI2MD	SPI1MD	—	—	AD1MD	0000
PMD2	0762	—	—	—	—	IC4MD	IC3MD	IC2MD	IC1MD	—	—	—	—	OC4MD	OC3MD	OC2MD	OC1MD	0000
PMD3	0764	—	—	—	—	—	CMPMD	—	—	CRCMD	—	—	—	—	—	I2C2MD	—	0000
PMD4	0766	—	—	—	—	—	—	—	—	—	—	—	—	REFOMD	CTMUMD	—	—	0000
PMD6	076A	—	—	—	—	—	PWM3MD	PWM2MD	PWM1MD	—	—	—	—	—	—	—	—	0000
PMD7	076C	—	—	—	—	—	—	—	—	—	—	—	DMA0MD	PTGMD	—	—	—	0000
													DMA1MD					
													DMA2MD					
													DMA3MD					

Legend: — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

EXAMPLE 4-2: EXTENDED DATA SPACE (EDS) WRITE ADDRESS GENERATION

The paged memory scheme provides access to multiple 32-Kbyte windows in the EDS and PSV memory. The Data Space Page registers, DSxPAG, in combination with the upper half of the Data Space address, can provide up to 16 Mbytes of additional address space in the EDS and 8 Mbytes (DSRPAG only) of PSV address space. The paged data memory space is shown in Example 4-3.

The Program Space (PS) can be accessed with a DSRPAG of 0x200 or greater. Only reads from PS are supported using the DSRPAG. Writes to PS are not supported, so DSWPAG is dedicated to DS, including EDS only. The Data Space and EDS can be read from, and written to, using DSRPAG and DSWPAG, respectively.

REGISTER 8-5: DMAxSTBH: DMA CHANNEL x START ADDRESS REGISTER B (HIGH)

U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
—	—	—	—	—	—	—	—
bit 15							bit 8

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
STB<23:16>							
bit 7							bit 0

Legend:

R = Readable bit

W = Writable bit

U = Unimplemented bit, read as '0'

-n = Value at POR

'1' = Bit is set

'0' = Bit is cleared

x = Bit is unknown

bit 15-8 **Unimplemented:** Read as '0'bit 7-0 **STB<23:16>:** Secondary Start Address bits (source or destination)**REGISTER 8-6: DMAxSTBL: DMA CHANNEL x START ADDRESS REGISTER B (LOW)**

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
STB<15:8>							
bit 15							bit 8

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
STB<7:0>							
bit 7							bit 0

Legend:

R = Readable bit

W = Writable bit

U = Unimplemented bit, read as '0'

-n = Value at POR

'1' = Bit is set

'0' = Bit is cleared

x = Bit is unknown

bit 15-0 **STB<15:0>:** Secondary Start Address bits (source or destination)

9.1 CPU Clocking System

The dsPIC33EPXXXGP50X, dsPIC33EPXXXMC20X/50X and PIC24EPXXXGP/MC20X family of devices provides six system clock options:

- Fast RC (FRC) Oscillator
- FRC Oscillator with Phase Locked Loop (PLL)
- FRC Oscillator with Postscaler
- Primary (XT, HS or EC) Oscillator
- Primary Oscillator with PLL
- Low-Power RC (LPRC) Oscillator

Instruction execution speed or device operating frequency, FCY , is given by Equation 9-1.

EQUATION 9-1: DEVICE OPERATING FREQUENCY

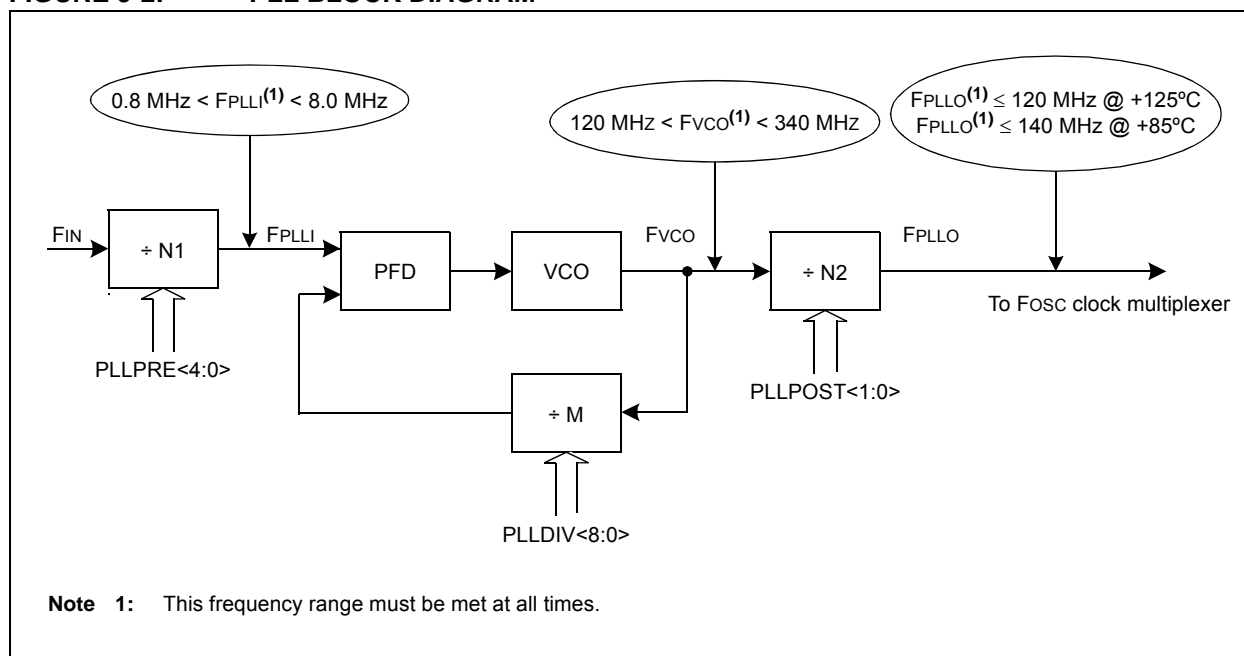
$$FCY = Fosc/2$$

Figure 9-2 is a block diagram of the PLL module.

Equation 9-2 provides the relationship between input frequency (F_{IN}) and output frequency (F_{PLLO}). In clock modes S1 and S3, when the PLL output is selected, $FOSC = F_{PLLO}$.

Equation 9-3 provides the relationship between input frequency (F_{IN}) and VCO frequency (F_{VCO}).

FIGURE 9-2: PLL BLOCK DIAGRAM



EQUATION 9-2: F_{PLLO} CALCULATION

$$F_{PLLO} = F_{IN} \times \left(\frac{M}{N1 \times N2} \right) = F_{IN} \times \left(\frac{(PLLDIV + 2)}{(PLLPRE + 2) \times 2(PLLPOST + 1)} \right)$$

Where:

$$N1 = PLLPRE + 2$$

$$N2 = 2 \times (PLLPOST + 1)$$

$$M = PLLDIV + 2$$

EQUATION 9-3: F_{VCO} CALCULATION

$$F_{VCO} = F_{IN} \times \left(\frac{M}{N1} \right) = F_{IN} \times \left(\frac{(PLLDIV + 2)}{(PLLPRE + 2)} \right)$$

17.2 QEI Control Registers

REGISTER 17-1: QE1CON: QE1 CONTROL REGISTER

R/W-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
QE1EN	—	QE1SIDL	PIMOD2 ⁽¹⁾	PIMOD1 ⁽¹⁾	PIMOD0 ⁽¹⁾	IMV1 ⁽²⁾	IMV0 ⁽²⁾
bit 15							bit 8

U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
—	INTDIV2 ⁽³⁾	INTDIV1 ⁽³⁾	INTDIV0 ⁽³⁾	CNTPOL	GATEN	CCM1	CCM0
bit 7							bit 0

Legend:

R = Readable bit W = Writable bit U = Unimplemented bit, read as '0'
-n = Value at POR '1' = Bit is set '0' = Bit is cleared x = Bit is unknown

- bit 15 **QE1EN:** Quadrature Encoder Interface Module Counter Enable bit
1 = Module counters are enabled
0 = Module counters are disabled, but SFRs can be read or written to
- bit 14 **Unimplemented:** Read as '0'
- bit 13 **QE1SIDL:** QE1 Stop in Idle Mode bit
1 = Discontinues module operation when device enters Idle mode
0 = Continues module operation in Idle mode
- bit 12-10 **PIMOD<2:0>:** Position Counter Initialization Mode Select bits⁽¹⁾
111 = Reserved
110 = Modulo Count mode for position counter
101 = Resets the position counter when the position counter equals QE1GEC register
100 = Second index event after home event initializes position counter with contents of QE1IC register
011 = First index event after home event initializes position counter with contents of QE1IC register
010 = Next index input event initializes the position counter with contents of QE1IC register
001 = Every index input event resets the position counter
000 = Index input event does not affect position counter
- bit 9 **IMV1:** Index Match Value for Phase B bit⁽²⁾
1 = Phase B match occurs when QEB = 1
0 = Phase B match occurs when QEB = 0
- bit 8 **IMV0:** Index Match Value for Phase A bit⁽²⁾
1 = Phase A match occurs when QEA = 1
0 = Phase A match occurs when QEA = 0
- bit 7 **Unimplemented:** Read as '0'

- Note 1:** When CCM<1:0> = 10 or 11, all of the QE1 counters operate as timers and the PIMOD<2:0> bits are ignored.
- 2:** When CCM<1:0> = 00, and QEA and QEB values match the Index Match Value (IMV), the POSCNTNTH and POSCNTL registers are reset. QEA/QEB signals used for the index match have swap and polarity values applied, as determined by the SWPAB and QEAPOL/QEBPOL bits.
- 3:** The selected clock rate should be at least twice the expected maximum quadrature count rate.

REGISTER 17-1: QE1CON: QE1 CONTROL REGISTER (CONTINUED)

- bit 6-4 **INTDIV<2:0>**: Timer Input Clock Prescale Select bits (interval timer, main timer (position counter), velocity counter and index counter internal clock divider select)⁽³⁾
- 111 = 1:128 prescale value
 - 110 = 1:64 prescale value
 - 101 = 1:32 prescale value
 - 100 = 1:16 prescale value
 - 011 = 1:8 prescale value
 - 010 = 1:4 prescale value
 - 001 = 1:2 prescale value
 - 000 = 1:1 prescale value
- bit 3 **CNTPOL**: Position and Index Counter/Timer Direction Select bit
- 1 = Counter direction is negative unless modified by external up/down signal
 - 0 = Counter direction is positive unless modified by external up/down signal
- bit 2 **GATEN**: External Count Gate Enable bit
- 1 = External gate signal controls position counter operation
 - 0 = External gate signal does not affect position counter/timer operation
- bit 1-0 **CCM<1:0>**: Counter Control Mode Selection bits
- 11 = Internal Timer mode with optional external count is selected
 - 10 = External clock count with optional external count is selected
 - 01 = External clock count with external up/down direction is selected
 - 00 = Quadrature Encoder Interface (x4 mode) Count mode is selected

- Note 1:** When CCM<1:0> = 10 or 11, all of the QE1 counters operate as timers and the PIMOD<2:0> bits are ignored.
- 2:** When CCM<1:0> = 00, and QEA and QEB values match the Index Match Value (IMV), the POSCNTH and POSCNTL registers are reset. QEA/QEB signals used for the index match have swap and polarity values applied, as determined by the SWPAB and QEAPOL/QEBPOL bits.
- 3:** The selected clock rate should be at least twice the expected maximum quadrature count rate.

REGISTER 17-19: INT1HLDH: INTERVAL 1 TIMER HOLD HIGH WORD REGISTER

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
INTHLD<31:24>							
bit 15				bit 8			

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
INTHLD<23:16>							
bit 7				bit 0			

Legend:

R = Readable bit W = Writable bit U = Unimplemented bit, read as '0'
 -n = Value at POR '1' = Bit is set '0' = Bit is cleared x = Bit is unknown

bit 15-0 **INTHLD<31:16>**: Hold Register for Reading and Writing INT1TMRH bits

REGISTER 17-20: INT1HLDL: INTERVAL 1 TIMER HOLD LOW WORD REGISTER

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
INTHLD<15:8>							
bit 15				bit 8			

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
INTHLD<7:0>							
bit 7				bit 0			

Legend:

R = Readable bit W = Writable bit U = Unimplemented bit, read as '0'
 -n = Value at POR '1' = Bit is set '0' = Bit is cleared x = Bit is unknown

bit 15-0 **INTHLD<15:0>**: Hold Register for Reading and Writing INT1TMRL bits

19.2 I²C Control Registers

REGISTER 19-1: I2CxCON: I2Cx CONTROL REGISTER

R/W-0	U-0	R/W-0	R/W-1, HC	R/W-0	R/W-0	R/W-0	R/W-0
I2CEN	—	I2CSIDL	SCLREL	IPMIEN ⁽¹⁾	A10M	DISSLW	SMEN
bit 15							bit 8

R/W-0	R/W-0	R/W-0	R/W-0, HC	R/W-0, HC	R/W-0, HC	R/W-0, HC	R/W-0, HC
GCEN	STREN	ACKDT	ACKEN	RCEN	PEN	RSEN	SEN
bit 7							bit 0

Legend:	HC = Hardware Clearable bit		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

- bit 15 **I2CEN:** I2Cx Enable bit
1 = Enables the I2Cx module and configures the SDAx and SCLx pins as serial port pins
0 = Disables the I2Cx module; all I²C™ pins are controlled by port functions
- bit 14 **Unimplemented:** Read as '0'
- bit 13 **I2CSIDL:** I2Cx Stop in Idle Mode bit
1 = Discontinues module operation when device enters an Idle mode
0 = Continues module operation in Idle mode
- bit 12 **SCLREL:** SCLx Release Control bit (when operating as I²C slave)
1 = Releases SCLx clock
0 = Holds SCLx clock low (clock stretch)
If STREN = 1:
Bit is R/W (i.e., software can write '0' to initiate stretch and write '1' to release clock). Hardware is clear at the beginning of every slave data byte transmission. Hardware is clear at the end of every slave address byte reception. Hardware is clear at the end of every slave data byte reception.
If STREN = 0:
Bit is R/S (i.e., software can only write '1' to release clock). Hardware is clear at the beginning of every slave data byte transmission. Hardware is clear at the end of every slave address byte reception.
- bit 11 **IPMIEN:** Intelligent Peripheral Management Interface (IPMI) Enable bit⁽¹⁾
1 = IPMI mode is enabled; all addresses are Acknowledged
0 = IPMI mode disabled
- bit 10 **A10M:** 10-Bit Slave Address bit
1 = I2CxADD is a 10-bit slave address
0 = I2CxADD is a 7-bit slave address
- bit 9 **DISSLW:** Disable Slew Rate Control bit
1 = Slew rate control is disabled
0 = Slew rate control is enabled
- bit 8 **SMEN:** SMBus Input Levels bit
1 = Enables I/O pin thresholds compliant with SMBus specification
0 = Disables SMBus input thresholds
- bit 7 **GCEN:** General Call Enable bit (when operating as I²C slave)
1 = Enables interrupt when a general call address is received in I2CxRSR (module is enabled for reception)
0 = General call address disabled

Note 1: When performing master operations, ensure that the IPMIEN bit is set to '0'.

REGISTER 19-2: I2CxSTAT: I2Cx STATUS REGISTER

R-0, HSC	R-0, HSC	U-0	U-0	U-0	R/C-0, HS	R-0, HSC	R-0, HSC
ACKSTAT	TRSTAT	—	—	—	BCL	GCSTAT	ADD10
bit 15						bit 8	

R/C-0, HS	R/C-0, HS	R-0, HSC	R/C-0, HSC	R/C-0, HSC	R-0, HSC	R-0, HSC	R-0, HSC
IWCOL	I2COV	D_A	P	S	R_W	RBF	TBF
bit 7						bit 0	

Legend:	C = Clearable bit	HS = Hardware Settable bit	HSC = Hardware Settable/Clearable bit
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

- bit 15 **ACKSTAT:** Acknowledge Status bit (when operating as I²C™ master, applicable to master transmit operation)
1 = NACK received from slave
0 = ACK received from slave
Hardware is set or clear at the end of slave Acknowledge.
- bit 14 **TRSTAT:** Transmit Status bit (when operating as I²C master, applicable to master transmit operation)
1 = Master transmit is in progress (8 bits + ACK)
0 = Master transmit is not in progress
Hardware is set at the beginning of master transmission. Hardware is clear at the end of slave Acknowledge.
- bit 13-11 **Unimplemented:** Read as '0'
- bit 10 **BCL:** Master Bus Collision Detect bit
1 = A bus collision has been detected during a master operation
0 = No bus collision detected
Hardware is set at detection of a bus collision.
- bit 9 **GCSTAT:** General Call Status bit
1 = General call address was received
0 = General call address was not received
Hardware is set when address matches general call address. Hardware is clear at Stop detection.
- bit 8 **ADD10:** 10-Bit Address Status bit
1 = 10-bit address was matched
0 = 10-bit address was not matched
Hardware is set at the match of the 2nd byte of the matched 10-bit address. Hardware is clear at Stop detection.
- bit 7 **IWCOL:** I2Cx Write Collision Detect bit
1 = An attempt to write to the I2CxTRN register failed because the I²C module is busy
0 = No collision
Hardware is set at the occurrence of a write to I2CxTRN while busy (cleared by software).
- bit 6 **I2COV:** I2Cx Receive Overflow Flag bit
1 = A byte was received while the I2CxRCV register was still holding the previous byte
0 = No overflow
Hardware is set at an attempt to transfer I2CxRSR to I2CxRCV (cleared by software).
- bit 5 **D_A:** Data/Address bit (when operating as I²C slave)
1 = Indicates that the last byte received was data
0 = Indicates that the last byte received was a device address
Hardware is clear at a device address match. Hardware is set by reception of a slave byte.
- bit 4 **P:** Stop bit
1 = Indicates that a Stop bit has been detected last
0 = Stop bit was not detected last
Hardware is set or clear when a Start, Repeated Start or Stop is detected.

BUFFER 21-3: ECAN™ MESSAGE BUFFER WORD 2

R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x
EID5	EID4	EID3	EID2	EID1	EID0	RTR	RB1
bit 15							bit 8

U-x	U-x	U-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x
—	—	—	RB0	DLC3	DLC2	DLC1	DLC0
bit 7							bit 0

Legend:

R = Readable bit W = Writable bit U = Unimplemented bit, read as '0'
-n = Value at POR '1' = Bit is set '0' = Bit is cleared x = Bit is unknown

- bit 15-10 **EID<5:0>**: Extended Identifier bits
- bit 9 **RTR**: Remote Transmission Request bit
When IDE = 1:
1 = Message will request remote transmission
0 = Normal message
When IDE = 0:
The RTR bit is ignored.
- bit 8 **RB1**: Reserved Bit 1
User must set this bit to '0' per CAN protocol.
- bit 7-5 **Unimplemented**: Read as '0'
- bit 4 **RB0**: Reserved Bit 0
User must set this bit to '0' per CAN protocol.
- bit 3-0 **DLC<3:0>**: Data Length Code bits

BUFFER 21-4: ECAN™ MESSAGE BUFFER WORD 3

R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x
Byte 1							
bit 15							bit 8

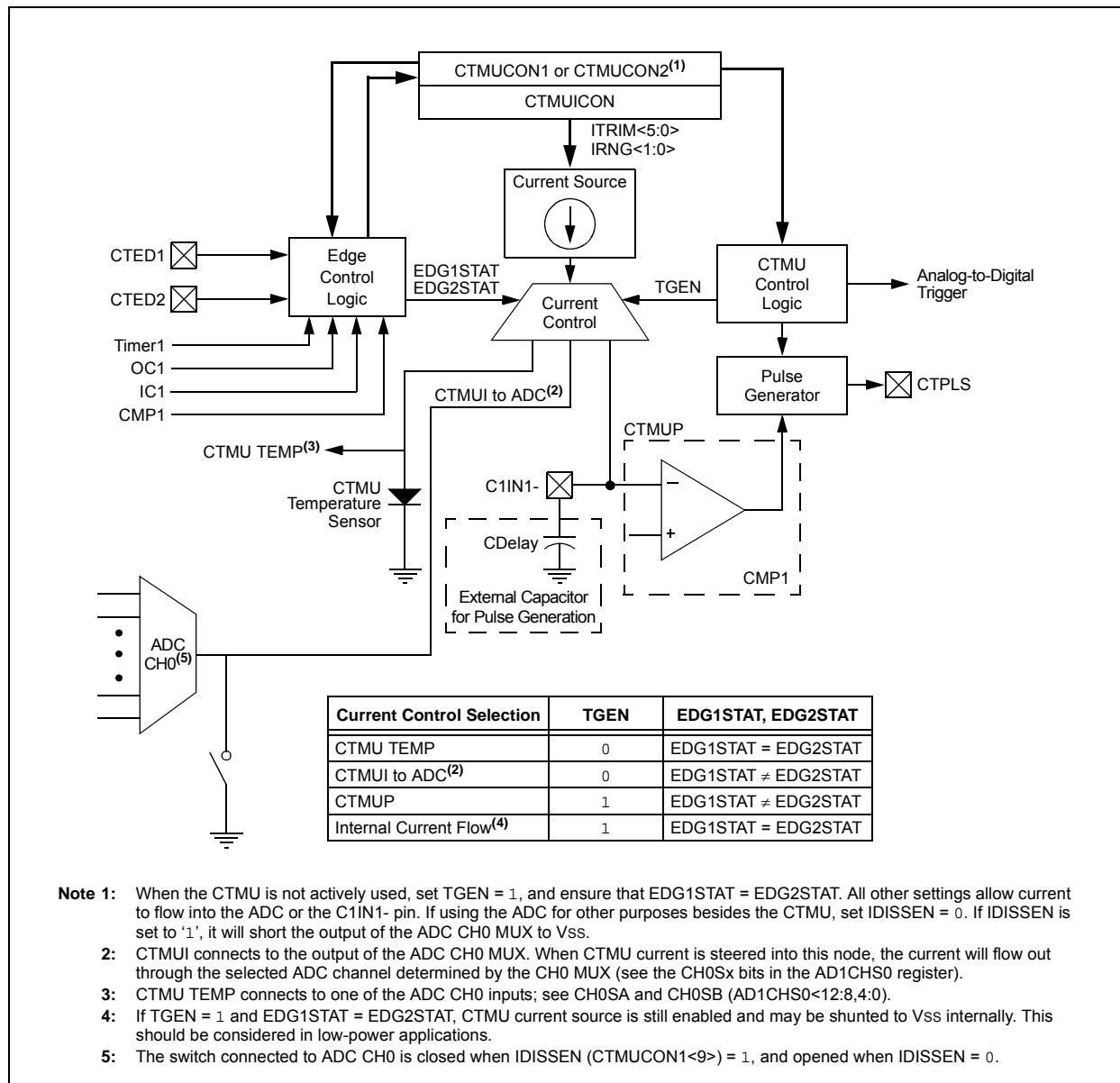
R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x
Byte 0							
bit 7							bit 0

Legend:

R = Readable bit W = Writable bit U = Unimplemented bit, read as '0'
-n = Value at POR '1' = Bit is set '0' = Bit is cleared x = Bit is unknown

- bit 15-8 **Byte 1<15:8>**: ECAN Message Byte 1 bits
- bit 7-0 **Byte 0<7:0>**: ECAN Message Byte 0 bits

FIGURE 22-1: CTMU BLOCK DIAGRAM



22.1 CTMU Resources

Many useful resources are provided on the main product page of the Microchip web site for the devices listed in this data sheet. This product page, which can be accessed using this link, contains the latest updates and additional information.

Note: In the event you are not able to access the product page using the link above, enter this URL in your browser:
<http://www.microchip.com/wwwproducts/Devices.aspx?dDocName=en555464>

22.1.1 KEY RESOURCES

- “Charge Time Measurement Unit (CTMU)” (DS70661) in the “dsPIC33/PIC24 Family Reference Manual”
- Code Samples
- Application Notes
- Software Libraries
- Webinars
- All Related “dsPIC33/PIC24 Family Reference Manual” Sections
- Development Tools

NOTES:

27.2 User ID Words

dsPIC33EPXXXGP50X, dsPIC33EPXXXMC20X/50X and PIC24EPXXXGP/MC20X devices contain four User ID Words, located at addresses, 0x800FF8 through 0x800FFE. The User ID Words can be used for storing product information such as serial numbers, system manufacturing dates, manufacturing lot numbers and other application-specific information.

The User ID Words register map is shown in Table 27-3.

TABLE 27-3: USER ID WORDS REGISTER MAP

File Name	Address	Bits 23-16	Bits 15-0
FUID0	0x800FF8	—	UID0
FUID1	0x800FFA	—	UID1
FUID2	0x800FFC	—	UID2
FUID3	0x800FFE	—	UID3

Legend: — = unimplemented, read as '1'.

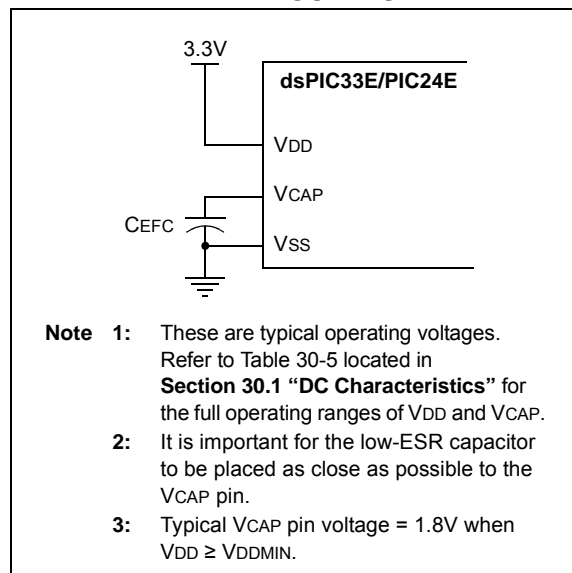
27.3 On-Chip Voltage Regulator

All of the dsPIC33EPXXXGP50X, dsPIC33EPXXXMC20X/50X and PIC24EPXXXGP/MC20X devices power their core digital logic at a nominal 1.8V. This can create a conflict for designs that are required to operate at a higher typical voltage, such as 3.3V. To simplify system design, all devices in the dsPIC33EPXXXGP50X, dsPIC33EPXXXMC20X/50X and PIC24EPXXXGP/MC20X family incorporate an on-chip regulator that allows the device to run its core logic from VDD.

The regulator provides power to the core from the other VDD pins. A low-ESR (less than 1 Ohm) capacitor (such as tantalum or ceramic) must be connected to the VCAP pin (Figure 27-1). This helps to maintain the stability of the regulator. The recommended value for the filter capacitor is provided in Table 30-5 located in Section 30.0 "Electrical Characteristics".

Note: It is important for the low-ESR capacitor to be placed as close as possible to the VCAP pin.

FIGURE 27-1: CONNECTIONS FOR THE ON-CHIP VOLTAGE REGULATOR^(1,2,3)



27.4 Brown-out Reset (BOR)

The Brown-out Reset (BOR) module is based on an internal voltage reference circuit that monitors the regulated supply voltage, VCAP. The main purpose of the BOR module is to generate a device Reset when a brown-out condition occurs. Brown-out conditions are generally caused by glitches on the AC mains (for example, missing portions of the AC cycle waveform due to bad power transmission lines or voltage sags due to excessive current draw when a large inductive load is turned on).

A BOR generates a Reset pulse, which resets the device. The BOR selects the clock source, based on the device Configuration bit values (FNOSC<2:0> and POSCMD<1:0>).

If an oscillator mode is selected, the BOR activates the Oscillator Start-up Timer (OST). The system clock is held until OST expires. If the PLL is used, the clock is held until the LOCK bit (OSCCON<5>) is '1'.

Concurrently, the PWRT Time-out (TPWRT) is applied before the internal Reset is released. If TPWRT = 0 and a crystal oscillator is being used, then a nominal delay of TFSCM is applied. The total delay in this case is TFSCM. Refer to Parameter SY35 in Table 30-22 of Section 30.0 "Electrical Characteristics" for specific TFSCM values.

The BOR status bit (RCON<1>) is set to indicate that a BOR has occurred. The BOR circuit continues to operate while in Sleep or Idle modes and resets the device should VDD fall below the BOR threshold voltage.

TABLE 30-54: OP AMP/COMPARATOR VOLTAGE REFERENCE SETTling TIME SPECIFICATIONS

AC CHARACTERISTICS			Standard Operating Conditions (see Note 2): 3.0V to 3.6V (unless otherwise stated) Operating temperature -40°C ≤ TA ≤ +85°C for Industrial -40°C ≤ TA ≤ +125°C for Extended				
Param.	Symbol	Characteristic	Min.	Typ.	Max.	Units	Conditions
VR310	TSET	Settling Time	—	1	10	μs	(Note 1)

Note 1: Settling time is measured while CVRR = 1 and CVR<3:0> bits transition from '0000' to '1111'.

2: Device is functional at VBORMIN < VDD < VDDMIN, but will have degraded performance. Device functionality is tested, but not characterized. Analog modules (ADC, op amp/comparator and comparator voltage reference) may have degraded performance. Refer to Parameter BO10 in Table 30-13 for the minimum and maximum BOR values.

TABLE 30-55: OP AMP/COMPARATOR VOLTAGE REFERENCE SPECIFICATIONS

DC CHARACTERISTICS			Standard Operating Conditions (see Note 1): 3.0V to 3.6V (unless otherwise stated) Operating temperature -40°C ≤ TA ≤ +85°C for Industrial -40°C ≤ TA ≤ +125°C for Extended				
Param No.	Symbol	Characteristics	Min.	Typ.	Max.	Units	Conditions
VRD310	CVRES	Resolution	CVRSRC/24	—	CVRSRC/32	LSb	
VRD311	CVRAA	Absolute Accuracy ⁽²⁾	—	±25	—	mV	CVRSRC = 3.3V
VRD313	CVRSRC	Input Reference Voltage	0	—	AVDD + 0.3	V	
VRD314	CVRROUT	Buffer Output Resistance ⁽²⁾	—	1.5k	—	Ω	

Note 1: Device is functional at VBORMIN < VDD < VDDMIN, but will have degraded performance. Device functionality is tested, but not characterized. Analog modules (ADC, op amp/comparator and comparator voltage reference) may have degraded performance. Refer to Parameter BO10 in Table 30-13 for the minimum and maximum BOR values.

2: Parameter is characterized but not tested in manufacturing.

33.1 Package Marking Information (Continued)

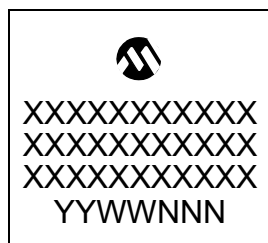
48-Lead UQFN (6x6x0.5 mm)



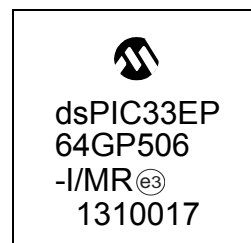
Example



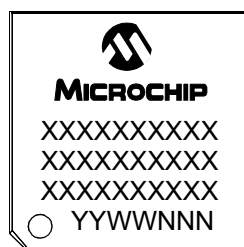
64-Lead QFN (9x9x0.9 mm)



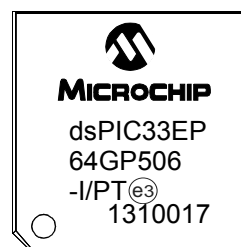
Example



64-Lead TQFP (10x10x1 mm)



Example



INDEX

A

Absolute Maximum Ratings	401
AC Characteristics	413, 471
10-Bit ADC Conversion Requirements	465
12-Bit ADC Conversion Requirements	463
ADC Module	459
ADC Module (10-Bit Mode)	461, 473
ADC Module (12-Bit Mode)	460, 473
Capacitive Loading Requirements on Output Pins	413
DMA Module Requirements	465
ECANx I/O Requirements	454
External Clock	414
High-Speed PWMx Requirements	422
I/O Timing Requirements	416
I2Cx Bus Data Requirements (Master Mode)	451
I2Cx Bus Data Requirements (Slave Mode)	453
Input Capture x Requirements	420
Internal FRC Accuracy	415
Internal LPRC Accuracy	415
Internal RC Accuracy	472
Load Conditions	413, 471
OCx/PWMx Mode Requirements	421
Op Amp/Comparator Voltage Reference Settling Time Specifications	457
Output Compare x Requirements	421
PLL Clock	415, 471
QE1 External Clock Requirements	423
QE1 Index Pulse Requirements	425
Quadrature Decoder Requirements	424
Reset, Watchdog Timer, Oscillator Start-up Timer, Power-up Timer Requirements	417
SPI1 Master Mode (Full-Duplex, CKE = 0, CKP = x, SMP = 1) Requirements	441
SPI1 Master Mode (Full-Duplex, CKE = 1, CKP = x, SMP = 1) Requirements	440
SPI1 Master Mode (Half-Duplex, Transmit Only) Requirements	439
SPI1 Maximum Data/Clock Rate Summary	438
SPI1 Slave Mode (Full-Duplex, CKE = 0, CKP = 0, SMP = 0) Requirements	449
SPI1 Slave Mode (Full-Duplex, CKE = 0, CKP = 1, SMP = 0) Requirements	447
SPI1 Slave Mode (Full-Duplex, CKE = 1, CKP = 0, SMP = 0) Requirements	443
SPI1 Slave Mode (Full-Duplex, CKE = 1, CKP = 1, SMP = 0) Requirements	445
SPI2 Master Mode (Full-Duplex, CKE = 0, CKP = x, SMP = 1) Requirements	429
SPI2 Master Mode (Full-Duplex, CKE = 1, CKP = x, SMP = 1) Requirements	428
SPI2 Master Mode (Half-Duplex, Transmit Only) Requirements	427
SPI2 Maximum Data/Clock Rate Summary	426
SPI2 Slave Mode (Full-Duplex, CKE = 0, CKP = 0, SMP = 0) Requirements	437
SPI2 Slave Mode (Full-Duplex, CKE = 0, CKP = 1, SMP = 0) Requirements	435
SPI2 Slave Mode (Full-Duplex, CKE = 1, CKP = 0, SMP = 0) Requirements	431
SPI2 Slave Mode (Full-Duplex, CKE = 1, CKP = 1, SMP = 0) Requirements	433

Timer1 External Clock Requirements	418
Timer2/Timer4 External Clock Requirements	419
Timer3/Timer5 External Clock Requirements	419
UARTx I/O Requirements	454
ADC	
Control Registers	325
Helpful Tips	324
Key Features	321
Resources	324
Arithmetic Logic Unit (ALU)	44
Assembler	
MPASM Assembler	398
B	
Bit-Reversed Addressing	115
Example	116
Implementation	115
Sequence Table (16-Entry)	116
Block Diagrams	
Data Access from Program Space	
Address Generation	117
16-Bit Timer1 Module	203
ADC Conversion Clock Period	323
ADC with Connection Options for ANx Pins and Op Amps	322
Arbiter Architecture	110
BEMF Voltage Measurement Using ADC	34
Boost Converter Implementation	32
CALL Stack Frame	111
Comparator (Module 4)	356
Connections for On-Chip Voltage Regulator	384
CPU Core	36
CRC Module	373
CRC Shift Engine	374
CTMU Module	316
Digital Filter Interconnect	357
DMA Controller	141
DMA Controller Module	139
dsPIC33EPXXXGP50X, dsPIC33EPXXXMC20X/50X and PIC24EPXXXGP/MC20X	25
ECAN Module	288
EDS Read Address Generation	105
EDS Write Address Generation	106
Example of MCLR Pin Connections	30
High-Speed PWMx Architectural Overview	227
High-Speed PWMx Register Interconnection	228
I2Cx Module	274
Input Capture x	213
Interleaved PFC	34
Multiphase Synchronous Buck Converter	33
Multiplexing Remappable Output for RPN	180
Op Amp Configuration A	358
Op Amp Configuration B	359
Op Amp/Comparator Voltage Reference Module	356
Op Amp/Comparator x (Modules 1, 2, 3)	355
Oscillator System	153
Output Compare x Module	219
PLL	154
Programmer's Model	38
PTG Module	338
Quadrature Encoder Interface	250
Recommended Minimum Connection	30