



Welcome to E-XFL.COM

What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "<u>Embedded -</u> <u>Microcontrollers</u>"

Details

E·XFI

Product Status	Obsolete
Core Processor	PIC
Core Size	16-Bit
Speed	60 MIPs
Connectivity	I ² C, IrDA, LINbus, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, DMA, POR, PWM, WDT
Number of I/O	21
Program Memory Size	256KB (85.5K x 24)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	16K x 16
Voltage - Supply (Vcc/Vdd)	3V ~ 3.6V
Data Converters	A/D 6x10b/12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 125°C (TA)
Mounting Type	Surface Mount
Package / Case	28-SOIC (0.295", 7.50mm Width)
Supplier Device Package	28-SOIC
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/pic24ep256gp202t-e-so

Email: info@E-XFL.COM

Address: Room A, 16/F, Full Win Commercial Centre, 573 Nathan Road, Mongkok, Hong Kong

1.0 DEVICE OVERVIEW

- Note 1: This data sheet summarizes the features of the dsPIC33EPXXXGP50X, dsPIC33EPXXXMC20X/50X and PIC24EPXXXGP/MC20X families of devices. It is not intended to be a comprehensive resource. To complement the information in this data sheet, refer to the related section of the "dsPIC33/ PIC24 Family Reference Manual", which is available from the Microchip web site (www.microchip.com)
 - Some registers and associated bits described in this section may not be available on all devices. Refer to Section 4.0 "Memory Organization" in this data sheet for device-specific register and bit information.

This document contains device-specific information for the dsPIC33EPXXXGP50X, dsPIC33EPXXXMC20X/ 50X and PIC24EPXXXGP/MC20X Digital Signal Controller (DSC) and Microcontroller (MCU) devices.

dsPIC33EPXXXMC20X/50X and dsPIC33EPXXXGP50X devices contain extensive Digital Signal Processor (DSP) functionality with a high-performance, 16-bit MCU architecture.

Figure 1-1 shows a general block diagram of the core and peripheral modules. Table 1-1 lists the functions of the various pins shown in the pinout diagrams.

FIGURE 1-1: dsPIC33EPXXXGP50X, dsPIC33EPXXXMC20X/50X AND PIC24EPXXXGP/MC20X BLOCK DIAGRAM



Pin Name ⁽⁴⁾	Pin Type	Buffer Type	PPS	Description
AN0-AN15	I	Analog	No	Analog input channels.
CLKI	I	ST/ CMOS	No	External clock source input. Always associated with OSC1 pin function.
CLKO	0	_	No	Oscillator crystal output. Connects to crystal or resonator in Crystal Oscillator mode. Optionally functions as CLKO in RC and EC modes. Always associated with OSC2 pin function.
OSC1 OSC2	I I/O	ST/ CMOS	No No	Oscillator crystal input. ST buffer when configured in RC mode; CMOS otherwise. Oscillator crystal output. Connects to crystal or resonator in Crystal
				Oscillator mode. Optionally functions as CLKO in RC and EC modes.
REFCLKO	0		Yes	Reference clock output.
IC1-IC4	Ι	ST	Yes	Capture Inputs 1 through 4.
OCFA	I	ST	Yes	Compare Fault A input (for Compare channels).
		SI	N0 Voc	Compare Fault B input (for Compare channels).
		— ст	No	External Interrunt 0
INT1		ST	Yes	External Interrupt 1.
INT2	1	ST	Yes	External Interrupt 2.
RA0-RA4, RA7-RA12	I/O	ST	No	PORTA is a bidirectional I/O port.
RB0-RB15	I/O	ST	No	PORTB is a bidirectional I/O port.
RC0-RC13, RC15	I/O	ST	No	PORTC is a bidirectional I/O port.
RD5, RD6, RD8	I/O	ST	No	PORTD is a bidirectional I/O port.
RE12-RE15	I/O	ST	No	PORTE is a bidirectional I/O port.
RF0, RF1	I/O	ST	No	PORTF is a bidirectional I/O port.
RG6-RG9	I/O	ST	No	PORTG is a bidirectional I/O port.
T1CK	Ι	ST	No	Timer1 external clock input.
T2CK	I	ST	Yes	Timer2 external clock input.
T3CK		ST	No	Timer3 external clock input.
T4CK		ST	NO No	Timer4 external clock input.
CTPLS	0	ST	No	
CTED1	I	ST	No	CTMU External Edge Input 1.
CTED2	I.	ST	No	CTMU External Edge Input 2.
U1CTS	Ι	ST	No	UART1 Clear-To-Send.
U1RTS	0		No	UART1 Ready-To-Send.
U1RX		ST	Yes	UART1 receive.
		— ст	Yes	UART1 transmit.
				D = D = D = D = D = D = D = D = D = D =
Legend: $CMOS = CI ST = Schmi$	viUS CO	ier input v	input with CN	or output Analog = Analog input $P = Power$ MOS levels $O = Output$ $I = Input$
PPS = Peri	oheral l	Pin Selec	t.	TTL = TTL input buffer

TABLE 1-1:PINOUT I/O DESCRIPTIONS

Note 1: This pin is available on dsPIC33EPXXXMC20X/50X and PIC24EPXXXMC20X devices only.

2: This pin is available on dsPIC33EPXXXGP/MC50X devices only.

3: This is the default Fault on Reset for dsPIC33EPXXXMC20X/50X and PIC24EPXXXMC20X devices. See Section 16.0 "High-Speed PWM Module (dsPIC33EPXXXMC20X/50X and PIC24EPXXXMC20X Devices Only)" for more information.

4: Not all pins are available in all packages variants. See the "Pin Diagrams" section for pin availability.

5: There is an internal pull-up resistor connected to the TMS pin when the JTAG interface is active. See the JTAGEN bit field in Table 27-2.

2.7 Oscillator Value Conditions on Device Start-up

If the PLL of the target device is enabled and configured for the device start-up oscillator, the maximum oscillator source frequency must be limited to 3 MHz < F_{IN} < 5.5 MHz to comply with device PLL start-up conditions. This means that if the external oscillator frequency is outside this range, the application must start-up in the FRC mode first. The default PLL settings after a POR with an oscillator frequency outside this range will violate the device operating speed.

Once the device powers up, the application firmware can initialize the PLL SFRs, CLKDIV and PLLFBD, to a suitable value, and then perform a clock switch to the Oscillator + PLL clock source. Note that clock switching must be enabled in the device Configuration Word.

2.8 Unused I/Os

Unused I/O pins should be configured as outputs and driven to a logic low state.

Alternatively, connect a 1k to 10k resistor between Vss and unused pins, and drive the output to logic low.

2.9 Application Examples

- · Induction heating
- Uninterruptable Power Supplies (UPS)
- DC/AC inverters
- · Compressor motor control
- · Washing machine 3-phase motor control
- BLDC motor control
- · Automotive HVAC, cooling fans, fuel pumps
- Stepper motor control
- · Audio and fluid sensor monitoring
- · Camera lens focus and stability control
- Speech (playback, hands-free kits, answering machines, VoIP)
- Consumer audio
- Industrial and building control (security systems and access control)
- · Barcode reading
- Networking: LAN switches, gateways
- Data storage device management
- · Smart cards and smart card readers

Examples of typical application connections are shown in Figure 2-4 through Figure 2-8.

FIGURE 2-4: BOOST CONVERTER IMPLEMENTATION



REGISTER 3-1: SR: CPU STATUS REGISTER (CONTINUED)

bit 7-5	IPL<2:0>: CPU Interrupt Priority Level Status bits ^(2,3) 111 = CPU Interrupt Priority Level is 7 (15); user interrupts are disabled 110 = CPU Interrupt Priority Level is 6 (14) 101 = CPU Interrupt Priority Level is 5 (13) 100 = CPU Interrupt Priority Level is 4 (12) 011 = CPU Interrupt Priority Level is 3 (11) 010 = CPU Interrupt Priority Level is 2 (10) 001 = CPU Interrupt Priority Level is 1 (9) 000 = CPU Interrupt Priority Level is 0 (8)
bit 4	RA: REPEAT Loop Active bit 1 = REPEAT loop in progress 0 = REPEAT loop not in progress
bit 3	N: MCU ALU Negative bit 1 = Result was negative 0 = Result was non-negative (zero or positive)
bit 2	 OV: MCU ALU Overflow bit This bit is used for signed arithmetic (2's complement). It indicates an overflow of the magnitude that causes the sign bit to change state. 1 = Overflow occurred for signed arithmetic (in this arithmetic operation) 0 = No overflow occurred
bit 1	 Z: MCU ALU Zero bit 1 = An operation that affects the Z bit has set it at some time in the past 0 = The most recent operation that affects the Z bit has cleared it (i.e., a non-zero result)
bit 0	C: MCU ALU Carry/Borrow bit 1 = A carry-out from the Most Significant bit of the result occurred 0 = No carry-out from the Most Significant bit of the result occurred
Note 1: 2:	This bit is available on dsPIC33EPXXXMC20X/50X and dsPIC33EPXXXGP50X devices only. The IPL<2:0> bits are concatenated with the IPL<3> bit (CORCON<3>) to form the CPU Interrupt Priority

- Level. The value in parentheses indicates the IPL, if IPL<3> = 1. User interrupts are disabled when IPL<3> = 1.
 3: The IPL<2:0> Status bits are read-only when the NSTDIS bit (INTCON1<15>) = 1.
- 4: A data write to the SR register can modify the SA and SB bits by either a data write to SA and SB or by clearing the SAB bit. To avoid a possible SA or SB bit write race condition, the SA and SB bits should not be modified using bit operations.

IADLE 4	-10:	QEII	REGI			SFICSSE		5208/50/		CZ4EP/		ZUX DE	VICES U					
File Name	Addr.	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	All Resets
QEI1CON	01C0	QEIEN	—	QEISIDL	ISIDL PIMOD<2:0> IMV<1:0> — INTDIV<2:0> CNTPOL GATEN CCM					<1:0>	0000							
QEI1IOC	01C2	QCAPEN	FLTREN		QFDIV<2:0>		OUTFN	NC<1:0>	SWPAB	HOMPOL	IDXPOL	QEBPOL	QEAPOL	HOME	INDEX	QEB	QEA	000x
QEI1STAT	01C4	_	—	PCHEQIRQ	PCHEQIEN	PCLEQIRQ	PCLEQIEN	POSOVIRQ	POSOVIEN	PCIIRQ	PCIIEN	VELOVIRQ	VELOVIEN	HOMIRQ	HOMIEN	IDXIRQ	IDXIEN	0000
POS1CNTL	01C6								POSCNT<15	0>								0000
POS1CNTH	01C8							F	POSCNT<31:	16>								0000
POS1HLD	01CA								POSHLD<15	0>								0000
VEL1CNT	01CC								VELCNT<15:	0>								0000
INT1TMRL	01CE								INTTMR<15:	0>								0000
INT1TMRH	01D0								INTTMR<31:1	6>								0000
INT1HLDL	01D2								INTHLD<15:)>								0000
INT1HLDH	01D4								INTHLD<31:1	6>								0000
INDX1CNTL	01D6								INDXCNT<15	:0>								0000
INDX1CNTH	01D8							I	NDXCNT<31:	16>								0000
INDX1HLD	01DA								INDXHLD<15	:0>								0000
QEI1GECL	01DC								QEIGEC<15:	0>								0000
QEI1ICL	01DC								QEIIC<15:0	>								0000
QEI1GECH	01DE								QEIGEC<31:	16>								0000
QEI1ICH	01DE								QEIIC<31:16	}>								0000
QEI1LECL	01E0								QEILEC<15:)>								0000
QEI1LECH	01E2								QEILEC<31:1	6>								0000

TABLE 4-16: QEI1 REGISTER MAP FOR dsPIC33EPXXXMC20X/50X AND PIC24EPXXXMC20X DEVICES ONLY

Legend: x = unknown value on Reset, — = unimplemented, read as '0'. Reset values are shown in hexadecimal.



8.1 DMA Resources

Many useful resources are provided on the main product page of the Microchip web site for the devices listed in this data sheet. This product page, which can be accessed using this link, contains the latest updates and additional information.

Note:	In the event you are not able to access the
	product page using the link above, enter
	this URL in your browser:
	http://www.microchip.com/wwwproducts/
	Devices.aspx?dDocName=en555464

8.1.1 KEY RESOURCES

- Section 22. "Direct Memory Access (DMA)" (DS70348) in the "dsPIC33/PIC24 Family Reference Manual"
- Code Samples
- · Application Notes
- Software Libraries
- Webinars
- All Related "dsPIC33/PIC24 Family Reference Manual" Sections
- Development Tools

8.2 DMAC Registers

Each DMAC Channel x (where x = 0 through 3) contains the following registers:

- 16-Bit DMA Channel Control register (DMAxCON)
- 16-Bit DMA Channel IRQ Select register (DMAxREQ)
- 32-Bit DMA RAM Primary Start Address register (DMAxSTA)
- 32-Bit DMA RAM Secondary Start Address register (DMAxSTB)
- 16-Bit DMA Peripheral Address register (DMAxPAD)
- 14-Bit DMA Transfer Count register (DMAxCNT)

Additional status registers (DMAPWC, DMARQC, DMAPPS, DMALCA and DSADR) are common to all DMAC channels. These status registers provide information on write and request collisions, as well as on last address and channel access information.

The interrupt flags (DMAxIF) are located in an IFSx register in the interrupt controller. The corresponding interrupt enable control bits (DMAxIE) are located in an IECx register in the interrupt controller, and the corresponding interrupt priority control bits (DMAxIP) are located in an IPCx register in the interrupt controller.

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	U-0	U-0	U-0
CHEN	SIZE	DIR	HALF	NULLW	_	—	—
bit 15							bit 8
U-0	U-0	R/W-0	R/W-0	U-0	U-0	R/W-0	R/W-0
		AMODE1	AMODE0			MODE1	MODE0
bit 7							bit 0
Legend:			,			(0)	
R = Readable	bit	W = Writable	bit		mented bit, read	as '0'	
-n = Value at F	POR	'1' = Bit is set		0^{\prime} = Bit is cle	eared	x = Bit is unkn	IOWN
bit 15		Channel Enabl	o hit				
bit 15	1 = Channel	is enabled					
	0 = Channel	is disabled					
bit 14	SIZE: DMA D	ata Transfer Si	ze bit				
	1 = Byte						
	0 = Word						
bit 13	DIR: DMA Tra	ansfer Direction) bit (source/d	estination bus	select)		
	1 = Reads from 0 = Reads from 1	om RAM addre	ddress. writes to p	s to RAM addr	ess ess		
bit 12	HALF: DMA	Block Transfer	Interrupt Sele	ct bit			
	1 = Initiates i	nterrupt when I	nalf of the dat	a has been mo	oved		
	0 = Initiates i	nterrupt when a	all of the data	has been mov	ved		
bit 11	NULLW: Null	Data Periphera	al Write Mode	Select bit			
	1 = Null data	write to periph	eral in additio	n to RAM write	e (DIR bit must a	also be clear)	
bit 10-6	Unimplemen	ted: Read as '	ר'				
bit 5-4	AMODE<1:0	: DMA Channe	el Addressina	Mode Select	bits		
	11 = Reserve	ed					
	10 = Peripher	ral Indirect Add	ressing mode				
	01 = Register	Indirect withou	ut Post-Increm	nent mode			
hit 3 2		tod: Pood as '	ost-incremen	tmode			
bit 1_0		DMA Channel	Operating Mc	nda Salact hits			
bit 1-0	11 = One-Sh	ot. Pina-Pona r	nodes are en	abled (one blo	ck transfer from	/to each DMA b	ouffer)
	10 = Continue	ous, Ping-Pong	modes are e	nabled			
	01 = One-Sho	ot, Ping-Pong r	nodes are dis	abled			
		ous, Ping-Pong	modes are d	ISADIEO			

REGISTER 8-1: DMAXCON: DMA CHANNEL X CONTROL REGISTER

U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	_	_	—	_	—	_	—
bit 15		L	I	4			bit 8
U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
—				INT2R<6:0>			
bit 7							bit 0
Legend:							
R = Readable	bit	W = Writable	bit	U = Unimpler	mented bit, read	l as '0'	
-n = Value at POR							
-n = Value at F	POR	'1' = Bit is set		'0' = Bit is cle	ared	x = Bit is unkr	nown
-n = Value at F	POR	'1' = Bit is set		'0' = Bit is cle	ared	x = Bit is unkr	iown
-n = Value at F bit 15-7	POR Unimplemen	<pre>'1' = Bit is set ted: Read as '0</pre>	0'	ʻ0' = Bit is cle	ared	x = Bit is unkr	iown
-n = Value at F bit 15-7 bit 6-0	Unimplement INT2R<6:0>: (see Table 11-	'1' = Bit is set ted: Read as '0 Assign Externa -2 for input pin)' al Interrupt 2 (selection nun	'0' = Bit is cle (INT2) to the C nbers)	orresponding R	x = Bit is unkr Pn Pin bits	iown
-n = Value at F bit 15-7 bit 6-0	POR Unimplement INT2R<6:0>: (see Table 11- 1111001 = In	'1' = Bit is set ted: Read as '0 Assign Externa -2 for input pin uput tied to RPI	o' al Interrupt 2 (selection nun 121	'0' = Bit is cle (INT2) to the C nbers)	ared	x = Bit is unkr Pn Pin bits	iown
-n = Value at F bit 15-7 bit 6-0	OR Unimplemen INT2R<6:0>: (see Table 11- 1111001 = In	'1' = Bit is set ted: Read as '(Assign Externa -2 for input pin put tied to RPI	o' al Interrupt 2 (selection nun 121	'0' = Bit is cle (INT2) to the C nbers)	orresponding R	x = Bit is unkr Pn Pin bits	iown
-n = Value at F bit 15-7 bit 6-0	POR Unimplement INT2R<6:0>: (see Table 11- 1111001 = In	'1' = Bit is set ted: Read as '0 Assign Externa 2 for input pin uput tied to RPI	o' al Interrupt 2 (selection nun 121	'0' = Bit is cle (INT2) to the C nbers)	orresponding R	x = Bit is unkr Pn Pin bits	iown
-n = Value at F bit 15-7 bit 6-0	POR Unimplement INT2R<6:0>: (see Table 11- 1111001 = In	'1' = Bit is set ted: Read as '0 Assign Externa 2 for input pin put tied to RPI	o' al Interrupt 2 (selection nun 121 P1	'0' = Bit is cle (INT2) to the C nbers)	orresponding R	x = Bit is unkr Pn Pin bits	iown
-n = Value at F bit 15-7 bit 6-0	Unimplement INT2R<6:0>: (see Table 11- 1111001 = In 0000001 = In 0000000 = In	'1' = Bit is set ted: Read as '0 Assign Externa 2 for input pin put tied to RPI put tied to CMI put tied to Vss	o' al Interrupt 2 (selection nun 121 P1	'0' = Bit is cle (INT2) to the C nbers)	orresponding R	x = Bit is unkr	iown

REGISTER 11-2: RPINR1: PERIPHERAL PIN SELECT INPUT REGISTER 1

REGISTER 11-3: RPINR3: PERIPHERAL PIN SELECT INPUT REGISTER 3

U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0	
—	_		_				_	
bit 15							bit 8	
U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	
—				T2CKR<6:0>				
bit 7							bit 0	
Legend:								
R = Readabl	le bit	W = Writable I	bit	U = Unimplem	nented bit, read	as '0'		
-n = Value at	t POR	'1' = Bit is set	'1' = Bit is set		'0' = Bit is cleared		x = Bit is unknown	
bit 15-7	Unimplemen	ted: Read as 'o)'					
bit 15-7 bit 6-0	Unimplemen T2CKR<6:0> (see Table 11	ted: Read as '(: Assign Timer2 -2 for input pin)' 2 External Clo selection nur	ock (T2CK) to th nbers)	e Correspondi	ng RPn pin bits		
bit 15-7 bit 6-0	Unimplemen T2CKR<6:0> (see Table 11 1111001 = Ir	ted: Read as '(: Assign Timer2 -2 for input pin nput tied to RPI) [;] 2 External Clo selection nur 121	ock (T2CK) to th nbers)	ie Correspondii	ng RPn pin bits		
bit 15-7 bit 6-0	Unimplemen T2CKR<6:0> (see Table 11 1111001 = Ir	ted: Read as '(: Assign Timer2 -2 for input pin nput tied to RPI) [;] 2 External Clo selection nur 121	ock (T2CK) to th nbers)	e Correspondi	ng RPn pin bits		
bit 15-7 bit 6-0	Unimplemen T2CKR<6:0> (see Table 11 1111001 = Ir	ted: Read as ' : Assign Timer2 -2 for input pin nput tied to RPI)' 2 External Cle selection nur 121	ock (T2CK) to th nbers)	e Correspondi	ng RPn pin bits		
bit 15-7 bit 6-0	Unimplemen T2CKR<6:0> (see Table 11 1111001 = Ir	ted: Read as 'c : Assign Timer2 -2 for input pin nput tied to RPI)' 2 External Clo selection nur 121 P1	ock (T2CK) to th nbers)	le Correspondi	ng RPn pin bits		
bit 15-7 bit 6-0	Unimplemen T2CKR<6:0> (see Table 11 1111001 = Ir 0000001 = Ir 0000000 = Ir	ted: Read as '(: Assign Timer2 -2 for input pin nput tied to RPI nput tied to CMI nput tied to Vss)' 2 External Clo selection nur 121 P1	ock (T2CK) to th nbers)	e Correspondi	ng RPn pin bits		

U-0	U-0	U-0	U-0	U-0	U-0	U-0	R/W-0
—	—	—	—	—	—	—	IC32
bit 15							bit 8
R/W-0	R/W/HS-0	U-0	R/W-0	R/W-1	R/W-1	R/W-0	R/W-1

REGISTER 14-2: ICxCON2: INPUT CAPTURE x CONTROL REGISTER 2

bit 7			bit 0
Legend:	HS = Hardware Settal	ble bit	
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	

SYNCSEL4⁽⁴⁾ SYNCSEL3⁽⁴⁾ SYNCSEL2⁽⁴⁾ SYNCSEL1⁽⁴⁾

SYNCSEL0⁽⁴⁾

		P	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15-9 Unimplemented: Read as '0'

TRIGSTAT⁽³⁾

ICTRIG⁽²⁾

bit 8

- IC32: Input Capture 32-Bit Timer Mode Select bit (Cascade mode)
 - 1 = Odd IC and Even IC form a single 32-bit input capture module⁽¹⁾
 - 0 = Cascade module operation is disabled

bit 7 ICTRIG: Input Capture Trigger Operation Select bit⁽²⁾

- 1 = Input source used to trigger the input capture timer (Trigger mode)
- 0 = Input source used to synchronize the input capture timer to a timer of another module (Synchronization mode)

bit 6 **TRIGSTAT:** Timer Trigger Status bit⁽³⁾

- 1 = ICxTMR has been triggered and is running
- 0 = ICxTMR has not been triggered and is being held clear

bit 5 Unimplemented: Read as '0'

- **Note 1:** The IC32 bit in both the Odd and Even IC must be set to enable Cascade mode.
 - 2: The input source is selected by the SYNCSEL<4:0> bits of the ICxCON2 register.
 - **3:** This bit is set by the selected input source (selected by SYNCSEL<4:0> bits). It can be read, set and cleared in software.
 - 4: Do not use the ICx module as its own Sync or Trigger source.
 - 5: This option should only be selected as a trigger source and not as a synchronization source.
 - 6: Each Input Capture x (ICx) module has one PTG input source. See Section 24.0 "Peripheral Trigger Generator (PTG) Module" for more information.

PTGO8 = IC1 PTGO9 = IC2 PTGO10 = IC3 PTGO11 = IC4

DS70000657H-page 216

REGISTER 16-13: IOCONX: PWMx I/O CONTROL REGISTER⁽²⁾ (CONTINUED)

- bit 1 SWAP: SWAP PWMxH and PWMxL Pins bit
 1 = PWMxH output signal is connected to PWMxL pins; PWMxL output signal is connected to PWMxH pins
 0 = PWMxH and PWMxL pins are mapped to their respective pins
 bit 0 OSYNC: Output Override Synchronization bit
 1 = Output overrides via the OVRDAT<1:0> bits are synchronized to the PWMx period boundary
 - 0 = Output overrides via the OVDDAT<1:0> bits occur on the next CPU clock boundary
- Note 1: These bits should not be changed after the PWMx module is enabled (PTEN = 1).
 - 2: If the PWMLOCK Configuration bit (FOSCSEL<6>) is a '1', the IOCONx register can only be written after the unlock sequence has been executed.

dsPIC33EPXXXGP50X, dsPIC33EPXXXMC20X/50X AND PIC24EPXXXGP/MC20X

REGISTER 17-17: INT1TMRH: INTERVAL 1 TIMER HIGH WORD REGISTER

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
			INTTM	R<31:24>			
bit 15							bit 8
R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
			INTTM	R<23:16>			
bit 7							bit 0
Legend:							
R = Readable b	bit	W = Writable bi	it	U = Unimplem	nented bit, read	d as '0'	
-n = Value at P	OR	'1' = Bit is set		'0' = Bit is clea	ared	x = Bit is unkr	nown

bit 15-0 INTTMR<31:16>: High Word Used to Form 32-Bit Interval Timer Register (INT1TMR) bits

REGISTER 17-18: INT1TMRL: INTERVAL 1 TIMER LOW WORD REGISTER

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
			INTTM	1R<15:8>			
bit 15							bit 8
R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
			INTT	/IR<7:0>			
bit 7							bit 0
Legend:							
R = Readable bit W = Writable bit			bit	U = Unimplemented bit, read as '0'			
-n = Value at POR (1' = Bit is				'0' = Bit is cle	ared	x = Bit is unkr	nown

bit 15-0 INTTMR<15:0>: Low Word Used to Form 32-Bit Interval Timer Register (INT1TMR) bits

R/W-0	R/W-0	R/W-0	U-0	U-0	U-0	U-0	U-0
DMABS2	DMABS1	DMABS0	—	_	_	_	—
bit 15							bit 8
U-0	U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
—	—	—	FSA4	FSA3	FSA2	FSA1	FSA0
bit 7							bit 0
Legend:							
R = Readable	bit	W = Writable I	bit	U = Unimple	mented bit, read	d as '0'	
-n = Value at P	POR	'1' = Bit is set		'0' = Bit is cle	eared	x = Bit is unkr	nown
bit 15-13 bit 12-5 bit 4-0	DMABS<2:0>: DMA Buffer Size bits 111 = Reserved 110 = 32 buffers in RAM 101 = 24 buffers in RAM 100 = 16 buffers in RAM 011 = 12 buffers in RAM 010 = 8 buffers in RAM 001 = 6 buffers in RAM 000 = 4 buffers in RAM Unimplemented: Read as '0' FSA<4:0>: FIFO Area Starts with Buffer bits 11111 = Read Buffer RB31 11110 = Read Buffer RB30 • • 00001 = TX/RX Buffer TRB1 00000 = TX/RX Buffer TRB1						

REGISTER 21-4: CxFCTRL: ECANx FIFO CONTROL REGISTER

REGISTER 25-5: CMxMSKCON: COMPARATOR x MASK GATING CONTROL REGISTER (CONTINUED)

bit 3 ABEN: AND Gate B Input Enable bit 1 = MBI is connected to AND gate 0 = MBI is not connected to AND gate bit 2 ABNEN: AND Gate B Input Inverted Enable bit 1 = Inverted MBI is connected to AND gate 0 = Inverted MBI is not connected to AND gate bit 1 AAEN: AND Gate A Input Enable bit 1 = MAI is connected to AND gate 0 = MAI is not connected to AND gate bit 0 AANEN: AND Gate A Input Inverted Enable bit 1 = Inverted MAI is connected to AND gate 0 = Inverted MAI is not connected to AND gate

Bit Field	Description
GCP	General Segment Code-Protect bit 1 = User program memory is not code-protected 0 = Code protection is enabled for the entire program memory space
GWRP	General Segment Write-Protect bit 1 = User program memory is not write-protected 0 = User program memory is write-protected
IESO	 Two-Speed Oscillator Start-up Enable bit 1 = Start up device with FRC, then automatically switch to the user-selected oscillator source when ready 0 = Start up device with user-selected oscillator source
PWMLOCK ⁽¹⁾	PWM Lock Enable bit 1 = Certain PWM registers may only be written after a key sequence 0 = PWM registers may be written without a key sequence
FNOSC<2:0>	Oscillator Selection bits 111 = Fast RC Oscillator with Divide-by-N (FRCDIVN) 110 = Fast RC Oscillator with Divide-by-16 (FRCDIV16) 101 = Low-Power RC Oscillator (LPRC) 100 = Reserved; do not use 011 = Primary Oscillator with PLL module (XT + PLL, HS + PLL, EC + PLL) 010 = Primary Oscillator (XT, HS, EC) 001 = Fast RC Oscillator with Divide-by-N with PLL module (FRCPLL) 000 = Fast RC Oscillator (FRC)
FCKSM<1:0>	Clock Switching Mode bits 1x = Clock switching is disabled, Fail-Safe Clock Monitor is disabled 01 = Clock switching is enabled, Fail-Safe Clock Monitor is disabled 00 = Clock switching is enabled, Fail-Safe Clock Monitor is enabled
IOL1WAY	Peripheral Pin Select Configuration bit 1 = Allow only one reconfiguration 0 = Allow multiple reconfigurations
OSCIOFNC	OSC2 Pin Function bit (except in XT and HS modes) 1 = OSC2 is the clock output 0 = OSC2 is a general purpose digital I/O pin
POSCMD<1:0>	Primary Oscillator Mode Select bits 11 = Primary Oscillator is disabled 10 = HS Crystal Oscillator mode 01 = XT Crystal Oscillator mode 00 = EC (External Clock) mode
FWDTEN	 Watchdog Timer Enable bit 1 = Watchdog Timer is always enabled (LPRC oscillator cannot be disabled. Clearing the SWDTEN bit in the RCON register will have no effect.) 0 = Watchdog Timer is enabled/disabled by user software (LPRC can be disabled by clearing the SWDTEN bit in the RCON register)
WINDIS	Watchdog Timer Window Enable bit 1 = Watchdog Timer in Non-Window mode 0 = Watchdog Timer in Window mode
PLLKEN	PLL Lock Enable bit 1 = PLL lock is enabled 0 = PLL lock is disabled

TABLE 27-2: CONFIGURATION BITS DESCRIPTION

Note 1: This bit is only available on dsPIC33EPXXXMC20X/50X and PIC24EPXXXMC20X devices.

2: When JTAGEN = 1, an internal pull-up resistor is enabled on the TMS pin. Erased devices default to JTAGEN = 1. Applications requiring I/O pins in a high-impedance state (tri-state) in Reset should use pins other than TMS for this purpose.

DC CHARACTERISTICS			$\begin{tabular}{lllllllllllllllllllllllllllllllllll$					
Param No.	Symbol	Characteristic	Min. Typ. ⁽¹⁾ Max. Units Cond				Conditions	
		Program Flash Memory						
D130	Eр	Cell Endurance	10,000		_	E/W	-40°C to +125°C	
D131	Vpr	VDD for Read	3.0		3.6	V		
D132b	VPEW	VDD for Self-Timed Write	3.0		3.6	V		
D134	TRETD	Characteristic Retention	20	—	—	Year	Provided no other specifications are violated, -40°C to +125°C	
D135	IDDP	Supply Current during Programming ⁽²⁾	—	10	—	mA		
D136	IPEAK	Instantaneous Peak Current During Start-up	_	_	150	mA		
D137a	TPE	Page Erase Time	17.7	—	22.9	ms	TPE = 146893 FRC cycles, Ta = +85°C (See Note 3)	
D137b	Тре	Page Erase Time	17.5	_	23.1	ms	TPE = 146893 FRC cycles, TA = +125°C (See Note 3)	
D138a	Tww	Word Write Cycle Time	41.7	_	53.8	μs	Tww = 346 FRC cycles, TA = +85°C (See Note 3)	
D138b	Tww	Word Write Cycle Time	41.2	—	54.4	μs	Tww = 346 FRC cycles, Ta = +125°C (See Note 3)	

TABLE 30-14: DC CHARACTERISTICS: PROGRAM MEMORY

Note 1: Data in "Typical" column is at 3.3V, +25°C unless otherwise stated.

2: Parameter characterized but not tested in manufacturing.

3: Other conditions: FRC = 7.37 MHz, TUN<5:0> = 011111 (for Minimum), TUN<5:0> = 100000 (for Maximum). This parameter depends on the FRC accuracy (see Table 30-19) and the value of the FRC Oscillator Tuning register (see Register 9-4). For complete details on calculating the Minimum and Maximum time, see Section 5.3 "Programming Operations".

NOTES:

31.0 HIGH-TEMPERATURE ELECTRICAL CHARACTERISTICS

This section provides an overview of dsPIC33EPXXXGP50X, dsPIC33EPXXXMC20X/50X and PIC24EPXXXGP/ MC20X electrical characteristics for devices operating in an ambient temperature range of -40°C to +150°C.

The specifications between -40° C to $+150^{\circ}$ C are identical to those shown in **Section 30.0** "**Electrical Characteristics**" for operation between -40° C to $+125^{\circ}$ C, with the exception of the parameters listed in this section.

Parameters in this section begin with an H, which denotes High temperature. For example, Parameter DC10 in **Section 30.0 "Electrical Characteristics"** is the Industrial and Extended temperature equivalent of HDC10.

Absolute maximum ratings for the dsPIC33EPXXXGP50X, dsPIC33EPXXXMC20X/50X and PIC24EPXXXGP/MC20X high-temperature devices are listed below. Exposure to these maximum rating conditions for extended periods can affect device reliability. Functional operation of the device at these or any other conditions above the parameters indicated in the operation listings of this specification is not implied.

Absolute Maximum Ratings⁽¹⁾

Ambient temperature under bias ⁽²⁾	40°C to +150°C
Storage temperature	-65°C to +160°C
Voltage on VDD with respect to Vss	-0.3V to +4.0V
Voltage on any pin that is not 5V tolerant with respect to Vss ⁽³⁾	-0.3V to (VDD + 0.3V)
Voltage on any 5V tolerant pin with respect to Vss when VDD < 3.0V ⁽³⁾	-0.3V to 3.6V
Voltage on any 5V tolerant pin with respect to Vss when $VDD \ge 3.0V^{(3)}$	-0.3V to 5.5V
Maximum current out of Vss pin	60 mA
Maximum current into VDD pin ⁽⁴⁾	60 mA
Maximum junction temperature	+155°C
Maximum current sourced/sunk by any 4x I/O pin	10 mA
Maximum current sourced/sunk by any 8x I/O pin	
Maximum current sunk by all ports combined	70 mA
Maximum current sourced by all ports combined ⁽⁴⁾	70 mA

- **Note 1:** Stresses above those listed under "Absolute Maximum Ratings" can cause permanent damage to the device. This is a stress rating only, and functional operation of the device at those or any other conditions above those indicated in the operation listings of this specification is not implied. Exposure to maximum rating conditions for extended periods can affect device reliability.
 - 2: AEC-Q100 reliability testing for devices intended to operate at +150°C is 1,000 hours. Any design in which the total operating time from +125°C to +150°C will be greater than 1,000 hours is not warranted without prior written approval from Microchip Technology Inc.
 - 3: Refer to the "Pin Diagrams" section for 5V tolerant pins.
 - 4: Maximum allowable current is a function of device maximum power dissipation (see Table 31-2).

31.1 High-Temperature DC Characteristics

TABLE 31-1: OPERATING MIPS VS. VOLTAGE

			Max MIPS		
Characteristic	VDD Range (in Volts)	Temperature Range (in °C)	dsPIC33EPXXXGP50X, dsPIC33EPXXXMC20X/50X and PIC24EPXXXGP/MC20X		
HDC5	3.0 to 3.6V ⁽¹⁾	-40°C to +150°C	40		

Note 1: Device is functional at VBORMIN < VDD < VDDMIN. Analog modules, such as the ADC, may have degraded performance. Device functionality is tested but not characterized.

TABLE 31-2: THERMAL OPERATING CONDITIONS

Rating	Symbol	Min	Тур	Max	Unit
High-Temperature Devices					
Operating Junction Temperature Range	TJ	-40		+155	°C
Operating Ambient Temperature Range	TA	-40	—	+150	°C
Power Dissipation: Internal Chip Power Dissipation: $PINT = VDD x (IDD - \Sigma IOH)$ I/O Pin Power Dissipation: $I/O = \Sigma (\{VDD - VOH\} x IOH) + \Sigma (VOL x IOL)$	PD		Pint + Pi/c)	W
Maximum Allowed Power Dissipation	PDMAX	(TJ – TA)/θJ	IA	W

TABLE 31-3: DC TEMPERATURE AND VOLTAGE SPECIFICATIONS

DC CHARACTERISTICS			Standard Operating Conditions: 3.0V to 3.6V(unless otherwise stated)Operating temperature $-40^{\circ}C \le TA \le +150^{\circ}C$					
Parameter No.	Symbol	Characteristic	Min Typ Max Units Conditions					
Operating V	Operating Voltage							
HDC10	Supply Voltage							
	Vdd	_	3.0	3.3	3.6	V	-40°C to +150°C	

NOTES:

28-Lead Plastic Small Outline (SO) - Wide, 7.50 mm Body [SOIC]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging





Microchip Technology Drawing C04-052C Sheet 1 of 2