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"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

#### Applications of "<u>Embedded -</u> <u>Microcontrollers</u>"

#### Details

Product Status	Obsolete
Core Processor	PIC
Core Size	16-Bit
Speed	60 MIPs
Connectivity	I <sup>2</sup> C, IrDA, LINbus, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, DMA, POR, PWM, WDT
Number of I/O	21
Program Memory Size	256KB (85.5K x 24)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	16K x 16
Voltage - Supply (Vcc/Vdd)	3V ~ 3.6V
Data Converters	A/D 6x10b/12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 125°C (TA)
Mounting Type	Surface Mount
Package / Case	28-SSOP (0.209", 5.30mm Width)
Supplier Device Package	28-SSOP
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/pic24ep256gp202t-e-ss

Email: info@E-XFL.COM

Address: Room A, 16/F, Full Win Commercial Centre, 573 Nathan Road, Mongkok, Hong Kong

# TABLE 2: dsPIC33EPXXXMC20X/50X and PIC24EPXXXMC20X MOTOR CONTROL FAMILIES (CONTINUED)

						Rer	nappa	ble P	eriphe	erals								1			
Device	Page Erase Size (Instructions)	Program Flash Memory (Kbyte	RAM (Kbytes)	16-Bit/32-Bit Timers	Input Capture	Output Compare	Motor Control PWM <sup>(4)</sup> (Channels)	Quadrature Encoder Interface	UART	SPI <sup>(2)</sup>	ECAN™ Technology	External Interrupts <sup>(3)</sup>	I <sup>2</sup> C <sup>TM</sup>	<b>CRC Generator</b>	10-Bit/12-Bit ADC (Channels)	Op Amps/Comparators	CTMU	PTG	I/O Pins	Pins	Packages
dsPIC33EP32MC504	512	32	4																		
dsPIC33EP64MC504	1024	64	8				6	1	1 2			1 3 2		1 9			Yes	Yes	35	44/ 48	VTLA <sup>(5)</sup> , TQFP, QFN, UQFN
dsPIC33EP128MC504	1024	128	16	5	4	4				2	2 1		2		9	3/4					
dsPIC33EP256MC504	1024	256	32																		
dsPIC33EP512MC504	1024	512	48																		
dsPIC33EP64MC506	1024	64	8		5 4																
dsPIC33EP128MC506	1024	128	16	5		4	6	1	2	2	1	2	2	1	16		Vaa	Voo	50	64	TQFP, QFN
dsPIC33EP256MC506	1024	256	32	э	4	4	6	1	2	2	1	3	2	1	16	3/4	res	res	53	64	
dsPIC33EP512MC506	1024	512	48																		

 Note 1:
 On 28-pin devices, Comparator 4 does not have external connections. Refer to Section 25.0 "Op Amp/Comparator Module" for details.

 2:
 Only SPI2 is remappable.

3: INT0 is not remappable.

4: Only the PWM Faults are remappable.

5: The SSOP and VTLA packages are not available for devices with 512 Kbytes of memory.

#### FIGURE 4-2: PROGRAM MEMORY MAP FOR dsPIC33EP64GP50X, dsPIC33EP64MC20X/50X AND PIC24EP64GP/MC20X DEVICES



Note: Memory areas are not shown to scale.

#### 4.6.3 MODULO ADDRESSING APPLICABILITY

Modulo Addressing can be applied to the Effective Address (EA) calculation associated with any W register. Address boundaries check for addresses equal to:

- The upper boundary addresses for incrementing buffers
- The lower boundary addresses for decrementing buffers

It is important to realize that the address boundaries check for addresses less than, or greater than, the upper (for incrementing buffers) and lower (for decrementing buffers) boundary addresses (not just equal to). Address changes can, therefore, jump beyond boundaries and still be adjusted correctly.

Note: The modulo corrected Effective Address is written back to the register only when Pre-Modify or Post-Modify Addressing mode is used to compute the Effective Address. When an address offset (such as [W7 + W2]) is used, Modulo Addressing correction is performed but the contents of the register remain unchanged.

# 4.7 Bit-Reversed Addressing (dsPIC33EPXXXMC20X/50X and dsPIC33EPXXXGP50X Devices Only)

Bit-Reversed Addressing mode is intended to simplify data reordering for radix-2 FFT algorithms. It is supported by the X AGU for data writes only.

The modifier, which can be a constant value or register contents, is regarded as having its bit order reversed. The address source and destination are kept in normal order. Thus, the only operand requiring reversal is the modifier.

# 4.7.1 BIT-REVERSED ADDRESSING IMPLEMENTATION

Bit-Reversed Addressing mode is enabled when all these conditions are met:

- BWMx bits (W register selection) in the MODCON register are any value other than '1111' (the stack cannot be accessed using Bit-Reversed Addressing)
- The BREN bit is set in the XBREV register
- The addressing mode used is Register Indirect with Pre-Increment or Post-Increment

If the length of a bit-reversed buffer is  $M = 2^{N}$  bytes, the last 'N' bits of the data buffer start address must be zeros.

XBREV<14:0> is the Bit-Reversed Addressing modifier, or 'pivot point', which is typically a constant. In the case of an FFT computation, its value is equal to half of the FFT data buffer size.

Note:	All bit-reversed EA calculations assume
	word-sized data (LSb of every EA is always
	clear). The XBREVx value is scaled
	accordingly to generate compatible (byte)
	addresses.

When enabled, Bit-Reversed Addressing is executed only for Register Indirect with Pre-Increment or Post-Increment Addressing and word-sized data writes. It does not function for any other addressing mode or for byte-sized data and normal addresses are generated instead. When Bit-Reversed Addressing is active, the W Address Pointer is always added to the address modifier (XBREVx) and the offset associated with the Register Indirect Addressing mode is ignored. In addition, as word-sized data is a requirement, the LSb of the EA is ignored (and always clear).

Note: Modulo Addressing and Bit-Reversed Addressing can be enabled simultaneously using the same W register, but Bit-Reversed Addressing operation will always take precedence for data writes when enabled.

If Bit-Reversed Addressing has already been enabled by setting the BREN (XBREV<15>) bit, a write to the XBREV register should not be immediately followed by an indirect read operation using the W register that has been designated as the Bit-Reversed Pointer.

U-0	U-0	U-0	U-0	U-0	U-0	U-0	R/W-0	
	—	_	_	_	_	_	PLLDIV8	
bit 15		·					bit 8	
R/W-0	R/W-0	R/W-1	R/W-1	R/W-0	R/W-0	R/W-0	R/W-0	
PLLDIV7	PLLDIV6	PLLDIV5	PLLDIV4	PLLDIV3	PLLDIV2	PLLDIV1	PLLDIV0	
bit 7		·			•		bit 0	
Legend:								
R = Readable bit		W = Writable	bit	U = Unimpler	mented bit, read	l as '0'		
-n = Value at F	POR	'1' = Bit is set		'0' = Bit is cle	ared	x = Bit is unknown		
bit 15-9	Unimplemen	ted: Read as '	0'					
bit 8-0	PLLDIV<8:0	>: PLL Feedba	ck Divisor bits	(also denoted	as 'M', PLL mu	ltiplier)		
	111111111	= 513						
	•							
	•							
	•							
	000110000:	= 50 (default)						
	•							
	•							
	•							
	00000010:	= 4						
	000000001	= 3 = 2						
	000000000000	-						

#### REGISTER 9-3: PLLFBD: PLL FEEDBACK DIVISOR REGISTER

### REGISTER 11-16: RPINR38: PERIPHERAL PIN SELECT INPUT REGISTER 38 (dsPIC33EPXXXMC20X AND PIC24EPXXXMC20X DEVICES ONLY)

U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0		
_				DTCMP1R<6:	0>				
bit 15							bit 8		
U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0		
_	—	_		—	—	_	—		
bit 7		·		÷			bit 0		
Legend:									
R = Readable bit W		W = Writable	bit	U = Unimplemented bit, read as '0'					
-n = Value at	POR	'1' = Bit is set		'0' = Bit is cle	ared	x = Bit is unknown			
bit 15	Unimplemer	ted: Read as '	0'						
bit 14-8	DTCMP1R<6 (see Table 11	<b>::0&gt;:</b> Assign PV -2 for input pin	VM Dead-Tim selection nun	e Compensation nbers)	on Input 1 to the	e Correspondine	g RPn Pin bits		
	1111001 <b>=  </b>	nput tied to RPI	121						
	•								
	•								
	0000001 =	nput tied to CM	P1						
	0000000 = li	nput tied to Vss	}						
bit 7-0	Unimplemer	ted: Read as '	0'						

NOTES:

## 12.1 Timer1 Resources

Many useful resources are provided on the main product page of the Microchip web site for the devices listed in this data sheet. This product page, which can be accessed using this link, contains the latest updates and additional information.

Note:	In the event you are not able to access the
	product page using the link above, enter
	this URL in your browser:
	http://www.microchip.com/wwwproducts/
	Devices.aspx?dDocName=en555464

#### 12.1.1 KEY RESOURCES

- "Timers" (DS70362) in the "dsPIC33/PIC24 Family Reference Manual"
- · Code Samples
- Application Notes
- · Software Libraries
- Webinars
- All Related "dsPIC33/PIC24 Family Reference Manual" Sections
- Development Tools

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	U-0	U-0		
PHR	PHF	PLR	PLF	FLTLEBEN	CLLEBEN	_	_		
bit 15	1		1		1		bit 8		
U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0		
—	—	BCH(")	BCL	BPHH	BPHL	BPLH	BPLL		
bit 7							bit 0		
Legend:									
R = Readable bit $W = Writable bit$ $U = Unimplemented bit, read as '0'$									
-n = Value at F	POR	'1' = Bit is set		'0' = Bit is cle	ared	x = Bit is unkr	= Bit is unknown		
bit 15	PHR: PWMxH	Rising Edge	Trigger Enabl	e bit					
	$\perp$ = Rising edg 0 = Leading-E	ge of PyvivixH v Edge Blanking i	anores risina	edge of PWM	anking counter kH				
bit 14	PHF: PWMxH	Falling Edge	Trigger Enabl	e bit					
	1 = Falling ed	ge of PWMxH	will trigger Le	ading-Edge Bla	anking counter				
	0 = Leading-E	Edge Blanking i	gnores falling	g edge of PWM	хH				
bit 13	PLR: PWMxL	. Rising Edge T	rigger Enable	e bit oding Edgo Blo	nking countor				
	0 = Leading-E	Edge Blanking i	gnores rising	edge of PWM	kL				
bit 12	PLF: PWMxL	Falling Edge T	rigger Enable	e bit					
	1 = Falling ed	ge of PWMxL	will trigger Le	ading-Edge Bla	anking counter				
	0 = Leading-E	Edge Blanking i	gnores falling	g edge of PWM	xL				
bit 11	1 = Leading-F	-ault Input Lea Edge Blanking i	ding-Edge Bla	anking Enable	bit				
	0 = Leading-E	Edge Blanking i	s not applied	to selected Fa	ult input				
bit 10	CLLEBEN: C	urrent-Limit Le	ading-Edge E	Blanking Enable	e bit				
	1 = Leading-E	Edge Blanking i	s applied to s	selected curren	t-limit input				
hit 0.6	0 = Leading-E	tode Blanking I	s not applied	to selected cul	rrent-limit input				
bit 5	BCH Blankin	a in Selected F	J Blanking Sign	al High Enable	hit(1)				
bit 5	1 = State blan	kina (of curren	t-limit and/or	Fault input sigr	nals) when seled	ted blanking s	ianal is hiah		
	0 = No blankii	ng when select	ed blanking s	signal is high	,	5	0 0		
bit 4	BCL: Blanking	g in Selected B	lanking Signa	al Low Enable I	bit <sup>(1)</sup>				
	1 = State blan	iking (of curren	t-limit and/or	Fault input sigr	nals) when seled	cted blanking s	ignal is low		
bit 3	BPHH: Blanki	ing in PWMxH	High Enable	hit					
bit o	1 = State blan	iking (of curren	t-limit and/or	Fault input sigr	nals) when PWN	/IxH output is h	igh		
	0 <b>= No blanki</b>	ng when PWM	xH output is h	nigh			-		
bit 2	BPHL: Blanki	ng in PWMxH	Low Enable b	pit					
	1 = State blan 0 = No blankii	nking (of curren ng when PWM	t-limit and/or xH output is le	Fault input sigr ow	nals) when PWN	IxH output is lo	W		
bit 1	BPLH: Blanki	ng in PWMxL I	High Enable b	oit					
	1 = State blan 0 = No blankii	nking (of curren ng when PWM	t-limit and/or xL output is h	Fault input sigr igh	nals) when PWN	/IxL output is hi	igh		
bit 0	BPLL: Blanki	ng in PWMxL L	ow Enable b	it					
	1 = State blan	king (of curren	t-limit and/or	Fault input sigr	nals) when PWN	IxL output is lo	W		
	v = i N o diankii		x∟ output is io	JVV					

# REGISTER 16-16: LEBCONX: PWMx LEADING-EDGE BLANKING CONTROL REGISTER

Note 1: The blanking signal is selected via the BLANKSELx bits in the AUXCONx register.

REGISTER 21-2: CxC1	RL2: ECANx CON	TROL REGISTER 2
---------------------	----------------	-----------------

U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0			
	_	_	_	_	_	_	_			
bit 15							bit 8			
							,			
U-0	U-0	U-0	R-0	R-0	R-0	R-0	R-0			
—	—	—	DNCNT4	DNCNT3	DNCNT2	DNCNT1	DNCNT0			
bit 7							bit 0			
Legend:										
R = Readable I	bit	W = Writable	bit	U = Unimpler	mented bit, read	as '0'				
-n = Value at P	OR	'1' = Bit is set		'0' = Bit is cle	ared	x = Bit is unknown				
bit 15-5	Unimplemen	ted: Read as '	0'							
bit 4-0	DNCNT<4:0>	: DeviceNet™	Filter Bit Num	ber bits						
	10010-1111	1 = Invalid sele	ection							
	10001 <b>= Com</b>	pares up to Da	ata Byte 3, bit	6 with EID<17	>					
	•									
	•									
	•									
	00001 = Compares up to Data Byte 1, bit 7 with EID<0> 00000 = Does not compare data bytes									

### REGISTER 21-16: CxRXFnSID: ECANx ACCEPTANCE FILTER n STANDARD IDENTIFIER REGISTER (n = 0-15)

R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	
SID10	SID9	SID8	SID7	SID6	SID5	SID4	SID3	
bit 15							bit 8	
R/W-x	R/W-x	R/W-x	U-0	R/W-x	U-0	R/W-x	R/W-x	
SID2	SID1	SID0	—	EXIDE	_	EID17	EID16	
bit 7							bit 0	
Legend:								
R = Readable	bit	W = Writable	bit	U = Unimpler	nented bit, read	d as '0'		
-n = Value at P	OR	'1' = Bit is set		'0' = Bit is cle	ared	x = Bit is unknown		
bit 15-5	<b>SID&lt;10:0&gt;:</b> S	tandard Identif	ier bits					
	1 = Message 0 = Message	address bit, SI address bit, SI	Dx, must be '2 Dx, must be '0	L' to match filte	er er			
bit 4	Unimplement	ted: Read as '	כי					
bit 3	EXIDE: Exten	ded Identifier E	Enable bit					
	If MIDE = 1:							
	1 = Matches c	only messages	with Extende	d Identifier add	lresses			
		only messages	with Standard		resses			
	Ignores EXIDI	E bit.						
bit 2	Unimplement	ted: Read as '	כ'					
bit 1-0	EID<17:16>:	Extended Iden	tifier bits					
	1 = Message	address bit, El	Dx, must be 'a	L' to match filte	er			
	0 = Message	address bit, El	Dx, must be '	o' to match filte	er			

REGISTER 24-6:	PTGSDLIM: PTG STEP DELAY LIMIT REGISTER <sup>(1,2)</sup>

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
			PTGSD	LIM<15:8>			
bit 15							bit 8
R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
			PTGSE	DLIM<7:0>			
bit 7							bit 0
Legend:							
R = Readable	R = Readable bit W = Writable bit U = Unimplemented bit, read as '0'						
-n = Value at P	1 = Value at POR '1' = Bit is set '0' = Bit is cleared x = Bit is unknow					nown	

bit 15-0 **PTGSDLIM<15:0>:** PTG Step Delay Limit Register bits Holds a PTG Step delay value representing the number of additional PTG clocks between the start of a Step command and the completion of a Step command.

**Note 1:** A base Step delay of one PTG clock is added to any value written to the PTGSDLIM register (Step Delay = (PTGSDLIM) + 1).

2: This register is read-only when the PTG module is executing Step commands (PTGEN = 1 and PTGSTRT = 1).

# REGISTER 24-7: PTGC0LIM: PTG COUNTER 0 LIMIT REGISTER<sup>(1)</sup>

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
			PTGC0	LIM<15:8>			
bit 15							bit 8
R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
			PTGC	)LIM<7:0>			
bit 7							bit 0
Legend:							
R = Readable	bit	W = Writable b	oit	U = Unimpler	mented bit, rea	ad as '0'	
-n = Value at F	POR	'1' = Bit is set		'0' = Bit is cle	ared	x = Bit is unkı	nown

bit 15-0 **PTGC0LIM<15:0>:** PTG Counter 0 Limit Register bits May be used to specify the loop count for the PTGJMPC0 Step command or as a limit register for the General Purpose Counter 0.

**Note 1:** This register is read-only when the PTG module is executing Step commands (PTGEN = 1 and PTGSTRT = 1).

### 27.2 User ID Words

dsPIC33EPXXXGP50X, dsPIC33EPXXXMC20X/50X and PIC24EPXXXGP/MC20X devices contain four User ID Words, located at addresses, 0x800FF8 through 0x800FFE. The User ID Words can be used for storing product information such as serial numbers, system manufacturing dates, manufacturing lot numbers and other application-specific information.

The User ID Words register map is shown in Table 27-3.

TABLE 27-3:USER ID WORDS REGISTER<br/>MAP

File Name	Address	Bits 23-16	Bits 15-0
FUID0	0x800FF8	—	UID0
FUID1	0x800FFA	—	UID1
FUID2	0x800FFC	—	UID2
FUID3	0x800FFE	—	UID3

**Legend:** — = unimplemented, read as '1'.

# 27.3 On-Chip Voltage Regulator

All of the dsPIC33EPXXXGP50X, dsPIC33EPXXXMC20X/50X and PIC24EPXXXGP/ MC20X devices power their core digital logic at a nominal 1.8V. This can create a conflict for designs that are required to operate at a higher typical voltage, such as 3.3V. To simplify system design, all devices in the dsPIC33EPXXXGP50X, dsPIC33EPXXXMC20X/50X and PIC24EPXXXGP/MC20X family incorporate an onchip regulator that allows the device to run its core logic from VDD.

The regulator provides power to the core from the other VDD pins. A low-ESR (less than 1 Ohm) capacitor (such as tantalum or ceramic) must be connected to the VCAP pin (Figure 27-1). This helps to maintain the stability of the regulator. The recommended value for the filter capacitor is provided in Table 30-5 located in **Section 30.0 "Electrical Characteristics"**.

Note: It is important for the low-ESR capacitor to be placed as close as possible to the VCAP pin.

# FIGURE 27-1: CONNECTIONS FOR THE ON-CHIP VOLTAGE

REGULATOR<sup>(1,2,3)</sup>



# 27.4 Brown-out Reset (BOR)

The Brown-out Reset (BOR) module is based on an internal voltage reference circuit that monitors the regulated supply voltage, VCAP. The main purpose of the BOR module is to generate a device Reset when a brown-out condition occurs. Brown-out conditions are generally caused by glitches on the AC mains (for example, missing portions of the AC cycle waveform due to bad power transmission lines or voltage sags due to excessive current draw when a large inductive load is turned on).

A BOR generates a Reset pulse, which resets the device. The BOR selects the clock source, based on the device Configuration bit values (FNOSC<2:0> and POSCMD<1:0>).

If an oscillator mode is selected, the BOR activates the Oscillator Start-up Timer (OST). The system clock is held until OST expires. If the PLL is used, the clock is held until the LOCK bit (OSCCON<5>) is '1'.

Concurrently, the PWRT Time-out (TPWRT) is applied before the internal Reset is released. If TPWRT = 0 and a crystal oscillator is being used, then a nominal delay of TFSCM is applied. The total delay in this case is TFSCM. Refer to Parameter SY35 in Table 30-22 of **Section 30.0 "Electrical Characteristics"** for specific TFSCM values.

The BOR status bit (RCON<1>) is set to indicate that a BOR has occurred. The BOR circuit continues to operate while in Sleep or Idle modes and resets the device should VDD fall below the BOR threshold voltage.

Base Instr #	Assembly Mnemonic		Assembly Syntax	Description	# of Words	# of Cycles <sup>(2)</sup>	Status Flags Affected
72	SL	SL	f	f = Left Shift f	1	1	C,N,OV,Z
		SL	f,WREG	WREG = Left Shift f	1	1	C,N,OV,Z
		SL	Ws,Wd	Wd = Left Shift Ws	1	1	C,N,OV,Z
		SL	Wb,Wns,Wnd	Wnd = Left Shift Wb by Wns	1	1	N,Z
		SL	Wb,#lit5,Wnd	Wnd = Left Shift Wb by lit5	1	1	N,Z
73	SUB	SUB	<sub>Acc</sub> (1)	Subtract Accumulators	1	1	OA,OB,OAB, SA,SB,SAB
		SUB	f	f = f – WREG	1	1	C,DC,N,OV,Z
		SUB	f,WREG	WREG = f – WREG	1	1	C,DC,N,OV,Z
		SUB	#lit10,Wn	Wn = Wn - lit10	1	1	C,DC,N,OV,Z
		SUB	Wb,Ws,Wd	Wd = Wb – Ws	1	1	C,DC,N,OV,Z
		SUB	Wb,#lit5,Wd	Wd = Wb – lit5	1	1	C,DC,N,OV,Z
74	SUBB	SUBB	f	$f = f - WREG - (\overline{C})$	1	1	C,DC,N,OV,Z
		SUBB	f,WREG	WREG = $f - WREG - (\overline{C})$	1	1	C,DC,N,OV,Z
		SUBB	#lit10,Wn	Wn = Wn – lit10 – $(\overline{C})$	1	1	C,DC,N,OV,Z
		SUBB	Wb,Ws,Wd	$Wd = Wb - Ws - (\overline{C})$	1	1	C,DC,N,OV,Z
		SUBB	Wb,#lit5,Wd	$Wd = Wb - lit5 - (\overline{C})$	1	1	C,DC,N,OV,Z
75	SUBR	SUBR	f	f = WREG – f	1	1	C,DC,N,OV,Z
		SUBR	f,WREG	WREG = WREG – f	1	1	C,DC,N,OV,Z
		SUBR	Wb,Ws,Wd	Wd = Ws – Wb	1	1	C,DC,N,OV,Z
		SUBR	Wb,#lit5,Wd	Wd = lit5 – Wb	1	1	C,DC,N,OV,Z
76	SUBBR	SUBBR	f	$f = WREG - f - (\overline{C})$	1	1	C,DC,N,OV,Z
		SUBBR	f,WREG	WREG = WREG – f – $(\overline{C})$	1	1	C,DC,N,OV,Z
		SUBBR	Wb,Ws,Wd	$Wd = Ws - Wb - (\overline{C})$	1	1	C,DC,N,OV,Z
		SUBBR	Wb,#lit5,Wd	$Wd = lit5 - Wb - (\overline{C})$	1	1	C,DC,N,OV,Z
77	SWAP	SWAP.b	Wn	Wn = nibble swap Wn	1	1	None
		SWAP	Wn	Wn = byte swap Wn	1	1	None
78	TBLRDH	TBLRDH	Ws,Wd	Read Prog<23:16> to Wd<7:0>	1	5	None
79	TBLRDL	TBLRDL	Ws,Wd	Read Prog<15:0> to Wd	1	5	None
80	TBLWTH	TBLWTH	Ws,Wd	Write Ws<7:0> to Prog<23:16>	1	2	None
81	TBLWTL	TBLWTL	Ws,Wd	Write Ws to Prog<15:0>	1	2	None
82	ULNK	ULNK		Unlink Frame Pointer	1	1	SFA
83	XOR	XOR	f	f = f .XOR. WREG	1	1	N,Z
		XOR	f,WREG	WREG = f .XOR. WREG	1	1	N,Z
		XOR	#lit10,Wn	Wd = lit10 .XOR. Wd	1	1	N,Z
		XOR	Wb,Ws,Wd	Wd = Wb .XOR. Ws	1	1	N,Z
		XOR	Wb,#lit5,Wd	Wd = Wb .XOR. lit5	1	1	N,Z
84	ZE	ZE	Ws,Wnd	Wnd = Zero-extend Ws	1	1	C,Z,N

## TABLE 28-2: INSTRUCTION SET OVERVIEW (CONTINUED)

Note 1: These instructions are available in dsPIC33EPXXXMC20X/50X and PIC24EPXXXMC20X devices only.

2: Read and Read-Modify-Write (e.g., bit operations and logical operations) on non-CPU SFRs incur an additional instruction cycle.



TADLE 30-23. THVIER I EATERINAL CLOCK THVIING REQUIREIVIEN 13	TABLE 30-23:	TIMER1 EXTERNAL	<b>CLOCK TIMING</b>	<b>REQUIREMENTS</b> <sup>(1)</sup>
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AC CHARACTERISTICS			Standard Ope (unless otherv Operating tem	rating C vise sta perature	conditions: 3.0           ted)           -40°C ≤ TA ≤           -40°C ≤ TA ≤	V to 3.6 +85°C +125°C	V for Industrial C for Extended	
Param No.	Symbol	Characteristic <sup>(2)</sup>		Min.	Тур.	Max.	Units	Conditions
TA10	ТтхН	T1CK High Time	Synchronous mode	Greater of: 20 or (Tcy + 20)/N	_	—	ns	Must also meet Parameter TA15, N = prescaler value (1, 8, 64, 256)
			Asynchronous	35	—	—	ns	
TA11	ΤτxL	T1CK Low Time	Synchronous mode	Greater of: 20 or (Tcy + 20)/N	_	_	ns	Must also meet Parameter TA15, N = prescaler value (1, 8, 64, 256)
			Asynchronous	10	—	—	ns	
TA15	ΤτχΡ	T1CK Input Period	Synchronous mode	Greater of: 40 or (2 Tcy + 40)/N	_		ns	N = prescale value (1, 8, 64, 256)
OS60	Ft1	T1CK Oscillator Input Frequency Range (oscillator enabled by setting bit, TCS (T1CON<1>))		DC		50	kHz	
TA20	TCKEXTMRL	Delay from E Clock Edge t Increment	xternal T1CK to Timer	0.75 Tcy + 40		1.75 Tcy + 40	ns	

Note 1: Timer1 is a Type A.

2: These parameters are characterized, but are not tested in manufacturing.



#### FIGURE 30-24: SPI1 MASTER MODE (FULL-DUPLEX, CKE = 1, CKP = x, SMP = 1) TIMING CHARACTERISTICS

# TABLE 30-43:SPI1 MASTER MODE (FULL-DUPLEX, CKE = 1, CKP = x, SMP = 1)TIMING REQUIREMENTS

AC CHA	RACTERIST	$\begin{array}{l} \mbox{Standard Operating Conditions: 3.0V to 3.6V} \\ \mbox{(unless otherwise stated)} \\ \mbox{Operating temperature} & -40^{\circ}C \leq TA \leq +85^{\circ}C \mbox{ for Industrial} \\ -40^{\circ}C \leq TA \leq +125^{\circ}C \mbox{ for Extended} \end{array}$					
Param.	Symbol	Characteristic <sup>(1)</sup>	Min.	Typ. <sup>(2)</sup>	Max.	Units	Conditions
SP10	FscP	Maximum SCK1 Frequency	_		10	MHz	(Note 3)
SP20	TscF	SCK1 Output Fall Time	—	—	_	ns	See Parameter DO32 (Note 4)
SP21	TscR	SCK1 Output Rise Time	_	—	_	ns	See Parameter DO31 (Note 4)
SP30	TdoF	SDO1 Data Output Fall Time	—	—	_	ns	See Parameter DO32 (Note 4)
SP31	TdoR	SDO1 Data Output Rise Time	—	—		ns	See Parameter DO31 (Note 4)
SP35	TscH2doV, TscL2doV	SDO1 Data Output Valid after SCK1 Edge	—	6	20	ns	
SP36	TdoV2sc, TdoV2scL	SDO1 Data Output Setup to First SCK1 Edge	30	—	_	ns	
SP40	TdiV2scH, TdiV2scL	Setup Time of SDI1 Data Input to SCK1 Edge	30	—	_	ns	
SP41	TscH2diL, TscL2diL	Hold Time of SDI1 Data Input to SCK1 Edge	30			ns	

**Note 1:** These parameters are characterized, but are not tested in manufacturing.

2: Data in "Typical" column is at 3.3V, +25°C unless otherwise stated.

- **3:** The minimum clock period for SCK1 is 100 ns. The clock generated in Master mode must not violate this specification.
- **4:** Assumes 50 pF load on all SPI1 pins.



FIGURE 30-26: SPI1 SLAVE MODE (FULL-DUPLEX, CKE = 1, CKP = 0, SMP = 0) TIMING CHARACTERISTICS

#### TABLE 30-54: OP AMP/COMPARATOR VOLTAGE REFERENCE SETTLING TIME SPECIFICATIONS

AC CHA	RACTERIS	TICS	$\begin{array}{l} \mbox{Standard Operating Conditions (see Note 2): 3.0V} \\ \mbox{(unless otherwise stated)} \\ \mbox{Operating temperature} & -40^\circ C \leq TA \leq +85^\circ C \mbox{ for Indu} \\ -40^\circ C \leq TA \leq +125^\circ C \mbox{ for Ex} \end{array}$				Note 2): 3.0V to 3.6V 85°C for Industrial 125°C for Extended	
Param.	Symbol	Characteristic	Min. Typ. Max. Units Conditions					
VR310	TSET	Settling Time	— 1 10 μs <b>(Note 1)</b>					

**Note 1:** Settling time is measured while CVRR = 1 and CVR<3:0> bits transition from '0000' to '1111'.

2: Device is functional at VBORMIN < VDD < VDDMIN, but will have degraded performance. Device functionality is tested, but not characterized. Analog modules (ADC, op amp/comparator and comparator voltage reference) may have degraded performance. Refer to Parameter BO10 in Table 30-13 for the minimum and maximum BOR values.

#### TABLE 30-55: OP AMP/COMPARATOR VOLTAGE REFERENCE SPECIFICATIONS

DC CHARACTERISTICS			Standard O (unless oth Operating te	perating erwise st emperatur	Conditions (sated) re $-40^{\circ}C \le T$ $-40^{\circ}C \le T$	see Note A ≤ +85°( A ≤ +125	<b>1): 3.0V to 3.6V</b> C for Industrial °C for Extended	
Param No.	Symbol	Characteristics	Min. Typ. Max. Units Conditions					
VRD310	CVRES	Resolution	CVRSRC/24	_	CVRSRC/32	LSb		
VRD311	CVRAA	Absolute Accuracy <sup>(2)</sup>	—	±25	—	mV	CVRSRC = 3.3V	
VRD313	CVRSRC	Input Reference Voltage	0	_	AVDD + 0.3	V		
VRD314	CVROUT	Buffer Output Resistance <sup>(2)</sup>	_	— 1.5k —				

**Note 1:** Device is functional at VBORMIN < VDD < VDDMIN, but will have degraded performance. Device functionality is tested, but not characterized. Analog modules (ADC, op amp/comparator and comparator voltage reference) may have degraded performance. Refer to Parameter BO10 in Table 30-13 for the minimum and maximum BOR values.

2: Parameter is characterized but not tested in manufacturing.

	30-37.												
АС СН	ARACTE	RISTICS	Standard C (unless oth Operating to	peratir erwise empera	ng Condition stated) <sup>(1)</sup> ture -40°C -40°C	I <b>S: 3.0V</b> ≤ Ta ≤ + ≤ Ta ≤ +	7 <b>to 3.6V</b> -85°C for Industrial -125°C for Extended						
Param No.	Symbol	Characteristic	Min.	Тур.	Max.	Units	Conditions						
	Device Supply												
AD01	AVDD	Module VDD Supply	Greater of: VDD – 0.3 or 3.0	—	Lesser of: VDD + 0.3 or 3.6	V							
AD02	AVss	Module Vss Supply	Vss – 0.3	_	Vss + 0.3	V							
		·	Refer	ence In	puts								
AD05	Vrefh	Reference Voltage High	AVss + 2.5	—	AVdd	V	VREFH = VREF+ VREFL = VREF- <b>(Note 1)</b>						
AD05a			3.0	—	3.6	V	VREFH = AVDD VREFL = AVSS = 0						
AD06	VREFL	Reference Voltage Low	AVss	_	AVDD – 2.5	V	(Note 1)						
AD06a	-		0	—	0	V	VREFH = AVDD VREFL = AVSS = 0						
AD07	Vref	Absolute Reference Voltage	2.5	—	3.6	V	VREF = VREFH - VREFL						
AD08	IREF	Current Drain	_	_	10 600	μΑ μΑ	ADC off ADC on						
AD09	IAD	Operating Current <sup>(2)</sup>	—	5	—	mA	ADC operating in 10-bit mode (Note 1)						
			—	2	—	mA	ADC operating in 12-bit mode (Note 1)						
			Ana	log Inp	out	•							
AD12	Vinh	Input Voltage Range Vinн	VINL	_	Vrefh	V	This voltage reflects Sample-and- Hold Channels 0, 1, 2 and 3 (CH0-CH3), positive input						
AD13	VINL	Input Voltage Range VINL	VREFL		AVss + 1V	V	This voltage reflects Sample-and- Hold Channels 0, 1, 2 and 3 (CH0-CH3), negative input						
AD17	Rin	Recommended Impedance of Analog Voltage Source	_		200	Ω	Impedance to achieve maximum performance of ADC						

# TABLE 30-57: ADC MODULE SPECIFICATIONS

**Note 1:** Device is functional at VBORMIN < VDD < VDDMIN, but will have degraded performance. Device functionality is tested, but not characterized. Analog modules (ADC, op amp/comparator and comparator voltage reference) may have degraded performance. Refer to Parameter BO10 in Table 30-13 for the minimum and maximum BOR values.

2: Parameter is characterized but not tested in manufacturing.

# 33.0 PACKAGING INFORMATION

## 33.1 Package Marking Information

## 28-Lead SPDIP



#### 28-Lead SOIC (.300")



28-Lead SSOP



Example dsPIC33EP64GP 502-I/SP@3 1310017

# Example



#### Example



28-Lead QFN-S (6x6x0.9 mm)



Example



Legend	: XXX Y YY WW NNN @3 *	Customer-specific information Year code (last digit of calendar year) Year code (last 2 digits of calendar year) Week code (week of January 1 is week '01') Alphanumeric traceability code Pb-free JEDEC designator for Matte Tin (Sn) This package is Pb-free. The Pb-free JEDEC designator ((e3)) can be found on the outer packaging for this package.
Note:	In the even be carried characters	nt the full Microchip part number cannot be marked on one line, it will d over to the next line, thus limiting the number of available s for customer-specific information.

#### 44-Lead Plastic Thin Quad Flatpack (PT) – 10x10x1 mm Body, 2.00 mm [TQFP]

**Note:** For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



	Units	MILLIMETERS				
	MIN	NOM	MAX			
Number of Leads	N		44			
Lead Pitch	e		0.80 BSC			
Overall Height	A	-	-	1.20		
Molded Package Thickness	A2	0.95	1.00	1.05		
Standoff	A1	0.05	-	0.15		
Foot Length	L	0.45	0.60	0.75		
Footprint	L1	1.00 REF				
Foot Angle	ф	0°	3.5°	7°		
Overall Width	E		12.00 BSC			
Overall Length	D	12.00 BSC				
Molded Package Width	E1	10.00 BSC				
Molded Package Length	D1	10.00 BSC				
Lead Thickness	С	0.09 – 0.20				
Lead Width	b	0.30	0.37	0.45		
Mold Draft Angle Top	α	11° 12° 13°				
Mold Draft Angle Bottom	β	11° 12° 13°				

Notes:

1. Pin 1 visual index feature may vary, but must be located within the hatched area.

2. Chamfers at corners are optional; size may vary.

3. Dimensions D1 and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.25 mm per side.

4. Dimensioning and tolerancing per ASME Y14.5M.

BSC: Basic Dimension. Theoretically exact value shown without tolerances.

REF: Reference Dimension, usually without tolerance, for information purposes only.

Microchip Technology Drawing C04-076B