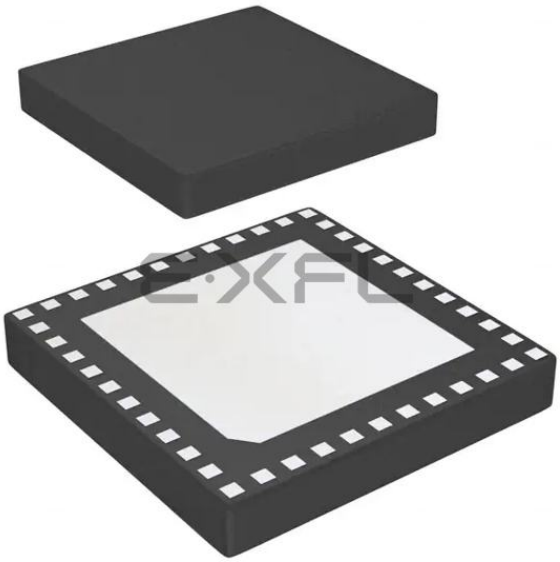

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## What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

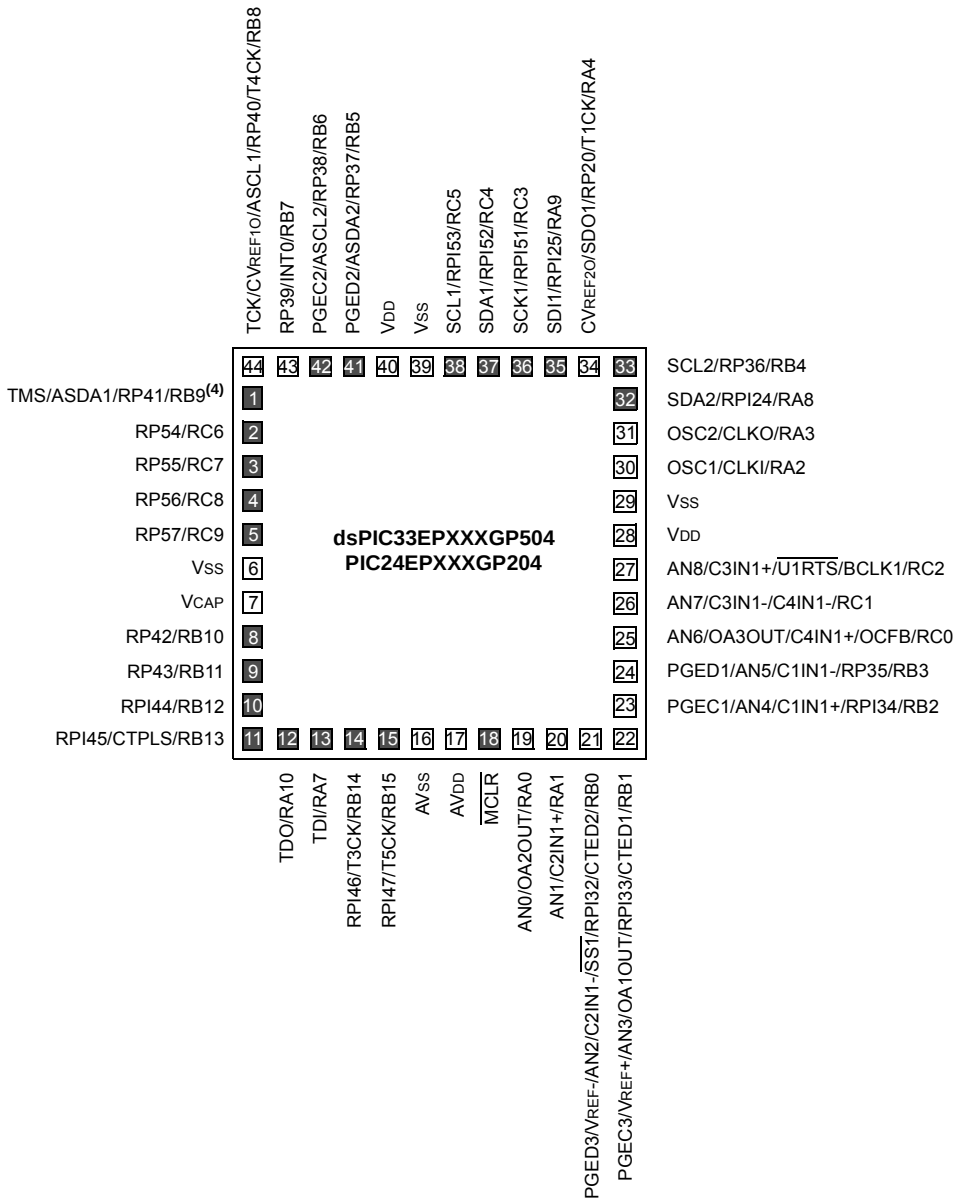
## Applications of "Embedded - Microcontrollers"

| Details | |
|---|---|
| Product Status | Active |
| Core Processor | PIC |
| Core Size | 16-Bit |
| Speed | 60 MIPs |
| Connectivity | I²C, IrDA, LINbus, SPI, UART/USART |
| Peripherals | Brown-out Detect/Reset, DMA, POR, PWM, WDT |
| Number of I/O | 35 |
| Program Memory Size | 256KB (85.5K x 24) |
| Program Memory Type | FLASH |
| EEPROM Size | - |
| RAM Size | 16K x 16 |
| Voltage - Supply (Vcc/Vdd) | 3V ~ 3.6V |
| Data Converters | A/D 9x10b/12b |
| Oscillator Type | Internal |
| Operating Temperature | -40°C ~ 125°C (TA) |
| Mounting Type | Surface Mount |
| Package / Case | 44-VFTLA Exposed Pad |
| Supplier Device Package | 44-VTLA (6x6) |
| Purchase URL | https://www.e-xfl.com/product-detail/microchip-technology/pic24ep256gp204-e-tl |

## Pin Diagrams (Continued)

**44-Pin VTLA(1,2,3)**

■ = Pins are up to 5V tolerant




**Note 1:** The RPn/RPIn pins can be used by any remappable peripheral with some limitation. See **Section 11.4 "Peripheral Pin Select (PPS)"** for available peripherals and for information on limitations.

**2:** Every I/O port pin (RAx-RGx) can be used as a Change Notification pin (CNAx-CNGx). See **Section 11.0 "I/O Ports"** for more information.

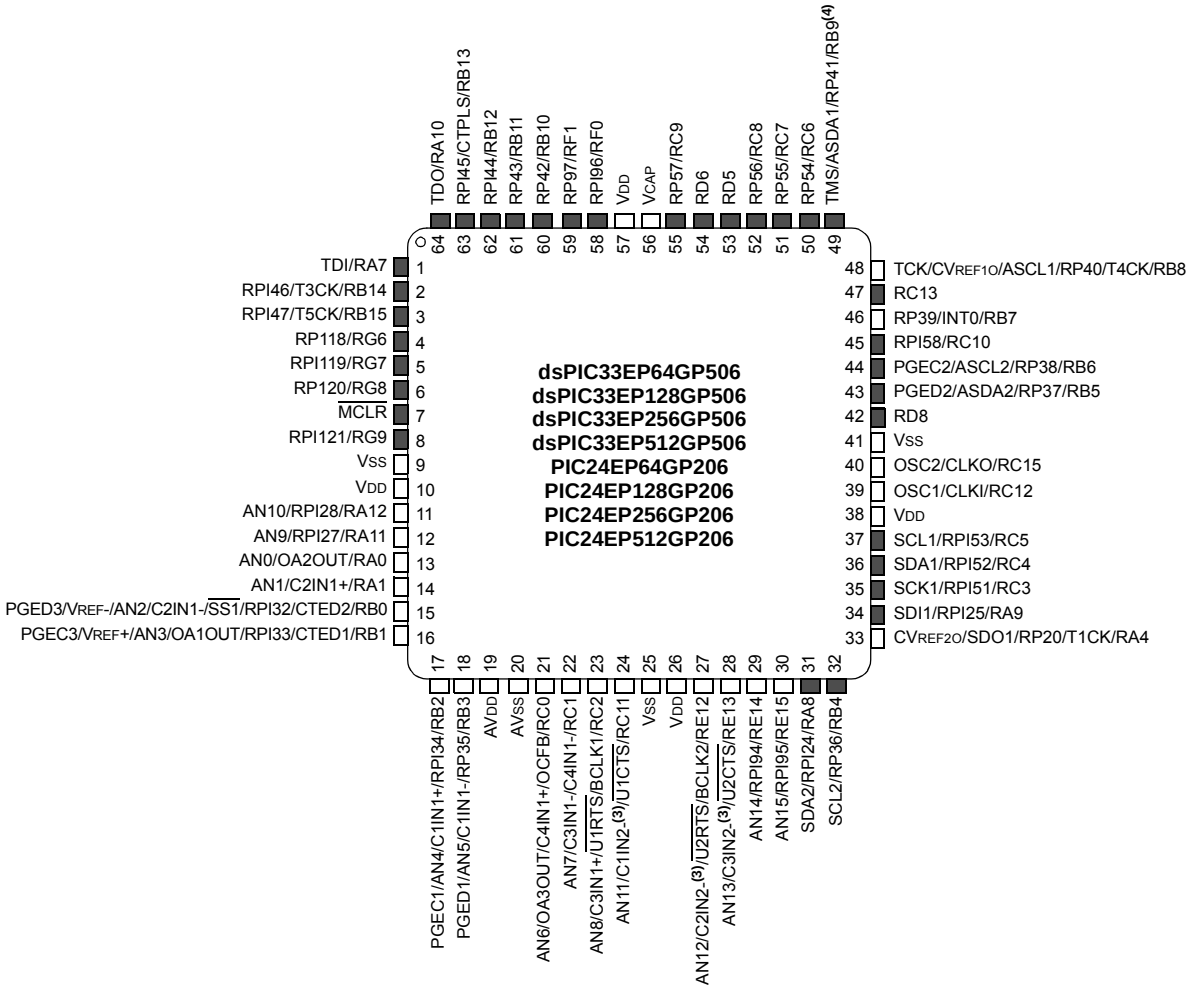
**3:** The metal pad at the bottom of the device is not connected to any pins and is recommended to be connected to VSS externally.

**4:** There is an internal pull-up resistor connected to the TMS pin when the JTAG interface is active. See the JTAGEN bit field in Table 27-2.

## Pin Diagrams (Continued)

**64-Pin TQFP(1,2,3)**

■ = Pins are up to 5V tolerant




**Note 1:** The RPn/RPIn pins can be used by any remappable peripheral with some limitation. See **Section 11.4 "Peripheral Pin Select (PPS)"** for available peripherals and for information on limitations.

**2:** Every I/O port pin (RAx-RGx) can be used as a Change Notification pin (CNAx-CNGx). See **Section 11.0 "I/O Ports"** for more information.

**3:** The metal pad at the bottom of the device is not connected to any pins and is recommended to be connected to VSS externally.

**4:** There is an internal pull-up resistor connected to the TMS pin when the JTAG interface is active. See the JTAGEN bit field in Table 27-2.

## 3.5 Programmer's Model

The programmer's model for the dsPIC33EPXXXGP50X, dsPIC33EPXXXMC20X/50X and PIC24EPXXXGP/MC20X is shown in Figure 3-2. All registers in the programmer's model are memory mapped and can be manipulated directly by instructions. Table 3-1 lists a description of each register.

In addition to the registers contained in the programmer's model, the dsPIC33EPXXXGP50X, dsPIC33EPXXXMC20X/50X and PIC24EPXXXGP/MC20X devices contain control registers for Modulo Addressing (dsPIC33EPXXXMC20X/50X and dsPIC33EPXXXGP50X devices only), Bit-Reversed Addressing (dsPIC33EPXXXMC20X/50X and dsPIC33EPXXXGP50X devices only) and interrupts. These registers are described in subsequent sections of this document.

All registers associated with the programmer's model are memory mapped, as shown in Table 4-1.

**TABLE 3-1: PROGRAMMER'S MODEL REGISTER DESCRIPTIONS**

| Register(s) Name | Description |
|---|---|
| W0 through W15 | Working Register Array |
| ACCA, ACCB | 40-Bit DSP Accumulators |
| PC | 23-Bit Program Counter |
| SR | ALU and DSP Engine STATUS Register |
| SPLIM | Stack Pointer Limit Value Register |
| TBLPAG | Table Memory Page Address Register |
| DSRPAG | Extended Data Space (EDS) Read Page Register |
| DSWPAG | Extended Data Space (EDS) Write Page Register |
| RCOUNT | REPEAT Loop Count Register |
| DCOUNT(1) | DO Loop Count Register |
| DOSTARTH(1,2), DOSTARTL(1,2) | DO Loop Start Address Register (High and Low) |
| DOENDH(1), DOENDL(1) | DO Loop End Address Register (High and Low) |
| CORCON | Contains DSP Engine, DO Loop Control and Trap Status bits |

**Note 1:** This register is available on dsPIC33EPXXXMC20X/50X and dsPIC33EPXXXGP50X devices only.

**2:** The DOSTARTH and DOSTARTL registers are read-only.

**TABLE 4-23: ECAN1 REGISTER MAP WHEN WIN (C1CTRL1<0>) = 1 FOR dsPIC33EPXXXMC/GP50X DEVICES ONLY (CONTINUED)**

| File Name | Addr | Bit 15 | Bit 14 | Bit 13 | Bit 12 | Bit 11 | Bit 10 | Bit 9 | Bit 8 | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 | All Resets |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| C1RXF11EID | 046E | EID<15:8> | | | | | | | | EID<7:0> | | | | | | | | xxxx |
| C1RXF12SID | 0470 | SID<10:3> | | | | | | | | SID<2:0> | | | — | EXIDE | — | EID<17:16> | | xxxx |
| C1RXF12EID | 0472 | EID<15:8> | | | | | | | | EID<7:0> | | | | | | | | xxxx |
| C1RXF13SID | 0474 | SID<10:3> | | | | | | | | SID<2:0> | | | — | EXIDE | — | EID<17:16> | | xxxx |
| C1RXF13EID | 0476 | EID<15:8> | | | | | | | | EID<7:0> | | | | | | | | xxxx |
| C1RXF14SID | 0478 | SID<10:3> | | | | | | | | SID<2:0> | | | — | EXIDE | — | EID<17:16> | | xxxx |
| C1RXF14EID | 047A | EID<15:8> | | | | | | | | EID<7:0> | | | | | | | | xxxx |
| C1RXF15SID | 047C | SID<10:3> | | | | | | | | SID<2:0> | | | — | EXIDE | — | EID<17:16> | | xxxx |
| C1RXF15EID | 047E | EID<15:8> | | | | | | | | EID<7:0> | | | | | | | | xxxx |

**Legend:** x = unknown value on Reset, — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

**TABLE 4-31: PERIPHERAL PIN SELECT INPUT REGISTER MAP FOR dsPIC33EPXXXGP50X DEVICES ONLY**

| File Name | Addr. | Bit 15 | Bit 14 | Bit 13 | Bit 12 | Bit 11 | Bit 10 | Bit 9 | Bit 8 | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 | All Resets |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| RPINR0 | 06A0 | — | INT1R<6:0> | | | | | | | — | — | — | — | — | — | — | — | 0000 |
| RPINR1 | 06A2 | — | — | — | — | — | — | — | — | — | INT2R<6:0> | | | | | | | 0000 |
| RPINR3 | 06A6 | — | — | — | — | — | — | — | — | — | T2CKR<6:0> | | | | | | | 0000 |
| RPINR7 | 06AE | — | IC2R<6:0> | | | | | | | — | IC1R<6:0> | | | | | | | 0000 |
| RPINR8 | 06B0 | — | IC4R<6:0> | | | | | | | — | IC3R<6:0> | | | | | | | 0000 |
| RPINR11 | 06B6 | — | — | — | — | — | — | — | — | — | OCFAR<6:0> | | | | | | | 0000 |
| RPINR18 | 06C4 | — | — | — | — | — | — | — | — | — | U1RXR<6:0> | | | | | | | 0000 |
| RPINR19 | 06C6 | — | — | — | — | — | — | — | — | — | U2RXR<6:0> | | | | | | | 0000 |
| RPINR22 | 06CC | — | SCK2INR<6:0> | | | | | | | — | SDI2R<6:0> | | | | | | | 0000 |
| RPINR23 | 06CE | — | — | — | — | — | — | — | — | — | SS2R<6:0> | | | | | | | 0000 |
| RPINR26 | 06D4 | — | — | — | — | — | — | — | — | — | C1RXR<6:0> | | | | | | | 0000 |

**Legend:** — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

**TABLE 4-32: PERIPHERAL PIN SELECT INPUT REGISTER MAP FOR dsPIC33EPXXXMC50X DEVICES ONLY**

| File Name | Addr. | Bit 15 | Bit 14 | Bit 13 | Bit 12 | Bit 11 | Bit 10 | Bit 9 | Bit 8 | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 | All Resets |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| RPINR0 | 06A0 | — | INT1R<6:0> | | | | | | | — | — | — | — | — | — | — | — | 0000 |
| RPINR1 | 06A2 | — | — | — | — | — | — | — | — | — | INT2R<6:0> | | | | | | | 0000 |
| RPINR3 | 06A6 | — | — | — | — | — | — | — | — | — | T2CKR<6:0> | | | | | | | 0000 |
| RPINR7 | 06AE | — | IC2R<6:0> | | | | | | | — | IC1R<6:0> | | | | | | | 0000 |
| RPINR8 | 06B0 | — | IC4R<6:0> | | | | | | | — | IC3R<6:0> | | | | | | | 0000 |
| RPINR11 | 06B6 | — | — | — | — | — | — | — | — | — | OCFAR<6:0> | | | | | | | 0000 |
| RPINR12 | 06B8 | — | FLT2R<6:0> | | | | | | | — | FLT1R<6:0> | | | | | | | 0000 |
| RPINR14 | 06BC | — | QEB1R<6:0> | | | | | | | — | QEA1R<6:0> | | | | | | | 0000 |
| RPINR15 | 06BE | — | HOME1R<6:0> | | | | | | | — | INDX1R<6:0> | | | | | | | 0000 |
| RPINR18 | 06C4 | — | — | — | — | — | — | — | — | — | U1RXR<6:0> | | | | | | | 0000 |
| RPINR19 | 06C6 | — | — | — | — | — | — | — | — | — | U2RXR<6:0> | | | | | | | 0000 |
| RPINR22 | 06CC | — | SCK2INR<6:0> | | | | | | | — | SDI2R<6:0> | | | | | | | 0000 |
| RPINR23 | 06CE | — | — | — | — | — | — | — | — | — | SS2R<6:0> | | | | | | | 0000 |
| RPINR26 | 06D4 | — | — | — | — | — | — | — | — | — | C1RXR<6:0> | | | | | | | 0000 |
| RPINR37 | 06EA | — | SYNCI1R<6:0> | | | | | | | — | — | — | — | — | — | — | — | 0000 |
| RPINR38 | 06EC | — | DTCMP1R<6:0> | | | | | | | — | — | — | — | — | — | — | — | 0000 |
| RPINR39 | 06EE | — | DTCMP3R<6:0> | | | | | | | — | DTCMP2R<6:0> | | | | | | | 0000 |

**Legend:** — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

## 4.5 Instruction Addressing Modes

The addressing modes shown in Table 4-63 form the basis of the addressing modes optimized to support the specific features of individual instructions. The addressing modes provided in the MAC class of instructions differ from those in the other instruction types.

### 4.5.1 FILE REGISTER INSTRUCTIONS

Most file register instructions use a 13-bit address field (f) to directly address data present in the first 8192 bytes of data memory (Near Data Space). Most file register instructions employ a working register, W0, which is denoted as WREG in these instructions. The destination is typically either the same file register or WREG (with the exception of the MUL instruction), which writes the result to a register or register pair. The MOV instruction allows additional flexibility and can access the entire Data Space.

### 4.5.2 MCU INSTRUCTIONS

The three-operand MCU instructions are of the form:

```
Operand 3 = Operand 1 <function> Operand 2
```

where Operand 1 is always a working register (that is, the addressing mode can only be Register Direct), which is referred to as Wb. Operand 2 can be a W register fetched from data memory or a 5-bit literal. The result location can either be a W register or a data memory location. The following addressing modes are supported by MCU instructions:

- Register Direct
- Register Indirect
- Register Indirect Post-Modified
- Register Indirect Pre-Modified
- 5-Bit or 10-Bit Literal

**Note:** Not all instructions support all the addressing modes given above. Individual instructions can support different subsets of these addressing modes.

**TABLE 4-63: FUNDAMENTAL ADDRESSING MODES SUPPORTED**

| Addressing Mode | Description |
|---|---|
| File Register Direct | The address of the file register is specified explicitly. |
| Register Direct | The contents of a register are accessed directly. |
| Register Indirect | The contents of Wn form the Effective Address (EA). |
| Register Indirect Post-Modified | The contents of Wn form the EA. Wn is post-modified (incremented or decremented) by a constant value. |
| Register Indirect Pre-Modified | Wn is pre-modified (incremented or decremented) by a signed constant value to form the EA. |
| Register Indirect with Register Offset (Register Indexed) | The sum of Wn and Wb forms the EA. |
| Register Indirect with Literal Offset | The sum of Wn and a literal forms the EA. |

**REGISTER 5-2: NVMADRH: NONVOLATILE MEMORY ADDRESS REGISTER HIGH**

| U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 |
|---|---|---|---|---|---|---|---|
| — | — | — | — | — | — | — | — |
| bit 15 | | | | | | | bit 8 |

| R/W-x | R/W-x | R/W-x | R/W-x | R/W-x | R/W-x | R/W-x | R/W-x |
|---|---|---|---|---|---|---|---|
| NVMADR<23:16> | | | | | | | |
| bit 7 | | | | | | | bit 0 |

| **Legend:** | | | |
|---|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as '0' | |
| -n = Value at POR | '1' = Bit is set | '0' = Bit is cleared | x = Bit is unknown |

bit 15-8 **Unimplemented:** Read as '0'

bit 7-0 **NVMADR<23:16>:** Nonvolatile Memory Write Address High bits

Selects the upper 8 bits of the location to program or erase in program Flash memory. This register may be read or written by the user application.

**REGISTER 5-3: NVMADRL: NONVOLATILE MEMORY ADDRESS REGISTER LOW**

| R/W-x | R/W-x | R/W-x | R/W-x | R/W-x | R/W-x | R/W-x | R/W-x |
|---|---|---|---|---|---|---|---|
| NVMADR<15:8> | | | | | | | |
| bit 15 | | | | | | | bit 8 |

| R/W-x | R/W-x | R/W-x | R/W-x | R/W-x | R/W-x | R/W-x | R/W-x |
|---|---|---|---|---|---|---|---|
| NVMADR<7:0> | | | | | | | |
| bit 7 | | | | | | | bit 0 |

| **Legend:** | | | |
|---|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as '0' | |
| -n = Value at POR | '1' = Bit is set | '0' = Bit is cleared | x = Bit is unknown |

bit 15-0 **NVMADR<15:0>:** Nonvolatile Memory Write Address Low bits

Selects the lower 16 bits of the location to program or erase in program Flash memory. This register may be read or written by the user application.

**REGISTER 5-4: NVMKEY: NONVOLATILE MEMORY KEY**

| U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 |
|---|---|---|---|---|---|---|---|
| — | — | — | — | — | — | — | — |
| bit 15 | | | | | | | bit 8 |

| W-0 | W-0 | W-0 | W-0 | W-0 | W-0 | W-0 | W-0 |
|---|---|---|---|---|---|---|---|
| NVMKEY<7:0> | | | | | | | |
| bit 7 | | | | | | | bit 0 |

| **Legend:** | | | |
|---|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as '0' | |
| -n = Value at POR | '1' = Bit is set | '0' = Bit is cleared | x = Bit is unknown |

bit 15-8 **Unimplemented:** Read as '0'

bit 7-0 **NVMKEY<7:0>:** Key Register (write-only) bits

**REGISTER 8-1: DMAxCON: DMA CHANNEL x CONTROL REGISTER**

| R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | U-0 | U-0 | U-0 |
|---|---|---|---|---|---|---|---|
| CHEN | SIZE | DIR | HALF | NULLW | — | — | — |
| bit 15 | | | | | | | bit 8 |

| U-0 | U-0 | R/W-0 | R/W-0 | U-0 | U-0 | R/W-0 | R/W-0 |
|---|---|---|---|---|---|---|---|
| — | — | AMODE1 | AMODE0 | — | — | MODE1 | MODE0 |
| bit 7 | | | | | | | bit 0 |

| **Legend:** | | | |
|---|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as '0' | |
| -n = Value at POR | '1' = Bit is set | '0' = Bit is cleared | x = Bit is unknown |

bit 15 **CHEN:** DMA Channel Enable bit
1 = Channel is enabled
0 = Channel is disabled

bit 14 **SIZE:** DMA Data Transfer Size bit
1 = Byte
0 = Word

bit 13 **DIR:** DMA Transfer Direction bit (source/destination bus select)
1 = Reads from RAM address, writes to peripheral address
0 = Reads from peripheral address, writes to RAM address

bit 12 **HALF:** DMA Block Transfer Interrupt Select bit
1 = Initiates interrupt when half of the data has been moved
0 = Initiates interrupt when all of the data has been moved

bit 11 **NULLW:** Null Data Peripheral Write Mode Select bit
1 = Null data write to peripheral in addition to RAM write (DIR bit must also be clear)
0 = Normal operation

bit 10-6 **Unimplemented:** Read as '0'

bit 5-4 **AMODE<1:0>:** DMA Channel Addressing Mode Select bits
11 = Reserved
10 = Peripheral Indirect Addressing mode
01 = Register Indirect without Post-Increment mode
00 = Register Indirect with Post-Increment mode

bit 3-2 **Unimplemented:** Read as '0'

bit 1-0 **MODE<1:0>:** DMA Channel Operating Mode Select bits
11 = One-Shot, Ping-Pong modes are enabled (one block transfer from/to each DMA buffer)
10 = Continuous, Ping-Pong modes are enabled
01 = One-Shot, Ping-Pong modes are disabled
00 = Continuous, Ping-Pong modes are disabled

**REGISTER 9-2: CLKDIV: CLOCK DIVISOR REGISTER (CONTINUED)**

bit 4-0 **PLLPRE<4:0>:** PLL Phase Detector Input Divider Select bits (also denoted as 'N1', PLL prescaler)
11111 = Input divided by 33
•
•
•
00001 = Input divided by 3
00000 = Input divided by 2 (default)

**Note 1:** The DOZE<2:0> bits can only be written to when the DOZEN bit is clear. If DOZEN = 1, any writes to DOZE<2:0> are ignored.

**2:** This bit is cleared when the ROI bit is set and an interrupt occurs.

**3:** The DOZEN bit cannot be set if DOZE<2:0> = 000. If DOZE<2:0> = 000, any attempt by user software to set the DOZEN bit is ignored.

# 17.0 QUADRATURE ENCODER INTERFACE (QEI) MODULE (dsPIC33EPXXXMC20X/50X and PIC24EPXXXMC20X DEVICES ONLY)

**Note 1:** This data sheet summarizes the features of the dsPIC33EPXXXGP50X, dsPIC33EPXXXMC20X/50X and PIC24EPXXXGP/MC20X families of devices. It is not intended to be a comprehensive reference source. To complement the information in this data sheet, refer to **"Quadrature Encoder Interface (QEI)"** (DS70601) in the "*dsPIC33/PIC24 Family Reference Manual*", which is available from the Microchip web site (www.microchip.com).

**2:** Some registers and associated bits described in this section may not be available on all devices. Refer to **Section 4.0 "Memory Organization"** in this data sheet for device-specific register and bit information.

This chapter describes the Quadrature Encoder Interface (QEI) module and associated operational modes. The QEI module provides the interface to incremental encoders for obtaining mechanical position data.

The operational features of the QEI module include:

- 32-Bit Position Counter
- 32-Bit Index Pulse Counter
- 32-Bit Interval Timer
- 16-Bit Velocity Counter
- 32-Bit Position Initialization/Capture/Compare High register
- 32-Bit Position Compare Low register
- x4 Quadrature Count mode
- External Up/Down Count mode
- External Gated Count mode
- External Gated Timer mode
- Internal Timer mode

Figure 17-1 illustrates the QEI block diagram.

**REGISTER 18-1: SPIxSTAT: SPIx STATUS AND CONTROL REGISTER (CONTINUED)**

bit 1 **SPITBF:** SPIx Transmit Buffer Full Status bit

1 = Transmit not yet started, SPIxTXB is full
0 = Transmit started, SPIxTXB is empty

Standard Buffer mode:
Automatically set in hardware when core writes to the SPIxBUF location, loading SPIxTXB. Automatically cleared in hardware when SPIx module transfers data from SPIxTXB to SPIxSR.

Enhanced Buffer mode:
Automatically set in hardware when the CPU writes to the SPIxBUF location, loading the last available buffer location. Automatically cleared in hardware when a buffer location is available for a CPU write operation.

bit 0 **SPIRBF:** SPIx Receive Buffer Full Status bit

1 = Receive is complete, SPIxRXB is full
0 = Receive is incomplete, SPIxRXB is empty

Standard Buffer mode:
Automatically set in hardware when SPIx transfers data from SPIxSR to SPIxRXB. Automatically cleared in hardware when the core reads the SPIxBUF location, reading SPIxRXB.

Enhanced Buffer mode:
Automatically set in hardware when SPIx transfers data from SPIxSR to the buffer, filling the last unread buffer location. Automatically cleared in hardware when a buffer location is available for a transfer from SPIxSR.

**REGISTER 19-2: I2CxSTAT: I2Cx STATUS REGISTER (CONTINUED)**

bit 3 **S:** Start bit
1 = Indicates that a Start (or Repeated Start) bit has been detected last
0 = Start bit was not detected last
Hardware is set or clear when a Start, Repeated Start or Stop is detected.

bit 2 **R_W:** Read/Write Information bit (when operating as $I^2C$ slave)
1 = Read – Indicates data transfer is output from the slave
0 = Write – Indicates data transfer is input to the slave
Hardware is set or clear after reception of an $I^2C$ device address byte.

bit 1 **RBF:** Receive Buffer Full Status bit
1 = Receive is complete, I2CxRCV is full
0 = Receive is not complete, I2CxRCV is empty
Hardware is set when I2CxRCV is written with a received byte. Hardware is clear when software reads I2CxRCV.

bit 0 **TBF:** Transmit Buffer Full Status bit
1 = Transmit in progress, I2CxTRN is full
0 = Transmit is complete, I2CxTRN is empty
Hardware is set when software writes to I2CxTRN. Hardware is clear at completion of a data transmission.

**REGISTER 21-2: CxCTRL2: ECANx CONTROL REGISTER 2**

| U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 |
|---|---|---|---|---|---|---|---|
| — | — | — | — | — | — | — | — |
| bit 15 | | | | | | | bit 8 |

| U-0 | U-0 | U-0 | R-0 | R-0 | R-0 | R-0 | R-0 |
|---|---|---|---|---|---|---|---|
| — | — | — | DNCNT4 | DNCNT3 | DNCNT2 | DNCNT1 | DNCNT0 |
| bit 7 | | | | | | | bit 0 |

| **Legend:** | | | |
|---|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as ‘0’ | |
| -n = Value at POR | ‘1’ = Bit is set | ‘0’ = Bit is cleared | x = Bit is unknown |

bit 15-5 **Unimplemented:** Read as ‘0’

bit 4-0 **DNCNT<4:0>:** DeviceNet™ Filter Bit Number bits

10010-11111 = Invalid selection
10001 = Compares up to Data Byte 3, bit 6 with EID<17>
•
•
•
00001 = Compares up to Data Byte 1, bit 7 with EID<0>
00000 = Does not compare data bytes

**REGISTER 23-7: AD1CSSH: ADC1 INPUT SCAN SELECT REGISTER HIGH(1)**

| R/W-0 | R/W-0 | U-0 | U-0 | U-0 | R/W-0 | R/W-0 | R/W-0 |
|---|---|---|---|---|---|---|---|
| CSS31 | CSS30 | — | — | — | CSS26(2) | CSS25(2) | CSS24(2) |
| bit 15 | | | | | | | bit 8 |

| U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 |
|---|---|---|---|---|---|---|---|
| — | — | — | — | — | — | — | — |
| bit 7 | | | | | | | bit 0 |

| **Legend:** | | | |
|---|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as '0' | |
| -n = Value at POR | '1' = Bit is set | '0' = Bit is cleared | x = Bit is unknown |

bit 15 **CSS31:** ADC1 Input Scan Selection bit
1 = Selects CTMU capacitive and time measurement for input scan (Open)
0 = Skips CTMU capacitive and time measurement for input scan (Open)

bit 14 **CSS30:** ADC1 Input Scan Selection bit
1 = Selects CTMU on-chip temperature measurement for input scan (CTMU TEMP)
0 = Skips CTMU on-chip temperature measurement for input scan (CTMU TEMP)

bit 13-11 **Unimplemented:** Read as '0'

bit 10 **CSS26:** ADC1 Input Scan Selection bit(2)
1 = Selects OA3/AN6 for input scan
0 = Skips OA3/AN6 for input scan

bit 9 **CSS25:** ADC1 Input Scan Selection bit(2)
1 = Selects OA2/AN0 for input scan
0 = Skips OA2/AN0 for input scan

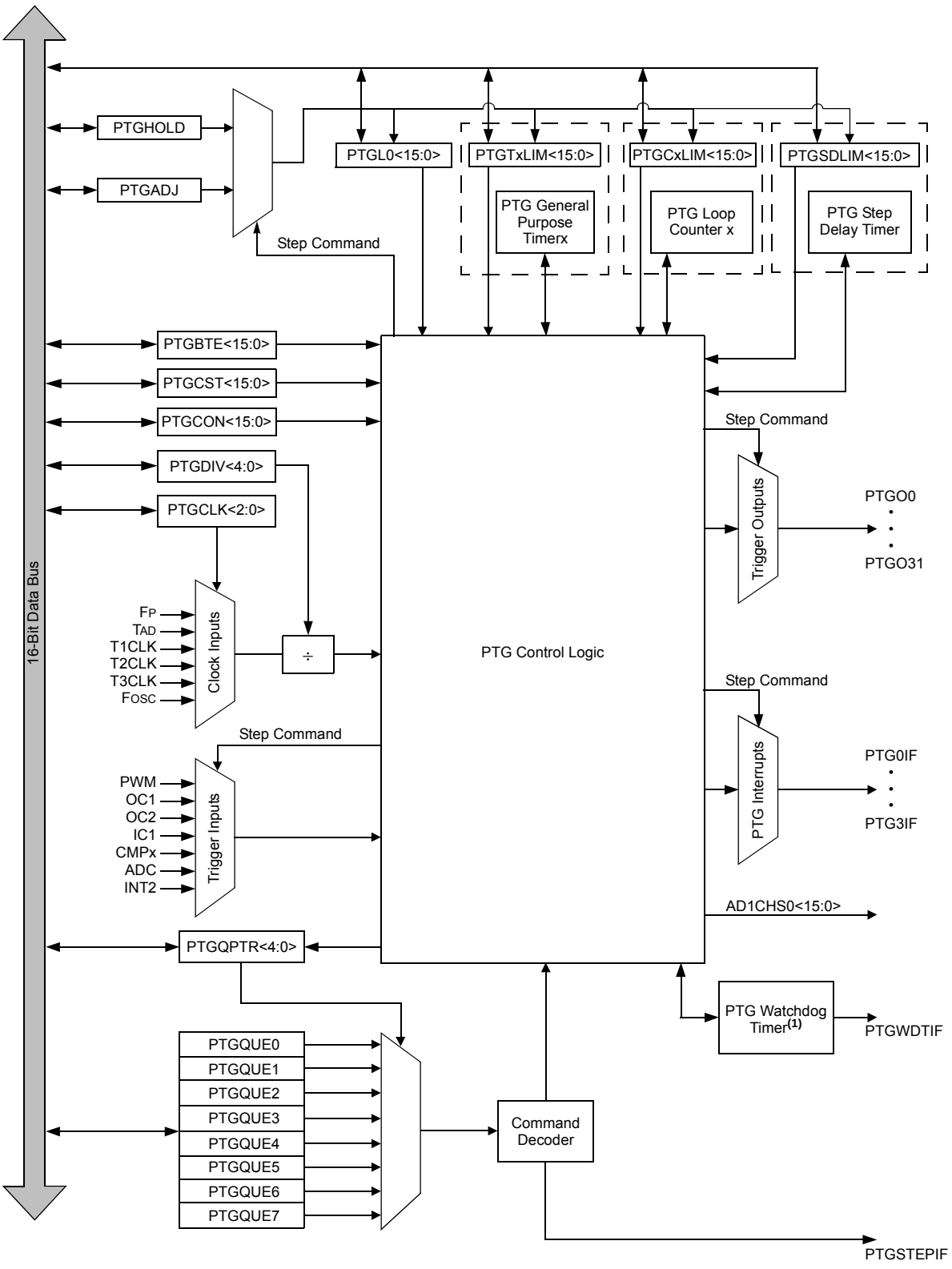
bit 8 **CSS24:** ADC1 Input Scan Selection bit(2)
1 = Selects OA1/AN3 for input scan
0 = Skips OA1/AN3 for input scan

bit 7-0 **Unimplemented:** Read as '0'

**Note 1:** All AD1CSSH bits can be selected by user software. However, inputs selected for scan, without a corresponding input on the device, convert VREFL.

**2:** The OAx input is used if the corresponding op amp is selected (OPMODE (CMxCON<10>) = 1); otherwise, the ANx input is used.

**FIGURE 24-1: PTG BLOCK DIAGRAM**




**Note 1:** This is a dedicated Watchdog Timer for the PTG module and is independent of the device Watchdog Timer.

**FIGURE 25-2: COMPARATOR MODULE BLOCK DIAGRAM (MODULE 4)**

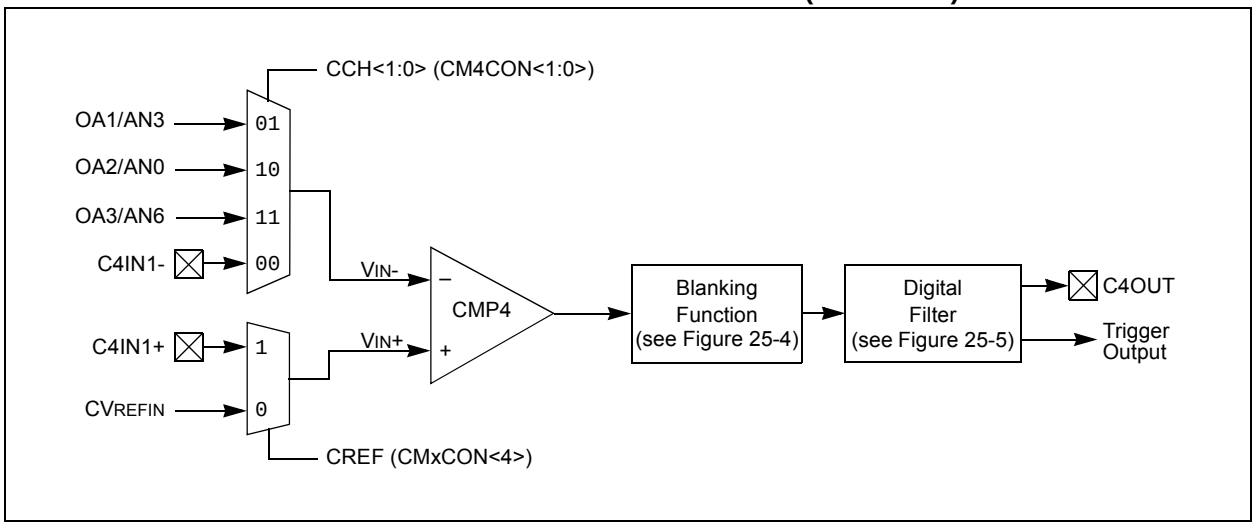
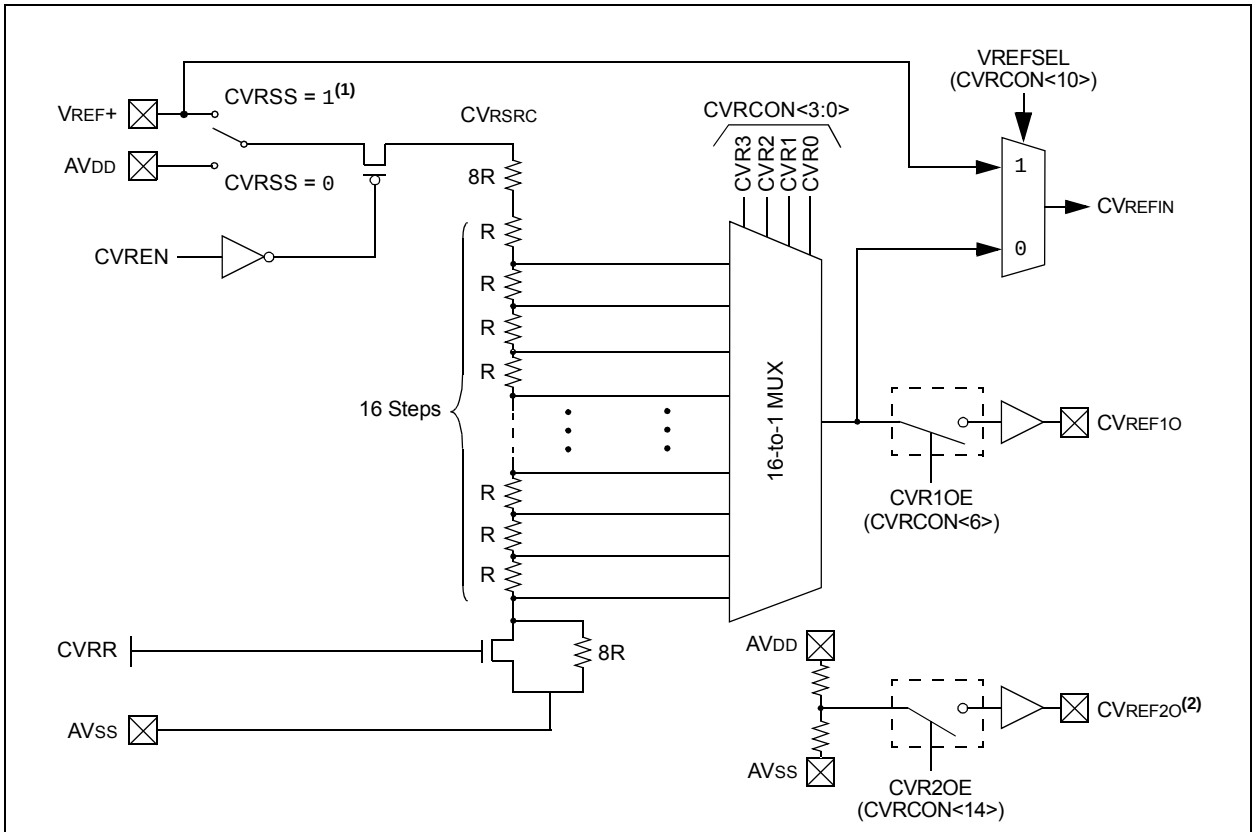



**FIGURE 25-3: OP AMP/COMPARATOR VOLTAGE REFERENCE BLOCK DIAGRAM**




**Note 1:** In order to operate with CVRSS = 1, at least one of the comparator modules must be enabled.

**2:** This reference is (AVDD + AVSS)/2.

**REGISTER 25-2: CMxCON: COMPARATOR x CONTROL REGISTER (x = 1, 2 OR 3)**

| R/W-0 | R/W-0 | R/W-0 | U-0 | U-0 | R/W-0 | R/W-0 | R/W-0 |
|---|---|---|---|---|---|---|---|
| CON | COE(2) | CPOL | — | — | OPMODE | CEVT | COUT |
| bit 15 | | | | | | | bit 8 |

| R/W-0 | R/W-0 | U-0 | R/W-0 | U-0 | U-0 | R/W-0 | R/W-0 |
|---|---|---|---|---|---|---|---|
| EVPOL1 | EVPOL0 | — | CREF(1) | — | — | CCH1(1) | CCH0(1) |
| bit 7 | | | | | | | bit 0 |

| **Legend:** | | | |
|---|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as '0' | |
| -n = Value at POR | '1' = Bit is set | '0' = Bit is cleared | x = Bit is unknown |

bit 15 **CON:** Op Amp/Comparator Enable bit
1 = Op amp/comparator is enabled
0 = Op amp/comparator is disabled

bit 14 **COE:** Comparator Output Enable bit(2)
1 = Comparator output is present on the CxOUT pin
0 = Comparator output is internal only

bit 13 **CPOL:** Comparator Output Polarity Select bit
1 = Comparator output is inverted
0 = Comparator output is not inverted

bit 12-11 **Unimplemented:** Read as '0'

bit 10 **OPMODE:** Op Amp/Comparator Operation Mode Select bit
1 = Circuit operates as an op amp
0 = Circuit operates as a comparator

bit 9 **CEVT:** Comparator Event bit
1 = Comparator event according to the EVPOL<1:0> settings occurred; disables future triggers and interrupts until the bit is cleared
0 = Comparator event did not occur

bit 8 **COUT:** Comparator Output bit
When CPOL = 0 (non-inverted polarity):
1 = $V_{IN+} > V_{IN-}$
0 = $V_{IN+} < V_{IN-}$
When CPOL = 1 (inverted polarity):
1 = $V_{IN+} < V_{IN-}$
0 = $V_{IN+} > V_{IN-}$

**Note 1:** Inputs that are selected and not available will be tied to $V_{SS}$. See the **"Pin Diagrams"** section for available inputs for each package.

**2:** This output is not available when OPMODE (CMxCON<10>) = 1.

**REGISTER 25-2: CMxCON: COMPARATOR x CONTROL REGISTER (x = 1, 2 OR 3) (CONTINUED)**

bit 7-6 **EVPOL<1:0>:** Trigger/Event/Interrupt Polarity Select bits
- 11 = Trigger/event/interrupt generated on any change of the comparator output (while CEVT = 0)
- 10 = Trigger/event/interrupt generated only on high-to-low transition of the polarity selected comparator output (while CEVT = 0)
  - If CPOL = 1 (inverted polarity):
    Low-to-high transition of the comparator output.
  - If CPOL = 0 (non-inverted polarity):
    High-to-low transition of the comparator output.
- 01 = Trigger/event/interrupt generated only on low-to-high transition of the polarity-selected comparator output (while CEVT = 0)
  - If CPOL = 1 (inverted polarity):
    High-to-low transition of the comparator output.
  - If CPOL = 0 (non-inverted polarity):
    Low-to-high transition of the comparator output
- 00 = Trigger/event/interrupt generation is disabled

bit 5 **Unimplemented:** Read as '0'

bit 4 **CREF:** Comparator Reference Select bit ($V_{IN+}$ input)(1)
- 1 = $V_{IN+}$ input connects to internal $CV_{REFIN}$ voltage(2)
- 0 = $V_{IN+}$ input connects to CxIN1+ pin

bit 3-2 **Unimplemented:** Read as '0'

bit 1-0 **CCH<1:0>:** Op Amp/Comparator Channel Select bits(1)
- 11 = Unimplemented
- 10 = Unimplemented
- 01 = Inverting input of the comparator connects to the CxIN2- pin(2)
- 00 = Inverting input of the op amp/comparator connects to the CxIN1- pin

**Note 1:** Inputs that are selected and not available will be tied to $V_{SS}$. See the **"Pin Diagrams"** section for available inputs for each package.

**2:** This output is not available when OPMODE (CMxCON<10>) = 1.

## 30.1 DC Characteristics

**TABLE 30-1: OPERATING MIPS VS. VOLTAGE**

| Characteristic | VDD Range (in Volts) | Temp Range (in °C) | Maximum MIPS |
|---|---|---|---|
| | | | dsPIC33EPXXXGP50X, dsPIC33EPXXXMC20X/50X and PIC24EPXXXGP/MC20X |
| — | 3.0V to 3.6V(1) | -40°C to +85°C | 70 |
| — | 3.0V to 3.6V(1) | -40°C to +125°C | 60 |

**Note 1:** Device is functional at VBORMIN < VDD < VDDMIN. Analog modules (ADC, op amp/comparator and comparator voltage reference) may have degraded performance. Device functionality is tested but not characterized. Refer to Parameter BO10 in Table 30-13 for the minimum and maximum BOR values.

**TABLE 30-2: THERMAL OPERATING CONDITIONS**

| Rating | Symbol | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|
| Industrial Temperature Devices | | | | | |
| Operating Junction Temperature Range | TJ | -40 | — | +125 | °C |
| Operating Ambient Temperature Range | TA | -40 | — | +85 | °C |
| Extended Temperature Devices | | | | | |
| Operating Junction Temperature Range | TJ | -40 | — | +140 | °C |
| Operating Ambient Temperature Range | TA | -40 | — | +125 | °C |
| Power Dissipation:<br>Internal chip power dissipation:<br>PINT = VDD x (IDD – Σ IOH)<br>I/O Pin Power Dissipation:<br>I/O = Σ ({VDD – VOH} x IOH) + Σ (VOL x IOL) | PD | PINT + PI/O | | | W |
| Maximum Allowed Power Dissipation | PDMAX | (TJ – TA)/θJA | | | W |

**TABLE 30-3: THERMAL PACKAGING CHARACTERISTICS**

| Characteristic | Symbol | Typ. | Max. | Unit | Notes |
|---|---|---|---|---|---|
| Package Thermal Resistance, 64-Pin QFN | θJA | 28.0 | — | °C/W | 1 |
| Package Thermal Resistance, 64-Pin TQFP 10x10 mm | θJA | 48.3 | — | °C/W | 1 |
| Package Thermal Resistance, 48-Pin UQFN 6x6 mm | θJA | 41 | — | °C/W | 1 |
| Package Thermal Resistance, 44-Pin QFN | θJA | 29.0 | — | °C/W | 1 |
| Package Thermal Resistance, 44-Pin TQFP 10x10 mm | θJA | 49.8 | — | °C/W | 1 |
| Package Thermal Resistance, 44-Pin VTLA 6x6 mm | θJA | 25.2 | — | °C/W | 1 |
| Package Thermal Resistance, 36-Pin VTLA 5x5 mm | θJA | 28.5 | — | °C/W | 1 |
| Package Thermal Resistance, 28-Pin QFN-S | θJA | 30.0 | — | °C/W | 1 |
| Package Thermal Resistance, 28-Pin SSOP | θJA | 71.0 | — | °C/W | 1 |
| Package Thermal Resistance, 28-Pin SOIC | θJA | 69.7 | — | °C/W | 1 |
| Package Thermal Resistance, 28-Pin SPDIP | θJA | 60.0 | — | °C/W | 1 |

**Note 1:** Junction to ambient thermal resistance, Theta-JA (θJA) numbers are achieved by package simulations.

**TABLE 30-11: DC CHARACTERISTICS: I/O PIN INPUT SPECIFICATIONS**

| DC CHARACTERISTICS | | | Standard Operating Conditions: 3.0V to 3.6V (unless otherwise stated)<br>Operating temperature -40°C ≤ TA ≤ +85°C for Industrial<br>-40°C ≤ TA ≤ +125°C for Extended | | | | |
|---|---|---|---|---|---|---|---|
| **Param No.** | **Symbol** | **Characteristic** | **Min.** | **Typ.** | **Max.** | **Units** | **Conditions** |
| | VIL | **Input Low Voltage** | | | | | |
| DI10 | | Any I/O Pin and $\overline{MCLR}$ | VSS | — | 0.2 VDD | V | |
| DI18 | | I/O Pins with SDAx, SCLx | VSS | — | 0.3 VDD | V | SMBus disabled |
| DI19 | | I/O Pins with SDAx, SCLx | VSS | — | 0.8 | V | SMBus enabled |
| | VIH | **Input High Voltage** | | | | | |
| DI20 | | I/O Pins Not 5V Tolerant | 0.8 VDD | — | VDD | V | **(Note 3)** |
| | | I/O Pins 5V Tolerant and $\overline{MCLR}$ | 0.8 VDD | — | 5.5 | V | **(Note 3)** |
| | | I/O Pins with SDAx, SCLx | 0.8 VDD | — | 5.5 | V | SMBus disabled |
| | | I/O Pins with SDAx, SCLx | 2.1 | — | 5.5 | V | SMBus enabled |
| | ICNPU | **Change Notification Pull-up Current** | | | | | |
| DI30 | | | 150 | 250 | 550 | μA | VDD = 3.3V, VPIN = VSS |
| | ICNPD | **Change Notification Pull-Down Current(4)** | | | | | |
| DI31 | | | 20 | 50 | 100 | μA | VDD = 3.3V, VPIN = VDD |

**Note 1:** The leakage current on the $\overline{MCLR}$ pin is strongly dependent on the applied voltage level. The specified levels represent normal operating conditions. Higher leakage current can be measured at different input voltages.

**2:** Negative current is defined as current sourced by the pin.

**3:** See the **"Pin Diagrams"** section for the 5V tolerant I/O pins.

**4:** VIL source < (VSS – 0.3). Characterized but not tested.

**5:** Non-5V tolerant pins VIH source > (VDD + 0.3), 5V tolerant pins VIH source > 5.5V. Characterized but not tested.

**6:** Digital 5V tolerant pins cannot tolerate any "positive" input injection current from input sources > 5.5V.

**7:** Non-zero injection currents can affect the ADC results by approximately 4-6 counts.

**8:** Any number and/or combination of I/O pins not excluded under IICL or IICH conditions are permitted provided the mathematical "absolute instantaneous" sum of the input injection currents from all pins do not exceed the specified limit. Characterized but not tested.