

Welcome to E-XFL.COM

What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "<u>Embedded -</u> <u>Microcontrollers</u>"

Details

E·XFI

Product Status	Obsolete
Core Processor	PIC
Core Size	16-Bit
Speed	60 MIPs
Connectivity	I ² C, IrDA, LINbus, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, DMA, POR, PWM, WDT
Number of I/O	35
Program Memory Size	256КВ (85.5К х 24)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	16K x 16
Voltage - Supply (Vcc/Vdd)	3V ~ 3.6V
Data Converters	A/D 9x10b/12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 150°C (TA)
Mounting Type	Surface Mount
Package / Case	44-VQFN Exposed Pad
Supplier Device Package	44-QFN (8x8)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/pic24ep256gp204-h-ml

Email: info@E-XFL.COM

Address: Room A, 16/F, Full Win Commercial Centre, 573 Nathan Road, Mongkok, Hong Kong



FIGURE 4-7: DATA MEMORY MAP FOR dsPIC33EP32MC20X/50X AND dsPIC33EP32GP50X DEVICES



FIGURE 4-8: DATA MEMORY MAP FOR dsPIC33EP64MC20X/50X AND dsPIC33EP64GP50X DEVICES

4.2.5 X AND Y DATA SPACES

The dsPIC33EPXXXMC20X/50X and dsPIC33EPXXXGP50X core has two Data Spaces, X and Y. These Data Spaces can be considered either separate (for some DSP instructions) or as one unified linear address range (for MCU instructions). The Data Spaces are accessed using two Address Generation Units (AGUs) and separate data paths. This feature allows certain instructions to concurrently fetch two words from RAM, thereby enabling efficient execution of DSP algorithms, such as Finite Impulse Response (FIR) filtering and Fast Fourier Transform (FFT).

The X Data Space is used by all instructions and supports all addressing modes. X Data Space has separate read and write data buses. The X read data bus is the read data path for all instructions that view Data Space as combined X and Y address space. It is also the X data prefetch path for the dual operand DSP instructions (MAC class).

The Y Data Space is used in concert with the X Data Space by the MAC class of instructions (CLR, ED, EDAC, MAC, MOVSAC, MPY, MPY. N and MSC) to provide two concurrent data read paths.

Both the X and Y Data Spaces support Modulo Addressing mode for all instructions, subject to addressing mode restrictions. Bit-Reversed Addressing mode is only supported for writes to X Data Space. Modulo Addressing and Bit-Reversed Addressing are not present in PIC24EPXXXGP/MC20X devices.

All data memory writes, including in DSP instructions, view Data Space as combined X and Y address space. The boundary between the X and Y Data Spaces is device-dependent and is not user-programmable.

4.3 Memory Resources

Many useful resources are provided on the main product page of the Microchip web site for the devices listed in this data sheet. This product page, which can be accessed using this link, contains the latest updates and additional information.

Note:	In the event you are not able to access the
	product page using the link above, enter
	this URL in your browser:
	http://www.microchip.com/wwwproducts/
	Devices.aspx?dDocName=en555464

4.3.1 KEY RESOURCES

- "Program Memory" (DS70613) in the "dsPIC33/ PIC24 Family Reference Manual"
- Code Samples
- Application Notes
- Software Libraries
- Webinars
- All Related *"dsPIC33/PIC24 Family Reference Manual"* Sections
- Development Tools

4.4.1 PAGED MEMORY SCHEME

The dsPIC33EPXXXGP50X, dsPIC33EPXXXMC20X/ 50X and PIC24EPXXXGP/MC20X architecture extends the available Data Space through a paging scheme, which allows the available Data Space to be accessed using MOV instructions in a linear fashion for pre-modified and post-modified Effective Addresses (EA). The upper half of the base Data Space address is used in conjunction with the Data Space Page registers, the 10-bit Read Page register (DSRPAG) or the 9-bit Write Page register (DSWPAG), to form an Extended Data Space (EDS) address or Program Space Visibility (PSV) address. The Data Space Page registers are located in the SFR space.

Construction of the EDS address is shown in Example 4-1. When DSRPAG<9> = 0 and the base address bit, EA<15> = 1, the DSRPAG<8:0> bits are concatenated onto EA<14:0> to form the 24-bit EDS read address. Similarly, when base address bit, EA<15> = 1, DSWPAG<8:0> are concatenated onto EA<14:0> to form the 24-bit EDS write address.





4.4.3 DATA MEMORY ARBITRATION AND BUS MASTER PRIORITY

EDS accesses from bus masters in the system are arbitrated.

The arbiter for data memory (including EDS) arbitrates between the CPU, the DMA and the ICD module. In the event of coincidental access to a bus by the bus masters, the arbiter determines which bus master access has the highest priority. The other bus masters are suspended and processed after the access of the bus by the bus master with the highest priority.

By default, the CPU is Bus Master 0 (M0) with the highest priority and the ICD is Bus Master 4 (M4) with the lowest priority. The remaining bus master (DMA Controller) is allocated to M3 (M1 and M2 are reserved and cannot be used). The user application may raise or lower the priority of the DMA Controller to be above that of the CPU by setting the appropriate bits in the EDS Bus Master Priority Control (MSTRPR) register. All bus masters with raised priorities will maintain the same priority relationship relative to each other (i.e., M1 being highest and M3 being lowest, with M2 in between). Also, all the bus masters with priorities below

FIGURE 4-18: ARBITER ARCHITECTURE

that of the CPU maintain the same priority relationship relative to each other. The priority schemes for bus masters with different MSTRPR values are tabulated in Table 4-62.

This bus master priority control allows the user application to manipulate the real-time response of the system, either statically during initialization or dynamically in response to real-time events.

TABLE 4-62:	DATA MEMORY BUS
	ARBITER PRIORITY

Briority	MSTRPR<15:0> Bit Setting ⁽¹⁾				
Phoney	0x0000	0x0020			
M0 (highest)	CPU	DMA			
M1	Reserved	CPU			
M2	Reserved	Reserved			
M3	DMA	Reserved			
M4 (lowest)	ICD	ICD			

Note 1: All other values of MSTRPR<15:0> are reserved.



10.3 Doze Mode

The preferred strategies for reducing power consumption are changing clock speed and invoking one of the powersaving modes. In some circumstances, this cannot be practical. For example, it may be necessary for an application to maintain uninterrupted synchronous communication, even while it is doing nothing else. Reducing system clock speed can introduce communication errors, while using a power-saving mode can stop communications completely.

Doze mode is a simple and effective alternative method to reduce power consumption while the device is still executing code. In this mode, the system clock continues to operate from the same source and at the same speed. Peripheral modules continue to be clocked at the same speed, while the CPU clock speed is reduced. Synchronization between the two clock domains is maintained, allowing the peripherals to access the SFRs while the CPU executes code at a slower rate.

Doze mode is enabled by setting the DOZEN bit (CLKDIV<11>). The ratio between peripheral and core clock speed is determined by the DOZE<2:0> bits (CLKDIV<14:12>). There are eight possible configurations, from 1:1 to 1:128, with 1:1 being the default setting.

Programs can use Doze mode to selectively reduce power consumption in event-driven applications. This allows clock-sensitive functions, such as synchronous communications, to continue without interruption while the CPU Idles, waiting for something to invoke an interrupt routine. An automatic return to full-speed CPU operation on interrupts can be enabled by setting the ROI bit (CLKDIV<15>). By default, interrupt events have no effect on Doze mode operation.

For example, suppose the device is operating at 20 MIPS and the ECAN[™] module has been configured for 500 kbps, based on this device operating speed. If the device is placed in Doze mode with a clock frequency ratio of 1:4, the ECAN module continues to communicate at the required bit rate of 500 kbps, but the CPU now starts executing instructions at a frequency of 5 MIPS.

10.4 Peripheral Module Disable

The Peripheral Module Disable (PMD) registers provide a method to disable a peripheral module by stopping all clock sources supplied to that module. When a peripheral is disabled using the appropriate PMD control bit, the peripheral is in a minimum power consumption state. The control and status registers associated with the peripheral are also disabled, so writes to those registers do not have effect and read values are invalid.

A peripheral module is enabled only if both the associated bit in the PMD register is cleared and the peripheral is supported by the specific dsPIC[®] DSC variant. If the peripheral is present in the device, it is enabled in the PMD register by default.

Note:	If a PMD bit is set, the corresponding
	module is disabled after a delay of one
	instruction cycle. Similarly, if a PMD bit is
	cleared, the corresponding module is
	enabled after a delay of one instruction
	cycle (assuming the module control regis-
	ters are already configured to enable
	module operation).

10.5 Power-Saving Resources

Many useful resources are provided on the main product page of the Microchip web site for the devices listed in this data sheet. This product page, which can be accessed using this link, contains the latest updates and additional information.



10.5.1 KEY RESOURCES

- "Watchdog Timer and Power-Saving Modes" (DS70615) in the "dsPIC33/PIC24 Family Reference Manual"
- Code Samples
- Application Notes
- Software Libraries
- Webinars
- All Related "dsPIC33/PIC24 Family Reference Manual" Sections
- Development Tools

12.2 Timer1 Control Register

R/W-0	U-0	R/W-0	U-0	U-0	U-0	U-0	U-0				
TON ⁽¹⁾	—	TSIDL	—	_	—	—	—				
bit 15 bit 8											
U-0	R/W-0	R/W-0	R/W-0	U-0	R/W-0	R/W-0	U-0				
	TGATE	TCKPS1	TCKPS0	_	TSYNC ⁽¹⁾	TCS ⁽¹⁾	—				
bit 7							bit 0				
Legend:											
R = Readab	ole bit	W = Writable	bit	U = Unimpler	mented bit, read	as '0'					
-n = Value a	at POR	'1' = Bit is set		'0' = Bit is cle	ared	x = Bit is unkn	own				
		(4)									
bit 15	TON: Timer1	On bit ⁽¹⁾									
	1 = Starts 16-	bit Limer1 bit Timer1									
bit 1/	Unimplement	ted: Pead as '	ı'								
bit 13		1 Stop in Idle N	/ode hit								
DIC 15	1 = Discontinu	i stop in lae k	eration when a	device enters l	dle mode						
	0 = Continues	module opera	tion in Idle mo	ode							
bit 12-7	Unimplement	Unimplemented: Read as '0'									
bit 6	TGATE: Time	TGATE: Timer1 Gated Time Accumulation Enable bit									
	When TCS =	<u>1:</u> prod									
	i nis più is ignorea.										
1 = Gated time accumulation is enabled											
0 = Gated time accumulation is disabled											
bit 5-4	TCKPS<1:0>	: Timer1 Input	Clock Prescal	e Select bits							
	11 = 1:256										
	10 = 1:64 01 = 1:8										
	01 = 1.0 00 = 1.1										
bit 3	Unimplement	ted: Read as ')'								
bit 2	TSYNC: Time	er1 External Clo	ock Input Sync	chronization Se	elect bit ⁽¹⁾						
	When TCS =	1:									
	1 = Synchroni	izes external cl	ock input								
	0 = Does not	synchronize ex	ternal clock in	nput							
	This bit is jand	<u>ored</u> .									
bit 1	TCS: Timer1 (Clock Source S	Select bit ⁽¹⁾								
	1 = External c	lock is from pir	n, T1CK (on th	ne rising edge)							
	0 = Internal cl	ock (FP)		5 5-7							
bit 0	Unimplement	ted: Read as ')'								
Note 1: \	When Timer1 is en attempts by user so	abled in Exterr oftware to write	al Synchrono to the TMR1	us Counter mo register are ig	ode (TCS = 1, T nored.	SYNC = 1, TO	N = 1), any				

REGISTER 12-1: T1CON: TIMER1 CONTROL REGISTER

© 2011-2013 Microchip Technology Inc.

13.2 Timer Control Registers

R/M/ 0	11.0		11.0	11.0	11.0	11.0	11.0			
	0-0		0-0	0-0	0-0	0-0	0-0			
bit 15		TOIDE	_							
51115							bit 0			
U-0	R/W-0	R/W-0	R/W-0	R/W-0	U-0	R/W-0	U-0			
	TGATE	TCKPS1	TCKPS0	T32	_	TCS	_			
bit 7							bit 0			
Legend:										
R = Readable I	bit	W = Writable	bit	U = Unimpler	nented bit, read	as '0'				
-n = Value at P	OR	'1' = Bit is set		'0' = Bit is cle	ared	x = Bit is unkn	iown			
bit 15	When T32 = 1 1 = Starts 32-1 0 = Stops 32-1 When T32 = 0 1 = Starts 16-1 0 = Stops 16-1	On bit L: bit Timerx/y bit Timerx/y <u>):</u> bit Timerx bit Timerx								
bit 14	Unimplemented: Read as '0'									
bit 13	TSIDL: Timerx Stop in Idle Mode bit									
	 1 = Discontinues module operation when device enters Idle mode 0 = Continues module operation in Idle mode 									
bit 12-7	Unimplemented: Read as '0'									
bit 6	TGATE: Timerx Gated Time Accumulation Enable bit When TCS = 1: This bit is ignored. When TCS = 0: 1 1 = Gated time accumulation is enabled 0 0 = Gated time accumulation is disabled									
bit 5-4	TCKPS<1:0>	: Timerx Input (Clock Prescal	e Select bits						
	11 = 1:256 10 = 1:64 01 = 1:8 00 = 1:1									
bit 3	T32: 32-Bit Til 1 = Timerx an 0 = Timerx an	mer Mode Sele d Timery form d Timery act as	ect bit a single 32-bit s two 16-bit tir	t timer ners						
bit 2	Unimplement	ted: Read as 'd	י)							
bit 1	TCS: Timerx (1 = External c 0 = Internal cl	Clock Source S clock is from pir ock (FP)	Select bit n, TxCK (on th	e rising edge)						
bit 0	Unimplement	ted: Read as ')'							

REGISTER 13-1: TxCON: (TIMER2 AND TIMER4) CONTROL REGISTER

dsPIC33EPXXXGP50X, dsPIC33EPXXXMC20X/50X AND PIC24EPXXXGP/MC20X

r								
R/W-0	R/W-0	R/W-0	R/W-0	U-0	U-0	U-0	R/W-0	
FLTMD	FLTOUT	FLTTRIEN	OCINV	—	—	—	OC32	
bit 15	15							
R/W-0	R/W-0, HS	R/W-0	R/W-0	R/W-1	R/W-1	R/W-0	R/W-0	
OCTRIC	G TRIGSTAT	OCTRIS	SYNCSEL4	SYNCSEL3	SYNCSEL2	SYNCSEL1	SYNCSEL0	
bit 7							bit 0	
r								
Legend:		HS = Hardwa	ire Settable bit					
R = Reada	able bit	W = Writable	bit	U = Unimplem	nented bit, read	l as '0'		
-n = Value	at POR	'1' = Bit is set	['0' = Bit is clea	ared	x = Bit is unkn	own	
bit 15	FLTMD: Fault	Mode Select I	bit					
	1 = Fault mo	de is maintain	ed until the Fa	ault source is r	removed; the c	orresponding	OCFLTx bit is	
	cleared in	n software and	a new PWM pe	eriod starts	loved and a po	N DWM poriod	etarte	
hit 14							Starts	
DIL 14	1 = PWM out	nut is driven h	iah on a Fault					
	0 = PWM out	put is driven lo	w on a Fault					
bit 13	FLTTRIEN: Fa	ault Output Sta	ate Select bit					
	1 = OCx pin i	s tri-stated on	a Fault conditio	on				
	0 = OCx pin I	/O state is def	ined by the FLT	OUT bit on a F	ault condition			
bit 12	OCINV: Outpu	ut Compare x I	nvert bit					
	1 = OCx outp	out is inverted	bo					
hit 11_9		ted: Read as '	0'					
bit 8	OC32. Casca	de Two OCx M	° Iodules Enable	hit (32-hit oper	ration)			
1 = Cascade module operation is enabled								
0 = Cascade module operation is disabled								
bit 7	OCTRIG: Out	put Compare >	k Trigger/Sync S	Select bit				
 1 = Triggers OCx from the source designated by the SYNCSELx bits 0 = Synchronizes OCx with the source designated by the SYNCSELx bits 								
bit 6	TRIGSTAT: Ti	mer Trigger St	atus bit	0 ,				
	1 = Timer sou	urce has been	triggered and is	s running				
	0 = Timer sou	urce has not be	een triggered a	nd is being held	d clear			
bit 5	OCTRIS: Out	put Compare x	Coutput Pin Dir	ection Select b	it			
	1 = OCx is tri	-stated						
		ompare x mod	ule drives the C	DCx pin				
Note 1:	Do not use the O	Cx module as i	its own Synchro	nization or Trig	ger source.			
2:	When the OCy module as a Trigg	odule is turned jer source, the	l OFF, it sends a OCy module m	a trigger out sig nust be unseled	gnal. If the OCx	module uses t source prior	he OCy to disabling it.	
3:	Each Output Com	ipare x module	e (OCx) has one	e PTG Trigger/S	Synchronization	n source. See S	Section 24.0	
	PTGO0 = OC1	Jei Generator			malion.			
	PTGO1 = OC2							
	PTGO2 = OC3							
	PTGO3 = OC4							

REGISTER 15-2: OCxCON2: OUTPUT COMPARE x CONTROL REGISTER 2

18.0 SERIAL PERIPHERAL INTERFACE (SPI)

- Note 1: This data sheet summarizes the features of the dsPIC33EPXXXGP50X, dsPIC33EPXXXMC20X/50X and PIC24EPXXXGP/MC20X families of devices. It is not intended to be a comprehensive reference source. To complement the information in this data sheet, refer to "Serial Peripheral Interface (SPI)" (DS70569) in the "dsPIC33/PIC24 Family Reference Manual", which is available from the Microchip web site (www.microchip.com).
 - Some registers and associated bits described in this section may not be available on all devices. Refer to Section 4.0 "Memory Organization" in this data sheet for device-specific register and bit information.

The SPI module is a synchronous serial interface, useful for communicating with other peripheral or microcontroller devices. These peripheral devices can be serial EEPROMs, shift registers, display drivers, ADC Converters, etc. The SPI module is compatible with Motorola[®] SPI and SIOP interfaces.

The dsPIC33EPXXXGP50X, dsPIC33EPXXXMC20X/ 50X and PIC24EPXXXGP/MC20X device family offers two SPI modules on a single device. These modules, which are designated as SPI1 and SPI2, are functionally identical. Each SPI module includes an eight-word FIFO buffer and allows DMA bus connections. When using the SPI module with DMA, FIFO operation can be disabled.

Note: In this section, the SPI modules are referred to together as SPIx, or separately as SPI1 and SPI2. Special Function Registers follow a similar notation. For example, SPIxCON refers to the control register for the SPI1 and SPI2 modules.

The SPI1 module uses dedicated pins which allow for a higher speed when using SPI1. The SPI2 module takes advantage of the Peripheral Pin Select (PPS) feature to allow for greater flexibility in pin configuration of the SPI2 module, but results in a lower maximum speed for SPI2. See **Section 30.0** "**Electrical Characteristics**" for more information.

The SPIx serial interface consists of four pins, as follows:

- SDIx: Serial Data Input
- SDOx: Serial Data Output
- SCKx: Shift Clock Input or Output
- SSx/FSYNCx: Active-Low Slave Select or Frame Synchronization I/O Pulse

The SPIx module can be configured to operate with two, three or four pins. In 3-pin mode, SSx is not used. In 2-pin mode, neither SDOx nor SSx is used.

Figure 18-1 illustrates the block diagram of the SPIx module in Standard and Enhanced modes.

27.5 Watchdog Timer (WDT)

For dsPIC33EPXXXGP50X, dsPIC33EPXXXMC20X/ 50X and PIC24EPXXXGP/MC20X devices, the WDT is driven by the LPRC oscillator. When the WDT is enabled, the clock source is also enabled.

27.5.1 PRESCALER/POSTSCALER

The nominal WDT clock source from LPRC is 32 kHz. This feeds a prescaler that can be configured for either 5-bit (divide-by-32) or 7-bit (divide-by-128) operation. The prescaler is set by the WDTPRE Configuration bit. With a 32 kHz input, the prescaler yields a WDT Timeout period (TWDT), as shown in Parameter SY12 in Table 30-22.

A variable postscaler divides down the WDT prescaler output and allows for a wide range of time-out periods. The postscaler is controlled by the WDTPOST<3:0> Configuration bits (FWDT<3:0>), which allow the selection of 16 settings, from 1:1 to 1:32,768. Using the prescaler and postscaler, time-out periods ranging from 1 ms to 131 seconds can be achieved.

The WDT, prescaler and postscaler are reset:

- · On any device Reset
- On the completion of a clock switch, whether invoked by software (i.e., setting the OSWEN bit after changing the NOSCx bits) or by hardware (i.e., Fail-Safe Clock Monitor)
- When a PWRSAV instruction is executed (i.e., Sleep or Idle mode is entered)
- When the device exits Sleep or Idle mode to resume normal operation
- By a CLRWDT instruction during normal execution
- Note: The CLRWDT and PWRSAV instructions clear the prescaler and postscaler counts when executed.



FIGURE 27-2: WDT BLOCK DIAGRAM

27.5.2 SLEEP AND IDLE MODES

If the WDT is enabled, it continues to run during Sleep or Idle modes. When the WDT time-out occurs, the device wakes the device and code execution continues from where the PWRSAV instruction was executed. The corresponding SLEEP or IDLE bit (RCON<3,2>) needs to be cleared in software after the device wakes up.

27.5.3 ENABLING WDT

The WDT is enabled or disabled by the FWDTEN Configuration bit in the FWDT Configuration register. When the FWDTEN Configuration bit is set, the WDT is always enabled.

The WDT can be optionally controlled in software when the FWDTEN Configuration bit has been programmed to '0'. The WDT is enabled in software by setting the SWDTEN control bit (RCON<5>). The SWDTEN control bit is cleared on any device Reset. The software WDT option allows the user application to enable the WDT for critical code segments and disable the WDT during non-critical segments for maximum power savings.

The WDT flag bit, WDTO (RCON<4>), is not automatically cleared following a WDT time-out. To detect subsequent WDT events, the flag must be cleared in software.

27.5.4 WDT WINDOW

The Watchdog Timer has an optional Windowed mode, enabled by programming the WINDIS bit in the WDT Configuration register (FWDT<6>). In the Windowed mode (WINDIS = 0), the WDT should be cleared based on the settings in the programmable Watchdog Timer Window select bits (WDTWIN<1:0>).

30.1 DC Characteristics

|--|

	haracteristic VDD Range Temp Range (in Volts) (in °C)		Maximum MIPS
Characteristic			dsPIC33EPXXXGP50X, dsPIC33EPXXXMC20X/50X and PIC24EPXXXGP/MC20X
	3.0V to 3.6V ⁽¹⁾	-40°C to +85°C	70
—	3.0V to 3.6V ⁽¹⁾	-40°C to +125°C	60

Note 1: Device is functional at VBORMIN < VDD < VDDMIN. Analog modules (ADC, op amp/comparator and comparator voltage reference) may have degraded performance. Device functionality is tested but not characterized. Refer to Parameter BO10 in Table 30-13 for the minimum and maximum BOR values.

TABLE 30-2: THERMAL OPERATING CONDITIONS

Rating	Symbol	Min.	Тур.	Max.	Unit
Industrial Temperature Devices					
Operating Junction Temperature Range	TJ	-40		+125	°C
Operating Ambient Temperature Range	TA	-40		+85	°C
Extended Temperature Devices					
Operating Junction Temperature Range	TJ	-40		+140	°C
Operating Ambient Temperature Range	TA	-40	_	+125	°C
Power Dissipation: Internal chip power dissipation: $PINT = VDD x (IDD - \Sigma IOH)$ I/O Pin Power Dissipation:	dissipation: $x (IDD - \Sigma IOH)$ PD PINT + PI/O pation:		W		
$I/O = \Sigma (\{VDD - VOH\} \times IOH) + \Sigma (VOL \times IOL)$					
Maximum Allowed Power Dissipation	PDMAX	(TJ — TA)/θJ	IA	W

TABLE 30-3: THERMAL PACKAGING CHARACTERISTICS

Characteristic	Symbol	Тур.	Max.	Unit	Notes
Package Thermal Resistance, 64-Pin QFN	θJA	28.0	_	°C/W	1
Package Thermal Resistance, 64-Pin TQFP 10x10 mm	θJA	48.3		°C/W	1
Package Thermal Resistance, 48-Pin UQFN 6x6 mm	θја	41	-	°C/W	1
Package Thermal Resistance, 44-Pin QFN	θJA	29.0		°C/W	1
Package Thermal Resistance, 44-Pin TQFP 10x10 mm	θја	49.8		°C/W	1
Package Thermal Resistance, 44-Pin VTLA 6x6 mm	θја	25.2	_	°C/W	1
Package Thermal Resistance, 36-Pin VTLA 5x5 mm	θJA	28.5		°C/W	1
Package Thermal Resistance, 28-Pin QFN-S	θја	30.0		°C/W	1
Package Thermal Resistance, 28-Pin SSOP	θја	71.0	_	°C/W	1
Package Thermal Resistance, 28-Pin SOIC	θJA	69.7	_	°C/W	1
Package Thermal Resistance, 28-Pin SPDIP	θJA	60.0	_	°C/W	1

Note 1: Junction to ambient thermal resistance, Theta-JA (θ JA) numbers are achieved by package simulations.

TABLE 30-40:SPI2 SLAVE MODE (FULL-DUPLEX, CKE = 0, CKP = 0, SMP = 0)TIMING REQUIREMENTS

AC CHARACTERISTICS			$\begin{tabular}{lllllllllllllllllllllllllllllllllll$					
Param.	Symbol	Characteristic ⁽¹⁾	Min.	Min. Typ. ⁽²⁾ Max. Units Co				
SP70	FscP	Maximum SCK2 Input Frequency	—	—	11	MHz	(Note 3)	
SP72	TscF	SCK2 Input Fall Time	—	-	_	ns	See Parameter DO32 (Note 4)	
SP73	TscR	SCK2 Input Rise Time	_	—	—	ns	See Parameter DO31 (Note 4)	
SP30	TdoF	SDO2 Data Output Fall Time			_	ns	See Parameter DO31 (Note 4)	
SP31	TdoR	SDO2 Data Output Rise Time	—	_	_	ns	See Parameter DO31 (Note 4)	
SP35	TscH2doV, TscL2doV	SDO2 Data Output Valid after SCK2 Edge	—	6	20	ns		
SP36	TdoV2scH, TdoV2scL	SDO2 Data Output Setup to First SCK2 Edge	30	_	_	ns		
SP40	TdiV2scH, TdiV2scL	Setup Time of SDI2 Data Input to SCK2 Edge	30	_	_	ns		
SP41	TscH2diL, TscL2diL	Hold Time of SDI2 Data Input to SCK2 Edge	30	—	_	ns		
SP50	TssL2scH, TssL2scL	$\overline{SS2}$ ↓ to SCK2 ↑ or SCK2 ↓ Input	120		—	ns		
SP51	TssH2doZ	SS2 ↑ to SDO2 Output High-Impedance	10	—	50	ns	(Note 4)	
SP52	TscH2ssH TscL2ssH	SS2 ↑ after SCK2 Edge	1.5 Tcy + 40	—		ns	(Note 4)	

Note 1: These parameters are characterized, but are not tested in manufacturing.

2: Data in "Typical" column is at 3.3V, +25°C unless otherwise stated.

3: The minimum clock period for SCK2 is 91 ns. Therefore, the SCK2 clock generated by the master must not violate this specification.

4: Assumes 50 pF load on all SPI2 pins.

TABLE 30-45:SPI1 SLAVE MODE (FULL-DUPLEX, CKE = 1, CKP = 0, SMP = 0)TIMING REQUIREMENTS

AC CHARACTERISTICS			$\begin{array}{l} \mbox{Standard Operating Conditions: 3.0V to 3.6V} \\ \mbox{(unless otherwise stated)} \\ \mbox{Operating temperature} & -40^{\circ}C \leq TA \leq +85^{\circ}C \mbox{ for Industrial} \\ & -40^{\circ}C \leq TA \leq +125^{\circ}C \mbox{ for Extended} \end{array}$					
Param.	aram. Symbol Characteristic ⁽¹⁾			Typ. ⁽²⁾	Max.	Units	Conditions	
SP70	FscP	Maximum SCK1 Input Frequency	_		Lesser of FP or 15	MHz	(Note 3)	
SP72	TscF	SCK1 Input Fall Time	—	-	—	ns	See Parameter DO32 (Note 4)	
SP73	TscR	SCK1 Input Rise Time	—	-	—	ns	See Parameter DO31 (Note 4)	
SP30	TdoF	SDO1 Data Output Fall Time	—	_	—	ns	See Parameter DO32 (Note 4)	
SP31	TdoR	SDO1 Data Output Rise Time	—	_	—	ns	See Parameter DO31 (Note 4)	
SP35	TscH2doV, TscL2doV	SDO1 Data Output Valid after SCK1 Edge	—	6	20	ns		
SP36	TdoV2scH, TdoV2scL	SDO1 Data Output Setup to First SCK1 Edge	30	_	—	ns		
SP40	TdiV2scH, TdiV2scL	Setup Time of SDI1 Data Input to SCK1 Edge	30	_	—	ns		
SP41	TscH2diL, TscL2diL	Hold Time of SDI1 Data Input to SCK1 Edge	30		—	ns		
SP50	TssL2scH, TssL2scL	SS1 ↓ to SCK1 ↑ or SCK1 ↓ Input	120	-	_	ns		
SP51	TssH2doZ	SS1 ↑ to SDO1 Output High-Impedance	10	_	50	ns	(Note 4)	
SP52	TscH2ssH TscL2ssH	SS1 ↑ after SCK1 Edge	1.5 TCY + 40	_	_	ns	(Note 4)	
SP60	TssL2doV	SDO1 Data Output Valid after SS1 Edge	_	_	50	ns		

Note 1: These parameters are characterized, but are not tested in manufacturing.

2: Data in "Typical" column is at 3.3V, +25°C unless otherwise stated.

3: The minimum clock period for SCK1 is 66.7 ns. Therefore, the SCK1 clock generated by the master must not violate this specification.

4: Assumes 50 pF load on all SPI1 pins.



FIGURE 30-29: SPI1 SLAVE MODE (FULL-DUPLEX, CKE = 0, CKP = 0, SMP = 0) TIMING CHARACTERISTICS

AC CHARACTERISTICS				$\begin{array}{l} \mbox{Standard Operating Conditions: 3.0V to 3.6V} \\ \mbox{(unless otherwise stated)} \\ \mbox{Operating temperature} & -40^{\circ}C \leq TA \leq +85^{\circ}C \mbox{ for Industrial} \\ & -40^{\circ}C \leq TA \leq +125^{\circ}C \mbox{ for Extended} \end{array}$				
Param. No.	Symbol	Characteristic ⁽³⁾		Min.	Min. Max.		Conditions	
IS10	S10 TLO:SCL Clock Low Time		100 kHz mode	4.7		μS		
			400 kHz mode	1.3	_	μS		
			1 MHz mode ⁽¹⁾	0.5	—	μS		
IS11	THI:SCL	Clock High Time	100 kHz mode	4.0	-	μS	Device must operate at a minimum of 1.5 MHz	
			400 kHz mode	0.6	—	μS	Device must operate at a minimum of 10 MHz	
			1 MHz mode ⁽¹⁾	0.5		μS		
IS20	TF:SCL	SDAx and SCLx	100 kHz mode	—	300	ns	CB is specified to be from	
		Fall Time	400 kHz mode	20 + 0.1 Св	300	ns	10 to 400 pF	
			1 MHz mode ⁽¹⁾	—	100	ns		
IS21	TR:SCL	SDAx and SCLx Rise Time	100 kHz mode	—	1000	ns	CB is specified to be from	
			400 kHz mode	20 + 0.1 Св	300	ns	10 to 400 pF	
			1 MHz mode ⁽¹⁾	—	300	ns		
IS25	TSU:DAT	Data Input Setup Time	100 kHz mode	250		ns		
			400 kHz mode	100		ns		
			1 MHz mode ⁽¹⁾	100		ns		
IS26	THD:DAT	Data Input Hold Time	100 kHz mode	0		μS		
			400 kHz mode	0	0.9	μS		
			1 MHz mode ⁽¹⁾	0	0.3	μS		
IS30	Tsu:sta	Start Condition Setup Time	100 kHz mode	4.7		μS	Only relevant for Repeated	
			400 kHz mode	0.6		μS	Start condition	
			1 MHz mode ⁽¹⁾	0.25	—	μS		
IS31	THD:STA	Start Condition Hold Time	100 kHz mode	4.0	—	μS	After this period, the first	
			400 kHz mode	0.6	—	μS	clock pulse is generated	
			1 MHz mode ⁽¹⁾	0.25	—	μS		
IS33	TSU:STO	TO Stop Condition Setup Time	100 kHz mode	4.7	—	μS		
			400 kHz mode	0.6	—	μS		
			1 MHz mode ⁽¹⁾	0.6	—	μS		
IS34	THD:STO	Stop Condition	100 kHz mode	4	—	μS		
		Hold Time	400 kHz mode	0.6	—	μS		
			1 MHz mode ⁽¹⁾	0.25		μS		
IS40	TAA:SCL	Output Valid From Clock	100 kHz mode	0	3500	ns		
			400 kHz mode	0	1000	ns		
			1 MHz mode ⁽¹⁾	0	350	ns		
IS45	TBF:SDA	Bus Free Time	100 kHz mode	4.7	—	μS	Time the bus must be free	
			400 kHz mode	1.3	—	μS	perore a new transmission	
			1 MHz mode ⁽¹⁾	0.5	—	μS	Call Stall	
IS50	Св	Bus Capacitive Loading		—	400	pF		
IS51	TPGD	Pulse Gobbler De	65	390	ns	(Note 2)		

TABLE 30-50: I2Cx BUS DATA TIMING REQUIREMENTS (SLAVE MODE)

Note 1: Maximum pin capacitance = 10 pF for all I2Cx pins (for 1 MHz mode only).

2: Typical value for this parameter is 130 ns.

3: These parameters are characterized, but not tested in manufacturing.

31.2 **AC Characteristics and Timing Parameters**

The information contained in this section defines dsPIC33EPXXXGP50X, dsPIC33EPXXXMC20X/50X and PIC24EPXXXGP/MC20X AC characteristics and timing parameters for high-temperature devices. However, all AC timing specifications in this section are the same as those in Section 30.2 "AC Characteristics and Timing Parameters", with the exception of the parameters listed in this section.

Parameters in this section begin with an H, which denotes High temperature. For example, Parameter OS53 in Section 30.2 "AC Characteristics and Timing Parameters" is the Industrial and Extended temperature equivalent of HOS53.

TABLE 31-9: TEMPERATURE AND VOLTAGE SPECIFICATIONS – AC

	Standard Operating Conditions: 3.0V to 3.6V
	(unless otherwise stated)
AC CHARACTERISTICS	Operating temperature $-40^{\circ}C \le TA \le +150^{\circ}C$
	Operating voltage VDD range as described in Table 31-1.

FIGURE 31-1: LOAD CONDITIONS FOR DEVICE TIMING SPECIFICATIONS



TABLE 31-10: PLL CLOCK TIMING SPECIFICATIONS

AC CHARACTERISTICS			Standard Operating Conditions: 3.0V to 3.6V(unless otherwise stated)Operating temperature $-40^{\circ}C \le TA \le +150^{\circ}C$				
Param No.	Symbol	Characteristic	Min Typ Max Units Conditio				Conditions
HOS53	DCLK	CLKO Stability (Jitter) ⁽¹⁾	-5	0.5	5	%	Measured over 100 ms period

These parameters are characterized by similarity, but are not tested in manufacturing. This specification is Note 1: based on clock cycle by clock cycle measurements. To calculate the effective jitter for individual time bases or communication clocks use this formula:

$$Peripheral Clock Jitter = \frac{DCLK}{\sqrt{\frac{FOSC}{Peripheral Bit Rate Clock}}}$$

For example: FOSC = 32 MHz, DCLK = 5%, SPIx bit rate clock (i.e., SCKx) is 2 MHz. Г

$$SPI SCK Jitter = \left\lfloor \frac{D_{CLK}}{\sqrt{\left(\frac{32 MHz}{2 MHz}\right)}} \right\rfloor = \left\lfloor \frac{5\%}{\sqrt{16}} \right\rfloor = \left\lfloor \frac{5\%}{4} \right\rfloor = 1.25\%$$

٦

© 2011-2013 Microchip Technology Inc.

32.0 DC AND AC DEVICE CHARACTERISTICS GRAPHS

Note: The graphs provided following this note are a statistical summary based on a limited number of samples and are provided for design guidance purposes only. The performance characteristics listed herein are not tested or guaranteed. In some graphs, the data presented may be outside the specified operating range (e.g., outside specified power supply range) and therefore, outside the warranted range.

FIGURE 32-1: VOH – 4x DRIVER PINS VOH (V) -0.050 -0.045 3.6V -0.040 3.3V -0.035 3V -0.030 IOH(A) -0.025 -0.020 Absolute Maximum -0.015 -0.010 -0.005 0.000 0.50 1.00 2.00 2.50 3.00 3.50 0.00 1.50 4.00

FIGURE 32-2: VOH – 8x DRIVER PINS





FIGURE 32-4: Vol – 8x DRIVER PINS



44-Lead Plastic Quad Flat, No Lead Package (ML) - 8x8 mm Body [QFN]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



	MILLIMETERS				
Dimension	MIN	NOM	MAX		
Contact Pitch	E	0.65 BSC			
Optional Center Pad Width	W2			6.60	
Optional Center Pad Length	T2			6.60	
Contact Pad Spacing	C1		8.00		
Contact Pad Spacing	C2		8.00		
Contact Pad Width (X44)	X1			0.35	
Contact Pad Length (X44)	Y1			0.85	
Distance Between Pads	G	0.25			

Notes:

1. Dimensioning and tolerancing per ASME Y14.5M

BSC: Basic Dimension. Theoretically exact value shown without tolerances.

Microchip Technology Drawing No. C04-2103B

64-Lead Plastic Quad Flat, No Lead Package (MR) – 9x9x0.9 mm Body with 5.40 x 5.40 Exposed Pad [QFN]



Microchip Technology Drawing C04-154A Sheet 1 of 2