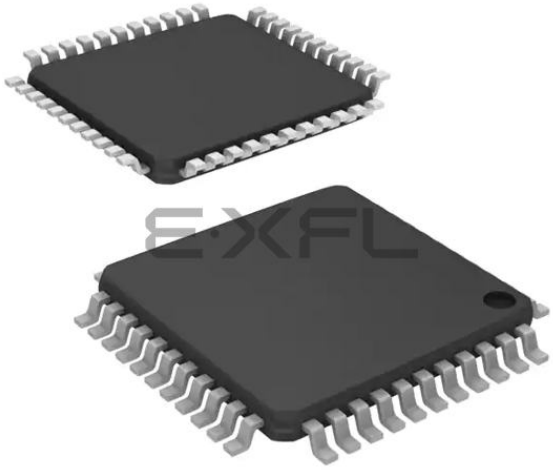

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Details	
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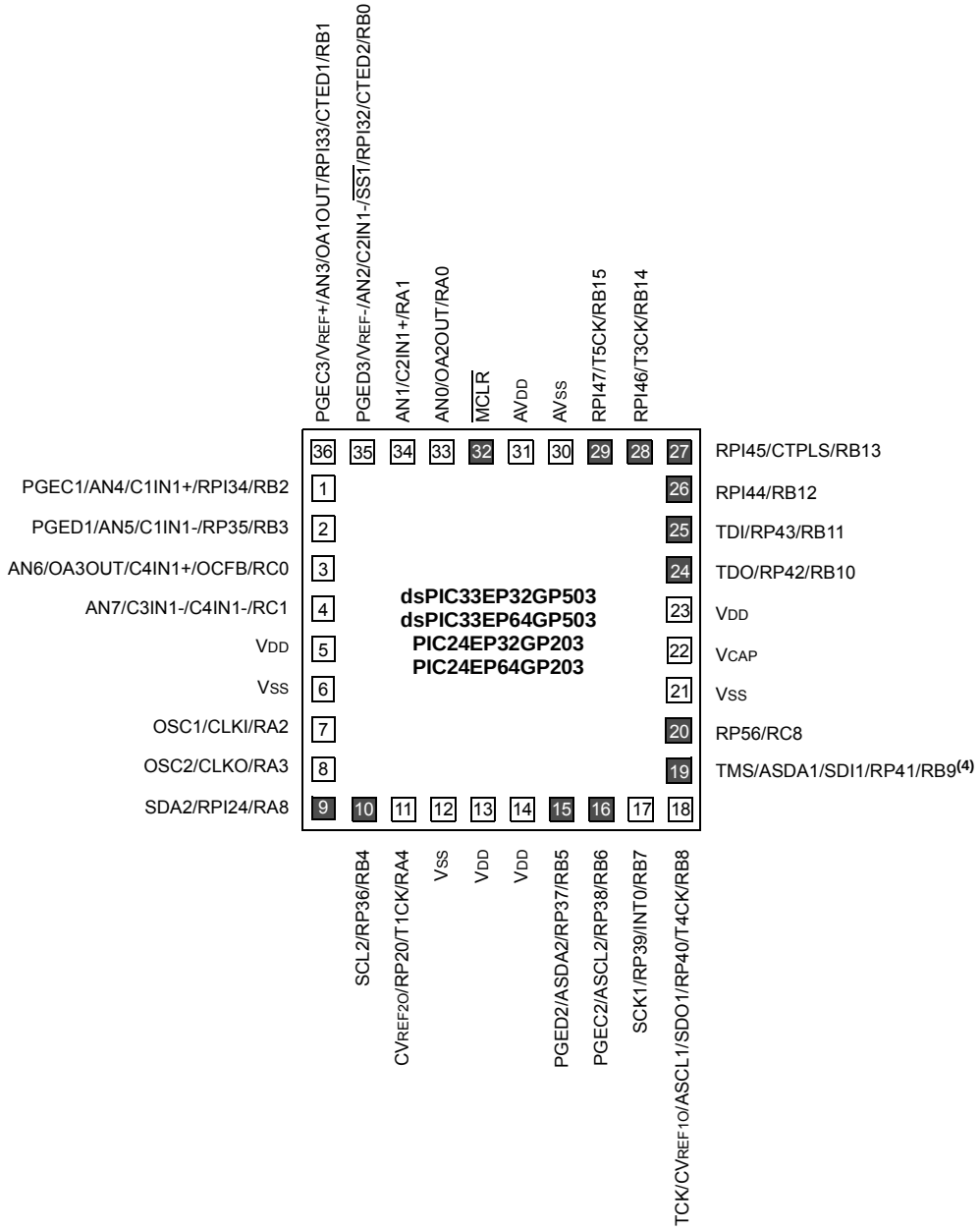
Peripherals	Brown-out Detect/Reset, DMA, POR, PWM, WDT
Number of I/O	35
Program Memory Size	256KB (85.5K x 24)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	16K x 16
Voltage - Supply (Vcc/Vdd)	3V ~ 3.6V
Data Converters	A/D 9x10b/12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 150°C (TA)
Mounting Type	Surface Mount
Package / Case	44-TQFP
Supplier Device Package	44-TQFP (10x10)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/pic24ep256gp204-h-pt

Pin Diagrams (Continued)

36-Pin VTLA(1,2,3)

■ = Pins are up to 5V tolerant



Note 1: The RPn/RPIn pins can be used by any remappable peripheral with some limitation. See **Section 11.4 "Peripheral Pin Select (PPS)"** for available peripherals and for information on limitations.

2: Every I/O port pin (RAx-RGx) can be used as a Change Notification pin (CNAx-CNGx). See **Section 11.0 "I/O Ports"** for more information.

3: The metal pad at the bottom of the device is not connected to any pins and is recommended to be connected to VSS externally.

4: There is an internal pull-up resistor connected to the TMS pin when the JTAG interface is active. See the JTAGEN bit field in Table 27-2.

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TABLE 4-29: PERIPHERAL PIN SELECT INPUT REGISTER MAP FOR PIC24EPXXXMC20X DEVICES ONLY

File Name	Addr.	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	All Resets
RPINR0	06A0	—	INT1R<6:0>							—	—	—	—	—	—	—	—	0000
RPINR1	06A2	—	—	—	—	—	—	—	—	—	INT2R<6:0>							0000
RPINR3	06A6	—	—	—	—	—	—	—	—	—	T2CKR<6:0>							0000
RPINR7	06AE	—	IC2R<6:0>							—	IC1R<6:0>							0000
RPINR8	06B0	—	IC4R<6:0>							—	IC3R<6:0>							0000
RPINR11	06B6	—	—	—	—	—	—	—	—	—	OCFAR<6:0>							0000
RPINR12	06B8	—	FLT2R<6:0>							—	FLT1R<6:0>							0000
RPINR14	06BC	—	QEB1R<6:0>							—	QEA1R<6:0>							0000
RPINR15	06BE	—	HOME1R<6:0>							—	INDX1R<6:0>							0000
RPINR18	06C4	—	—	—	—	—	—	—	—	—	U1RXR<6:0>							0000
RPINR19	06C6	—	—	—	—	—	—	—	—	—	U2RXR<6:0>							0000
RPINR22	06CC	—	SCK2INR<6:0>							—	SDI2R<6:0>							0000
RPINR23	06CE	—	—	—	—	—	—	—	—	—	SS2R<6:0>							0000
RPINR26	06D4	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
RPINR37	06EA	—	SYNCI1R<6:0>							—	—	—	—	—	—	—	—	0000
RPINR38	06EC	—	DTCMP1R<6:0>							—	—	—	—	—	—	—	—	0000
RPINR39	06EE	—	DTCMP3R<6:0>							—	DTCMP2R<6:0>							0000

Legend: — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

TABLE 4-30: PERIPHERAL PIN SELECT INPUT REGISTER MAP FOR PIC24EPXXXGP20X DEVICES ONLY

File Name	Addr.	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	All Resets
RPINR0	06A0	—	INT1R<6:0>							—	—	—	—	—	—	—	—	0000
RPINR1	06A2	—	—	—	—	—	—	—	—	—	INT2R<6:0>							0000
RPINR3	06A6	—	—	—	—	—	—	—	—	—	T2CKR<6:0>							0000
RPINR7	06AE	—	IC2R<6:0>							—	IC1R<6:0>							0000
RPINR8	06B0	—	IC4R<6:0>							—	IC3R<6:0>							0000
RPINR11	06B6	—	—	—	—	—	—	—	—	—	OCFAR<6:0>							0000
RPINR18	06C4	—	—	—	—	—	—	—	—	—	U1RXR<6:0>							0000
RPINR19	06C6	—	—	—	—	—	—	—	—	—	U2RXR<6:0>							0000
RPINR22	06CC	—	SCK2INR<6:0>							—	SDI2R<6:0>							0000
RPINR23	06CE	—	—	—	—	—	—	—	—	—	SS2R<6:0>							0000

Legend: — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

TABLE 4-42: OP AMP/COMPARATOR REGISTER MAP

File Name	Addr.	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	All Resets
CMSTAT	0A80	PSIDL	—	—	—	C4EVT	C3EVT	C2EVT	C1EVT	—	—	—	—	C4OUT	C3OUT	C2OUT	C1OUT	0000
CVRCON	0A82	—	CVR2OE	—	—	—	VREFSEL	—	—	CVREN	CVR1OE	CVRR	CVRSS	CVR<3:0>				0000
CM1CON	0A84	CON	COE	CPOL	—	—	OPMODE	CEVT	COUT	EVPOL<1:0>		—	CREF	—	—	CCH<1:0>		0000
CM1MSKSRC	0A86	—	—	—	—	SELSRCC<3:0>				SELSRCB<3:0>				SELSRCA<3:0>				0000
CM1MSKCON	0A88	HLMS	—	OCEN	OCNEN	OBEN	OBNEN	OAEN	OANEN	NAGS	PAGS	ACEN	ACNEN	ABEN	ABNEN	AAEN	AANEN	0000
CM1FLTR	0A8A	—	—	—	—	—	—	—	—	—	CFSEL<2:0>			CFLTREN	CFDIV<2:0>			0000
CM2CON	0A8C	CON	COE	CPOL	—	—	OPMODE	CEVT	COUT	EVPOL<1:0>		—	CREF	—	—	CCH<1:0>		0000
CM2MSKSRC	0A8E	—	—	—	—	SELSRCC<3:0>				SELSRCB<3:0>				SELSRCA<3:0>				0000
CM2MSKCON	0A90	HLMS	—	OCEN	OCNEN	OBEN	OBNEN	OAEN	OANEN	NAGS	PAGS	ACEN	ACNEN	ABEN	ABNEN	AAEN	AANEN	0000
CM2FLTR	0A92	—	—	—	—	—	—	—	—	—	CFSEL<2:0>			CFLTREN	CFDIV<2:0>			0000
CM3CON(1)	0A94	CON	COE	CPOL	—	—	OPMODE	CEVT	COUT	EVPOL<1:0>		—	CREF	—	—	CCH<1:0>		0000
CM3MSKSRC(1)	0A96	—	—	—	—	SELSRCC<3:0>				SELSRCB<3:0>				SELSRCA<3:0>				0000
CM3MSKCON(1)	0A98	HLMS	—	OCEN	OCNEN	OBEN	OBNEN	OAEN	OANEN	NAGS	PAGS	ACEN	ACNEN	ABEN	ABNEN	AAEN	AANEN	0000
CM3FLTR(1)	0A9A	—	—	—	—	—	—	—	—	—	CFSEL<2:0>			CFLTREN	CFDIV<2:0>			0000
CM4CON	0A9C	CON	COE	CPOL	—	—	—	CEVT	COUT	EVPOL<1:0>		—	CREF	—	—	CCH<1:0>		0000
CM4MSKSRC	0A9E	—	—	—	—	SELSRCC<3:0>				SELSRCB<3:0>				SELSRCA<3:0>				0000
CM4MSKCON	0AA0	HLMS	—	OCEN	OCNEN	OBEN	OBNEN	OAEN	OANEN	NAGS	PAGS	ACEN	ACNEN	ABEN	ABNEN	AAEN	AANEN	0000
CM4FLTR	0AA2	—	—	—	—	—	—	—	—	—	CFSEL<2:0>			CFLTREN	CFDIV<2:0>			0000

Legend: — = unimplemented, read as '0'. Reset values are shown in hexadecimal.
Note 1: These registers are unavailable on dsPIC33EPXXXGP502/MC502/MC202 and PIC24EP256GP/MC202 (28-pin) devices.

TABLE 4-43: CTMU REGISTER MAP

File Name	Addr.	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	All Resets
CTMUCON1	033A	CTMUEN	—	CTMUSIDL	TGEN	EDGEN	EDGSEQEN	IDISSEN	CTTRIG	—	—	—	—	—	—	—	—	0000
CTMUCON2	033C	EDG1MOD	EDG1POL	EDG1SEL<3:0>				EDG2STAT	EDG1STAT	EDG2MOD	EDG2POL	EDG2SEL<3:0>				—	—	0000
CTMUICON	033E	ITRIM<5:0>						IRNG<1:0>		—	—	—	—	—	—	—	—	0000

Legend: — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

TABLE 4-44: JTAG INTERFACE REGISTER MAP

File Name	Addr	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	All Resets
JDATAH	0FF0	—	—	—	—	JDATAH<27:16>												xxxx
JDATAL	0FF2	JDATAL<15:0>																0000

Legend: x = unknown value on Reset, — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

TABLE 4-52: PORTG REGISTER MAP FOR PIC24EPXXXGP/MC206 AND dsPIC33EPXXXGP/MC206/506 DEVICES ONLY

File Name	Addr.	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	All Resets
TRISG	0E60	—	—	—	—	—	—	TRISG9	TRISG8	TRISG7	TRISG6	—	—	—	—	—	—	03C0
PORTG	0E62	—	—	—	—	—	—	RG9	RG8	RG7	RG6	—	—	—	—	—	—	xxxx
LATG	0E64	—	—	—	—	—	—	LATG9	LATG8	LATG7	LATG6	—	—	—	—	—	—	xxxx
ODCG	0E66	—	—	—	—	—	—	ODCG9	ODCG8	ODCG7	ODCG6	—	—	—	—	—	—	0000
CNENG	0E68	—	—	—	—	—	—	CNIEG9	CNIEG8	CNIEG7	CNIEG6	—	—	—	—	—	—	0000
CNPUG	0E6A	—	—	—	—	—	—	CNPUG9	CNPUG8	CNPUG7	CNPUG6	—	—	—	—	—	—	0000
CNPDG	0E6C	—	—	—	—	—	—	CNPDG9	CNPDG8	CNPDG7	CNPDG6	—	—	—	—	—	—	0000

Legend: x = unknown value on Reset, — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

REGISTER 13-2: TyCON: (TIMER3 AND TIMER5) CONTROL REGISTER

R/W-0	U-0	R/W-0	U-0	U-0	U-0	U-0	U-0
TON(1)	—	TSIDL(2)	—	—	—	—	—
bit 15							bit 8

U-0	R/W-0	R/W-0	R/W-0	U-0	U-0	R/W-0	U-0
—	TGATE(1)	TCKPS1(1)	TCKPS0(1)	—	—	TCS(1,3)	—
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15 **TON:** Timery On bit(1)
1 = Starts 16-bit Timery
0 = Stops 16-bit Timery

bit 14 **Unimplemented:** Read as '0'

bit 13 **TSIDL:** Timery Stop in Idle Mode bit(2)
1 = Discontinues module operation when device enters Idle mode
0 = Continues module operation in Idle mode

bit 12-7 **Unimplemented:** Read as '0'

bit 6 **TGATE:** Timery Gated Time Accumulation Enable bit(1)
When TCS = 1:
This bit is ignored.
When TCS = 0:
1 = Gated time accumulation is enabled
0 = Gated time accumulation is disabled

bit 5-4 **TCKPS<1:0>:** Timery Input Clock Prescale Select bits(1)
11 = 1:256
10 = 1:64
01 = 1:8
00 = 1:1

bit 3-2 **Unimplemented:** Read as '0'

bit 1 **TCS:** Timery Clock Source Select bit(1,3)
1 = External clock is from pin, TyCK (on the rising edge)
0 = Internal clock (FP)

bit 0 **Unimplemented:** Read as '0'

Note 1: When 32-bit operation is enabled (T2CON<3> = 1), these bits have no effect on Timery operation; all timer functions are set through TxCON.

2: When 32-bit timer operation is enabled (T32 = 1) in the Timerx Control register (TxCON<3>), the TSIDL bit must be cleared to operate the 32-bit timer in Idle mode.

3: The TyCK pin is not available on all timers. See the **"Pin Diagrams"** section for the available pins.

14.2 Input Capture Registers

REGISTER 14-1: ICxCON1: INPUT CAPTURE x CONTROL REGISTER 1

U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	U-0	U-0
—	—	ICSIDL	ICTSEL2	ICTSEL1	ICTSEL0	—	—
bit 15							bit 8

U-0	R/W-0	R/W-0	R/HC/HS-0	R/HC/HS-0	R/W-0	R/W-0	R/W-0
—	ICI1	ICI0	ICOV	ICBNE	ICM2	ICM1	ICM0
bit 7							bit 0

Legend:	HC = Hardware Clearable bit	HS = Hardware Settable bit	
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15-14 **Unimplemented:** Read as '0'

bit 13 **ICSIDL:** Input Capture Stop in Idle Control bit
- 1 = Input capture will Halt in CPU Idle mode
- 0 = Input capture will continue to operate in CPU Idle mode

bit 12-10 **ICTSEL<2:0>:** Input Capture Timer Select bits
- 111 = Peripheral clock (FP) is the clock source of the ICx
- 110 = Reserved
- 101 = Reserved
- 100 = T1CLK is the clock source of the ICx (only the synchronous clock is supported)
- 011 = T5CLK is the clock source of the ICx
- 010 = T4CLK is the clock source of the ICx
- 001 = T2CLK is the clock source of the ICx
- 000 = T3CLK is the clock source of the ICx

bit 9-7 **Unimplemented:** Read as '0'

bit 6-5 **ICI<1:0>:** Number of Captures per Interrupt Select bits (this field is not used if ICM<2:0> = 001 or 111)
- 11 = Interrupt on every fourth capture event
- 10 = Interrupt on every third capture event
- 01 = Interrupt on every second capture event
- 00 = Interrupt on every capture event

bit 4 **ICOV:** Input Capture Overflow Status Flag bit (read-only)
- 1 = Input capture buffer overflow occurred
- 0 = No input capture buffer overflow occurred

bit 3 **ICBNE:** Input Capture Buffer Not Empty Status bit (read-only)
- 1 = Input capture buffer is not empty, at least one more capture value can be read
- 0 = Input capture buffer is empty

bit 2-0 **ICM<2:0>:** Input Capture Mode Select bits
- 111 = Input capture functions as interrupt pin only in CPU Sleep and Idle modes (rising edge detect only, all other control bits are not applicable)
- 110 = Unused (module is disabled)
- 101 = Capture mode, every 16th rising edge (Prescaler Capture mode)
- 100 = Capture mode, every 4th rising edge (Prescaler Capture mode)
- 011 = Capture mode, every rising edge (Simple Capture mode)
- 010 = Capture mode, every falling edge (Simple Capture mode)
- 001 = Capture mode, every edge rising and falling (Edge Detect mode (ICI<1:0>) is not used in this mode)
- 000 = Input capture module is turned off

REGISTER 17-19: INT1HLDH: INTERVAL 1 TIMER HOLD HIGH WORD REGISTER

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
INTHLD<31:24>							
bit 15							bit 8

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
INTHLD<23:16>							
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15-0 **INTHLD<31:16>:** Hold Register for Reading and Writing INT1TMRH bits

REGISTER 17-20: INT1HLDL: INTERVAL 1 TIMER HOLD LOW WORD REGISTER

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
INTHLD<15:8>							
bit 15							bit 8

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
INTHLD<7:0>							
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15-0 **INTHLD<15:0>:** Hold Register for Reading and Writing INT1TMRL bits

19.0 INTER-INTEGRATED CIRCUIT™ (I^2C™)

Note 1: This data sheet summarizes the features of the dsPIC33EPXXXGP50X, dsPIC33EPXXXMC20X/50X and PIC24EPXXXGP/MC20X families of devices. It is not intended to be a comprehensive reference source. To complement the information in this data sheet, refer to **"Inter-Integrated Circuit™ (I^2C™)"** (DS70330) in the "*dsPIC33/PIC24 Family Reference Manual*", which is available from the Microchip web site (www.microchip.com).

2: Some registers and associated bits described in this section may not be available on all devices. Refer to **Section 4.0 "Memory Organization"** in this data sheet for device-specific register and bit information.

3: There are minimum bit rates of approximately FCY/512. As a result, high processor speeds may not support 100 Kbit/second operation. See timing specifications, IM10 and IM11, and the **"Baud Rate Generator"** in the "*dsPIC33/PIC24 Family Reference Manual*".

The dsPIC33EPXXXGP50X, dsPIC33EPXXXMC20X/50X and PIC24EPXXXGP/MC20X family of devices contains two Inter-Integrated Circuit (I^2C) modules: I2C1 and I2C2.

The I^2C module provides complete hardware support for both Slave and Multi-Master modes of the I^2C serial communication standard, with a 16-bit interface.

The I^2C module has a 2-pin interface:

- The SCLx pin is clock
- The SDAx pin is data

The I^2C module offers the following key features:

- I^2C interface supporting both Master and Slave modes of operation
- I^2C Slave mode supports 7 and 10-bit addressing
- I^2C Master mode supports 7 and 10-bit addressing
- I^2C port allows bidirectional transfers between master and slaves
- Serial clock synchronization for I^2C port can be used as a handshake mechanism to suspend and resume serial transfer (SCLREL control)
- I^2C supports multi-master operation, detects bus collision and arbitrates accordingly
- Intelligent Platform Management Interface (IPMI) support
- System Management Bus (SMBus) support

20.1 UART Helpful Tips

1. In multi-node, direct-connect UART networks, UART receive inputs react to the complementary logic level defined by the URXINV bit (UxMODE<4>), which defines the Idle state, the default of which is logic high (i.e., URXINV = 0). Because remote devices do not initialize at the same time, it is likely that one of the devices, because the RX line is floating, will trigger a Start bit detection and will cause the first byte received, after the device has been initialized, to be invalid. To avoid this situation, the user should use a pull-up or pull-down resistor on the RX pin depending on the value of the URXINV bit.
   a) If URXINV = 0, use a pull-up resistor on the RX pin.
   b) If URXINV = 1, use a pull-down resistor on the RX pin.
2. The first character received on a wake-up from Sleep mode caused by activity on the UxRX pin of the UARTx module will be invalid. In Sleep mode, peripheral clocks are disabled. By the time the oscillator system has restarted and stabilized from Sleep mode, the baud rate bit sampling clock, relative to the incoming UxRX bit timing, is no longer synchronized, resulting in the first character being invalid; this is to be expected.

20.2 UART Resources

Many useful resources are provided on the main product page of the Microchip web site for the devices listed in this data sheet. This product page, which can be accessed using this link, contains the latest updates and additional information.

Note:	In the event you are not able to access the product page using the link above, enter this URL in your browser: http://www.microchip.com/wwwproducts/Devices.aspx?dDocName=en555464

20.2.1 KEY RESOURCES

- **"UART"** (DS70582) in the *"dsPIC33/PIC24 Family Reference Manual"*
- Code Samples
- Application Notes
- Software Libraries
- Webinars
- All Related *"dsPIC33/PIC24 Family Reference Manual"* Sections
- Development Tools

REGISTER 21-26: CxTRmnCON: ECANx TX/RX BUFFER mn CONTROL REGISTER (m = 0,2,4,6; n = 1,3,5,7)

R/W-0	R-0	R-0	R-0	R/W-0	R/W-0	R/W-0	R/W-0
TXENn	TXABTn	TXLARBn	TXERRn	TXREQn	RTRENn	TXnPRI1	TXnPRI0
bit 15							bit 8

R/W-0	R-0	R-0	R-0	R/W-0	R/W-0	R/W-0	R/W-0
TXENm	TXABTm(1)	TXLARBm(1)	TXERRm(1)	TXREQm	RTRENm	TXmPRI1	TXmPRI0
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15-8 See Definition for bits<7:0>, Controls Buffer n

bit 7 **TXENm:** TX/RX Buffer Selection bit
1 = Buffer TRBn is a transmit buffer
0 = Buffer TRBn is a receive buffer

bit 6 **TXABTm:** Message Aborted bit(1)
1 = Message was aborted
0 = Message completed transmission successfully

bit 5 **TXLARBm:** Message Lost Arbitration bit(1)
1 = Message lost arbitration while being sent
0 = Message did not lose arbitration while being sent

bit 4 **TXERRm:** Error Detected During Transmission bit(1)
1 = A bus error occurred while the message was being sent
0 = A bus error did not occur while the message was being sent

bit 3 **TXREQm:** Message Send Request bit
1 = Requests that a message be sent; the bit automatically clears when the message is successfully sent
0 = Clearing the bit to '0' while set requests a message abort

bit 2 **RTRENm:** Auto-Remote Transmit Enable bit
1 = When a remote transmit is received, TXREQ will be set
0 = When a remote transmit is received, TXREQ will be unaffected

bit 1-0 **TXmPRI<1:0>:** Message Transmission Priority bits
11 = Highest message priority
10 = High intermediate message priority
01 = Low intermediate message priority
00 = Lowest message priority

Note 1: This bit is cleared when TXREQ is set.

Note: The buffers, SID, EID, DLC, Data Field, and Receive Status registers are located in DMA RAM.

22.2 CTMU Control Registers

REGISTER 22-1: CTMUCON1: CTMU CONTROL REGISTER 1

R/W-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
CTMUEN	—	CTMUSIDL	TGEN	EDGEN	EDGSEQEN	IDISSEN(1)	CTTRIG
bit 15							bit 8

U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
—	—	—	—	—	—	—	—
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15 **CTMUEN:** CTMU Enable bit
1 = Module is enabled
0 = Module is disabled

bit 14 **Unimplemented:** Read as '0'

bit 13 **CTMUSIDL:** CTMU Stop in Idle Mode bit
1 = Discontinues module operation when device enters Idle mode
0 = Continues module operation in Idle mode

bit 12 **TGEN:** Time Generation Enable bit
1 = Enables edge delay generation
0 = Disables edge delay generation

bit 11 **EDGEN:** Edge Enable bit
1 = Hardware modules are used to trigger edges (TMRx, CTEDx, etc.)
0 = Software is used to trigger edges (manual set of EDGxSTAT)

bit 10 **EDGSEQEN:** Edge Sequence Enable bit
1 = Edge 1 event must occur before Edge 2 event can occur
0 = No edge sequence is needed

bit 9 **IDISSEN:** Analog Current Source Control bit(1)
1 = Analog current source output is grounded
0 = Analog current source output is not grounded

bit 8 **CTTRIG:** ADC Trigger Control bit
1 = CTMU triggers ADC start of conversion
0 = CTMU does not trigger ADC start of conversion

bit 7-0 **Unimplemented:** Read as '0'

Note 1: The ADC module Sample-and-Hold capacitor is not automatically discharged between sample/conversion cycles. Software using the ADC as part of a capacitance measurement must discharge the ADC capacitor before conducting the measurement. The IDISSEN bit, when set to '1', performs this function. The ADC must be sampling while the IDISSEN bit is active to connect the discharge sink to the capacitor array.

REGISTER 23-7: AD1CSSH: ADC1 INPUT SCAN SELECT REGISTER HIGH(1)

R/W-0	R/W-0	U-0	U-0	U-0	R/W-0	R/W-0	R/W-0
CSS31	CSS30	—	—	—	CSS26(2)	CSS25(2)	CSS24(2)
bit 15							bit 8

U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
—	—	—	—	—	—	—	—
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15 **CSS31:** ADC1 Input Scan Selection bit
1 = Selects CTMU capacitive and time measurement for input scan (Open)
0 = Skips CTMU capacitive and time measurement for input scan (Open)

bit 14 **CSS30:** ADC1 Input Scan Selection bit
1 = Selects CTMU on-chip temperature measurement for input scan (CTMU TEMP)
0 = Skips CTMU on-chip temperature measurement for input scan (CTMU TEMP)

bit 13-11 **Unimplemented:** Read as '0'

bit 10 **CSS26:** ADC1 Input Scan Selection bit(2)
1 = Selects OA3/AN6 for input scan
0 = Skips OA3/AN6 for input scan

bit 9 **CSS25:** ADC1 Input Scan Selection bit(2)
1 = Selects OA2/AN0 for input scan
0 = Skips OA2/AN0 for input scan

bit 8 **CSS24:** ADC1 Input Scan Selection bit(2)
1 = Selects OA1/AN3 for input scan
0 = Skips OA1/AN3 for input scan

bit 7-0 **Unimplemented:** Read as '0'

Note 1: All AD1CSSH bits can be selected by user software. However, inputs selected for scan, without a corresponding input on the device, convert VREFL.

2: The OAx input is used if the corresponding op amp is selected (OPMODE (CMxCON<10>) = 1); otherwise, the ANx input is used.

25.1.2 OP AMP CONFIGURATION B

Figure 25-7 shows a typical inverting amplifier circuit with the output of the op amp (OAxOUT) externally routed to a separate analog input pin (ANy) on the device. This op amp configuration is slightly different in terms of the op amp output and the ADC input connection, therefore, RINT1 is not included in the transfer function. However, this configuration requires the designer to externally route the op amp output (OAxOUT) to another analog input pin (ANy). See Table 30-53 in **Section 30.0 "Electrical Characteristics"** for the typical value of RINT1. Table 30-60 and Table 30-61 in **Section 30.0 "Electrical Characteristics"** describe the minimum sample time (TSAMP) requirements for the ADC module in this configuration.

Figure 25-7 also defines the equation to be used to calculate the expected voltage at point VOAxOUT. This is the typical inverting amplifier equation.

25.2 Op Amp/Comparator Resources

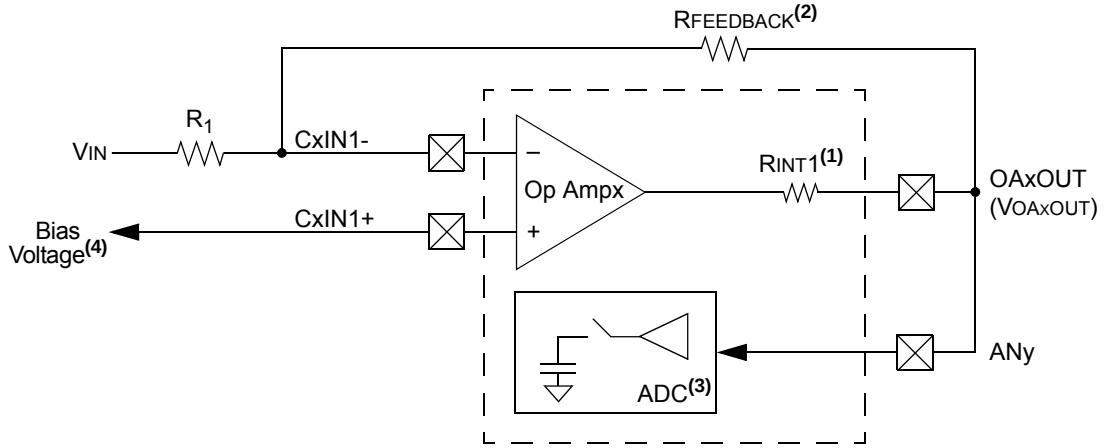
Many useful resources are provided on the main product page of the Microchip web site for the devices listed in this data sheet. This product page, which can be accessed using this link, contains the latest updates and additional information.

Note:	In the event you are not able to access the product page using the link above, enter this URL in your browser: http://www.microchip.com/wwwproducts/Devices.aspx?dDocName=en555464

25.2.1 KEY RESOURCES

- **"Op Amp/Comparator"** (DS70357) in the *"dsPIC33/PIC24 Family Reference Manual"*
- Code Samples
- Application Notes
- Software Libraries
- Webinars
- All Related *"dsPIC33/PIC24 Family Reference Manual"* Sections
- Development Tools

FIGURE 25-7: OP AMP CONFIGURATION B



$$V_{OAxOUT} = \left(\frac{R_{FEEDBACK}}{R_1}\right)(\ Bias\ Voltage - V_{IN} \ )$$

Note 1: See Table 30-53 for the Typical value.
2: See Table 30-53 for the Minimum value for the feedback resistor.
3: See Table 30-60 and Table 30-61 for the minimum sample time (TSAMP).
4: CVREF1O or CVREF2O are two options that are available for supplying bias voltage to the op amps.

REGISTER 25-7: CVRCON: COMPARATOR VOLTAGE REFERENCE CONTROL REGISTER

U-0	R/W-0	U-0	U-0	U-0	R/W-0	U-0	U-0
—	CVR2OE(1)	—	—	—	VREFSEL	—	—
bit 15							bit 8

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
CVREN	CVR1OE(1)	CVRR	CVRSS(2)	CVR3	CVR2	CVR1	CVR0
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15 **Unimplemented:** Read as '0'

bit 14 **CVR2OE:** Comparator Voltage Reference 2 Output Enable bit(1)
1 = (AVDD – AVSS)/2 is connected to the CVREF2O pin
0 = (AVDD – AVSS)/2 is disconnected from the CVREF2O pin

bit 13-11 **Unimplemented:** Read as '0'

bit 10 **VREFSEL:** Comparator Voltage Reference Select bit
1 = CVREFIN = VREF+
0 = CVREFIN is generated by the resistor network

bit 9-8 **Unimplemented:** Read as '0'

bit 7 **CVREN:** Comparator Voltage Reference Enable bit
1 = Comparator voltage reference circuit is powered on
0 = Comparator voltage reference circuit is powered down

bit 6 **CVR1OE:** Comparator Voltage Reference 1 Output Enable bit(1)
1 = Voltage level is output on the CVREF1O pin
0 = Voltage level is disconnected from then CVREF1O pin

bit 5 **CVRR:** Comparator Voltage Reference Range Selection bit
1 = CVRSRC/24 step-size
0 = CVRSRC/32 step-size

bit 4 **CVRSS:** Comparator Voltage Reference Source Selection bit(2)
1 = Comparator voltage reference source, CVRSRC = (VREF+) – (AVSS)
0 = Comparator voltage reference source, CVRSRC = AVDD – AVSS

bit 3-0 **CVR<3:0>** Comparator Voltage Reference Value Selection 0 ≤ CVR<3:0> ≤ 15 bits
When CVRR = 1:
CVREFIN = (CVR<3:0>/24) • (CVRSRC)
When CVRR = 0:
CVREFIN = (CVRSRC/4) + (CVR<3:0>/32) • (CVRSRC)

Note 1: CVRxOE overrides the TRISx and the ANSELx bit settings.
2: In order to operate with CVRSS = 1, at least one of the comparator modules must be enabled.

TABLE 28-2: INSTRUCTION SET OVERVIEW (CONTINUED)

Base Instr #	Assembly Mnemonic	Assembly Syntax		Description	# of Words	# of Cycles(2)	Status Flags Affected
25	DAW	DAW	Wn	Wn = decimal adjust Wn	1	1	C
26	DEC	DEC	f	f = f – 1	1	1	C,DC,N,OV,Z
		DEC	f,WREG	WREG = f – 1	1	1	C,DC,N,OV,Z
		DEC	Ws,Wd	Wd = Ws – 1	1	1	C,DC,N,OV,Z
27	DEC2	DEC2	f	f = f – 2	1	1	C,DC,N,OV,Z
		DEC2	f,WREG	WREG = f – 2	1	1	C,DC,N,OV,Z
		DEC2	Ws,Wd	Wd = Ws – 2	1	1	C,DC,N,OV,Z
28	DISI	DISI	#lit14	Disable Interrupts for k instruction cycles	1	1	None
29	DIV	DIV.S	Wm,Wn	Signed 16/16-bit Integer Divide	1	18	N,Z,C,OV
		DIV.SD	Wm,Wn	Signed 32/16-bit Integer Divide	1	18	N,Z,C,OV
		DIV.U	Wm,Wn	Unsigned 16/16-bit Integer Divide	1	18	N,Z,C,OV
		DIV.UD	Wm,Wn	Unsigned 32/16-bit Integer Divide	1	18	N,Z,C,OV
30	DIVF	DIVF	Wm,Wn(1)	Signed 16/16-bit Fractional Divide	1	18	N,Z,C,OV
31	DO	DO	#lit15,Expr(1)	Do code to PC + Expr, lit15 + 1 times	2	2	None
		DO	Wn,Expr(1)	Do code to PC + Expr, (Wn) + 1 times	2	2	None
32	ED	ED	Wm*Wm,Acc,Wx,Wy,Wxd(1)	Euclidean Distance (no accumulate)	1	1	OA,OB,OAB, SA,SB,SAB
33	EDAC	EDAC	Wm*Wm,Acc,Wx,Wy,Wxd(1)	Euclidean Distance	1	1	OA,OB,OAB, SA,SB,SAB
34	EXCH	EXCH	Wns,Wnd	Swap Wns with Wnd	1	1	None
35	FBCL	FBCL	Ws,Wnd	Find Bit Change from Left (MSb) Side	1	1	C
36	FF1L	FF1L	Ws,Wnd	Find First One from Left (MSb) Side	1	1	C
37	FF1R	FF1R	Ws,Wnd	Find First One from Right (LSb) Side	1	1	C
38	GOTO	GOTO	Expr	Go to address	2	4	None
		GOTO	Wn	Go to indirect	1	4	None
		GOTO.L	Wn	Go to indirect (long address)	1	4	None
39	INC	INC	f	f = f + 1	1	1	C,DC,N,OV,Z
		INC	f,WREG	WREG = f + 1	1	1	C,DC,N,OV,Z
		INC	Ws,Wd	Wd = Ws + 1	1	1	C,DC,N,OV,Z
40	INC2	INC2	f	f = f + 2	1	1	C,DC,N,OV,Z
		INC2	f,WREG	WREG = f + 2	1	1	C,DC,N,OV,Z
		INC2	Ws,Wd	Wd = Ws + 2	1	1	C,DC,N,OV,Z
41	IOR	IOR	f	f = f .IOR. WREG	1	1	N,Z
		IOR	f,WREG	WREG = f .IOR. WREG	1	1	N,Z
		IOR	#lit10,Wn	Wd = lit10 .IOR. Wd	1	1	N,Z
		IOR	Wb,Ws,Wd	Wd = Wb .IOR. Ws	1	1	N,Z
		IOR	Wb,#lit5,Wd	Wd = Wb .IOR. lit5	1	1	N,Z
42	LAC	LAC	Wso,#Slit4,Acc	Load Accumulator	1	1	OA,OB,OAB, SA,SB,SAB
43	LNK	LNK	#lit14	Link Frame Pointer	1	1	SFA
44	LSR	LSR	f	f = Logical Right Shift f	1	1	C,N,OV,Z
		LSR	f,WREG	WREG = Logical Right Shift f	1	1	C,N,OV,Z
		LSR	Ws,Wd	Wd = Logical Right Shift Ws	1	1	C,N,OV,Z
		LSR	Wb,Wns,Wnd	Wnd = Logical Right Shift Wb by Wns	1	1	N,Z
		LSR	Wb,#lit5,Wnd	Wnd = Logical Right Shift Wb by lit5	1	1	N,Z
45	MAC	MAC	Wm*Wn,Acc,Wx,Wxd,Wy,Wyd,AWB(1)	Multiply and Accumulate	1	1	OA,OB,OAB, SA,SB,SAB
		MAC	Wm*Wm,Acc,Wx,Wxd,Wy,Wyd(1)	Square and Accumulate	1	1	OA,OB,OAB, SA,SB,SAB

Note 1: These instructions are available in dsPIC33EPXXXMC20X/50X and PIC24EPXXXMC20X devices only.

2: Read and Read-Modify-Write (e.g., bit operations and logical operations) on non-CPU SFRs incur an additional instruction cycle.

29.2 MPLAB XC Compilers

The MPLAB XC Compilers are complete ANSI C compilers for all of Microchip's 8, 16 and 32-bit MCU and DSC devices. These compilers provide powerful integration capabilities, superior code optimization and ease of use. MPLAB XC Compilers run on Windows, Linux or MAC OS X.

For easy source level debugging, the compilers provide debug information that is optimized to the MPLAB X IDE.

The free MPLAB XC Compiler editions support all devices and commands, with no time or memory restrictions, and offer sufficient code optimization for most applications.

MPLAB XC Compilers include an assembler, linker and utilities. The assembler generates relocatable object files that can then be archived or linked with other relocatable object files and archives to create an executable file. MPLAB XC Compiler uses the assembler to produce its object file. Notable features of the assembler include:

- Support for the entire device instruction set
- Support for fixed-point and floating-point data
- Command-line interface
- Rich directive set
- Flexible macro language
- MPLAB X IDE compatibility

29.3 MPASM Assembler

The MPASM Assembler is a full-featured, universal macro assembler for PIC10/12/16/18 MCUs.

The MPASM Assembler generates relocatable object files for the MPLINK Object Linker, Intel® standard HEX files, MAP files to detail memory usage and symbol reference, absolute LST files that contain source lines and generated machine code, and COFF files for debugging.

The MPASM Assembler features include:

- Integration into MPLAB X IDE projects
- User-defined macros to streamline assembly code
- Conditional assembly for multipurpose source files
- Directives that allow complete control over the assembly process

29.4 MPLINK Object Linker/ MPLIB Object Librarian

The MPLINK Object Linker combines relocatable objects created by the MPASM Assembler. It can link relocatable objects from precompiled libraries, using directives from a linker script.

The MPLIB Object Librarian manages the creation and modification of library files of precompiled code. When a routine from a library is called from a source file, only the modules that contain that routine will be linked in with the application. This allows large libraries to be used efficiently in many different applications.

The object linker/library features include:

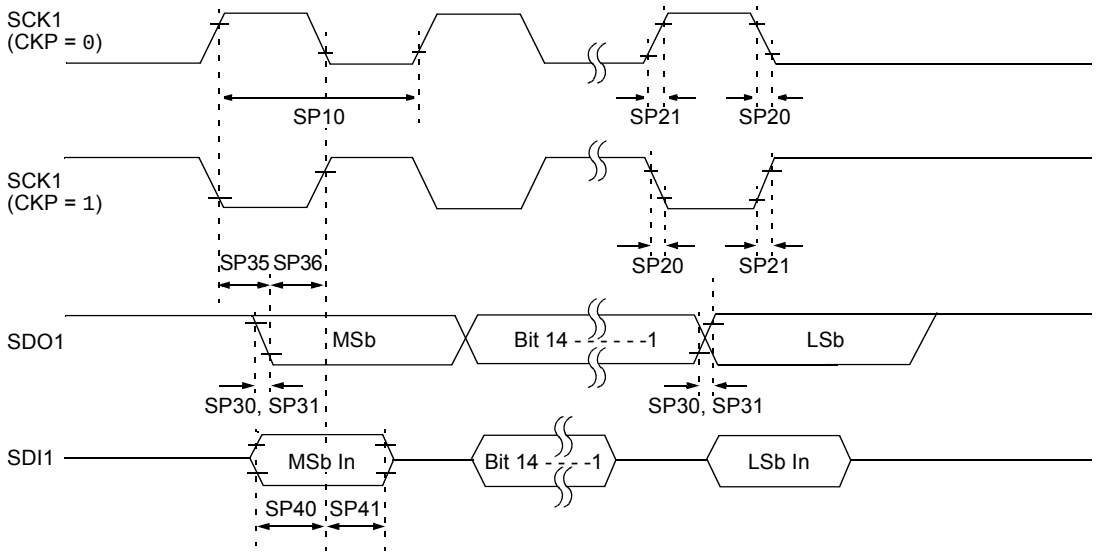
- Efficient linking of single libraries instead of many smaller files
- Enhanced code maintainability by grouping related modules together
- Flexible creation of libraries with easy module listing, replacement, deletion and extraction

29.5 MPLAB Assembler, Linker and Librarian for Various Device Families

MPLAB Assembler produces relocatable machine code from symbolic assembly language for PIC24, PIC32 and dsPIC DSC devices. MPLAB XC Compiler uses the assembler to produce its object file. The assembler generates relocatable object files that can then be archived or linked with other relocatable object files and archives to create an executable file. Notable features of the assembler include:

- Support for the entire device instruction set
- Support for fixed-point and floating-point data
- Command-line interface
- Rich directive set
- Flexible macro language
- MPLAB X IDE compatibility

FIGURE 30-25: SPI1 MASTER MODE (FULL-DUPLEX, CKE = 0, CKP = x, SMP = 1) TIMING CHARACTERISTICS



Note: Refer to Figure 30-1 for load conditions.

TABLE 30-44: SPI1 MASTER MODE (FULL-DUPLEX, CKE = 0, CKP = x, SMP = 1) TIMING REQUIREMENTS

AC CHARACTERISTICS			Standard Operating Conditions: 3.0V to 3.6V (unless otherwise stated) Operating temperature -40°C ≤ TA ≤ +85°C for Industrial -40°C ≤ TA ≤ +125°C for Extended				
Param.	**Symbol**	**Characteristic(1)**	**Min.**	**Typ.(2)**	**Max.**	**Units**	**Conditions**
SP10	FscP	Maximum SCK1 Frequency	—	—	10	MHz	-40ºC to +125ºC **(Note 3)**
SP20	TscF	SCK1 Output Fall Time	—	—	—	ns	See Parameter DO32 **(Note 4)**
SP21	TscR	SCK1 Output Rise Time	—	—	—	ns	See Parameter DO31 **(Note 4)**
SP30	TdoF	SDO1 Data Output Fall Time	—	—	—	ns	See Parameter DO32 **(Note 4)**
SP31	TdoR	SDO1 Data Output Rise Time	—	—	—	ns	See Parameter DO31 **(Note 4)**
SP35	TscH2doV, TscL2doV	SDO1 Data Output Valid after SCK1 Edge	—	6	20	ns	
SP36	TdoV2scH, TdoV2scL	SDO1 Data Output Setup to First SCK1 Edge	30	—	—	ns	
SP40	TdiV2scH, TdiV2scL	Setup Time of SDI1 Data Input to SCK1 Edge	30	—	—	ns	
SP41	TscH2diL, TscL2diL	Hold Time of SDI1 Data Input to SCK1 Edge	30	—	—	ns	

Note 1: These parameters are characterized, but are not tested in manufacturing.

2: Data in "Typical" column is at 3.3V, +25°C unless otherwise stated.

3: The minimum clock period for SCK1 is 100 ns. The clock generated in Master mode must not violate this specification.

4: Assumes 50 pF load on all SPI1 pins.

TABLE 30-53: OP AMP/COMPARATOR SPECIFICATIONS

DC CHARACTERISTICS			Standard Operating Conditions: 3.0V to 3.6V (unless otherwise stated)(1) Operating temperature -40°C ≤ TA ≤ +85°C for Industrial -40°C ≤ TA ≤ +125°C for Extended				
Param No.	**Symbol**	**Characteristic**	**Min.**	**Typ.(2)**	**Max.**	**Units**	**Conditions**
Comparator AC Characteristics							
CM10	TRESP	Response Time(3)	—	19	—	ns	V+ input step of 100 mV, V- input held at VDD/2
CM11	TMC2OV	Comparator Mode Change to Output Valid	—	—	10	µs	
Comparator DC Characteristics							
CM30	VOFFSET	Comparator Offset Voltage	—	±10	40	mV	
CM31	VHYST	Input Hysteresis Voltage(3)	—	30	—	mV	
CM32	TRISE/ TFALL	Comparator Output Rise/ Fall Time(3)	—	20	—	ns	1 pF load capacitance on input
CM33	VGAIN	Open-Loop Voltage Gain(3)	—	90	—	db	
CM34	VICM	Input Common-Mode Voltage	AVSS	—	AVDD	V	
Op Amp AC Characteristics							
CM20	SR	Slew Rate(3)	—	9	—	V/µs	10 pF load
CM21a	PM	Phase Margin (Configuration A)(3,4)	—	55	—	Degree	G = 100V/V; 10 pF load
CM21b	PM	Phase Margin (Configuration B)(3,5)	—	40	—	Degree	G = 100V/V; 10 pF load
CM22	GM	Gain Margin(3)	—	20	—	db	G = 100V/V; 10 pF load
CM23a	GBW	Gain Bandwidth (Configuration A)(3,4)	—	10	—	MHz	10 pF load
CM23b	GBW	Gain Bandwidth (Configuration B)(3,5)	—	6	—	MHz	10 pF load

Note 1: Device is functional at VBORMIN < VDD < VDDMIN, but will have degraded performance. Device functionality is tested, but not characterized. Analog modules (ADC, op amp/comparator and comparator voltage reference) may have degraded performance. Refer to Parameter BO10 in Table 30-13 for the minimum and maximum BOR values.

2: Data in "Typ" column is at 3.3V, +25°C unless otherwise stated.

3: Parameter is characterized but not tested in manufacturing.

4: See Figure 25-6 for configuration information.

5: See Figure 25-7 for configuration information.

6: Resistances can vary by ±10% between op amps.