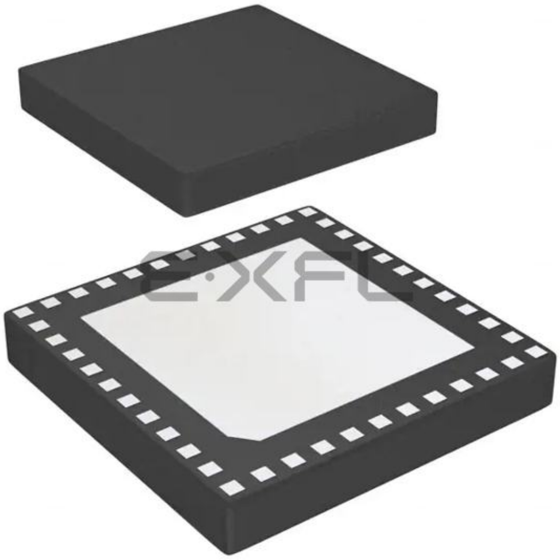

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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	PIC
Core Size	16-Bit
Speed	70 MIPs
Connectivity	I²C, IrDA, LINbus, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, DMA, POR, PWM, WDT
Number of I/O	35
Program Memory Size	256KB (85.5K x 24)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	16K x 16
Voltage - Supply (Vcc/Vdd)	3V ~ 3.6V
Data Converters	A/D 9x10b/12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	44-VFTLA Exposed Pad
Supplier Device Package	44-VTLA (6x6)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/pic24ep256gp204-i-tl

dsPIC33EPXXXGP50X, dsPIC33EPXXXMC20X/50X AND PIC24EPXXXGP/MC20X PRODUCT FAMILIES

The device names, pin counts, memory sizes and peripheral availability of each device are listed in Table 1 (General Purpose Families) and Table 2 (Motor Control Families). Their pinout diagrams appear on the following pages.

TABLE 1: dsPIC33EPXXXGP50X and PIC24EPXXXGP20X GENERAL PURPOSE FAMILIES

Device	Page Erase Size (Instructions)	Program Flash Memory (Kbytes)	RAM (Kbyte)	Remappable Peripherals							I^2C™	CRC Generator	10-Bit/12-Bit ADC (Channels)	Op Amps/Comparators	CTMU	PTG	I/O Pins	Pins	Packages
				16-Bit/32-Bit Timers	Input Capture	Output Compare	UART	SPI(2)	ECAN™ Technology	External Interrupts(3)									
PIC24EP32GP202	512	32	4	5	4	4	2	2	—	3	2	1	6	2/3(1)	Yes	Yes	21	28	SPDIP, SOIC, SSOP(4), QFN-S
PIC24EP64GP202	1024	64	8																
PIC24EP128GP202	1024	128	16																
PIC24EP256GP202	1024	256	32																
PIC24EP512GP202	1024	512	48																
PIC24EP32GP203	512	32	4	5	4	4	2	2	—	3	2	1	8	3/4	Yes	Yes	25	36	VTLA
PIC24EP64GP203	1024	64	8																
PIC24EP32GP204	512	32	4	5	4	4	2	2	—	3	2	1	9	3/4	Yes	Yes	35	44/48	VTLA(4), TQFP, QFN, UQFN
PIC24EP64GP204	1024	64	8																
PIC24EP128GP204	1024	128	16																
PIC24EP256GP204	1024	256	32																
PIC24EP512GP204	1024	512	48																
PIC24EP64GP206	1024	64	8	5	4	4	2	2	—	3	2	1	16	3/4	Yes	Yes	53	64	TQFP, QFN
PIC24EP128GP206	1024	128	16																
PIC24EP256GP206	1024	256	32																
PIC24EP512GP206	1024	512	48																
dsPIC33EP32GP502	512	32	4	5	4	4	2	2	1	3	2	1	6	2/3(1)	Yes	Yes	21	28	SPDIP, SOIC, SSOP(4), QFN-S
dsPIC33EP64GP502	1024	64	8																
dsPIC33EP128GP502	1024	128	16																
dsPIC33EP256GP502	1024	256	32																
dsPIC33EP512GP502	1024	512	48																
dsPIC33EP32GP503	512	32	4	5	4	4	2	2	1	3	2	1	8	3/4	Yes	Yes	25	36	VTLA
dsPIC33EP64GP503	1024	64	8																
dsPIC33EP32GP504	512	32	4	5	4	4	2	2	1	3	2	1	9	3/4	Yes	Yes	35	44/48	VTLA(4), TQFP, QFN, UQFN
dsPIC33EP64GP504	1024	64	8																
dsPIC33EP128GP504	1024	128	16																
dsPIC33EP256GP504	1024	256	32																
dsPIC33EP512GP504	1024	512	48																
dsPIC33EP64GP506	1024	64	8	5	4	4	2	2	1	3	2	1	16	3/4	Yes	Yes	53	64	TQFP, QFN
dsPIC33EP128GP506	1024	128	16																
dsPIC33EP256GP506	1024	256	32																
dsPIC33EP512GP506	1024	512	48																

Note 1: On 28-pin devices, Comparator 4 does not have external connections. Refer to **Section 25.0 “Op Amp/Comparator Module”** for details.
2: Only SPI2 is remappable.
3: INT0 is not remappable.
4: The SSOP and VTLA packages are not available for devices with 512 Kbytes of memory.

4.2 Data Address Space

The dsPIC33EPXXXGP50X, dsPIC33EPXXXMC20X/50X and PIC24EPXXXGP/MC20X CPU has a separate 16-bit-wide data memory space. The Data Space is accessed using separate Address Generation Units (AGUs) for read and write operations. The data memory maps, which are presented by device family and memory size, are shown in Figure 4-7 through Figure 4-16.

All Effective Addresses (EAs) in the data memory space are 16 bits wide and point to bytes within the Data Space. This arrangement gives a base Data Space address range of 64 Kbytes (32K words).

The base Data Space address is used in conjunction with a Read or Write Page register (DSRPAG or DSWPAG) to form an Extended Data Space, which has a total address range of 16 Mbytes.

dsPIC33EPXXXGP50X, dsPIC33EPXXXMC20X/50X and PIC24EPXXXGP/MC20X devices implement up to 52 Kbytes of data memory (4 Kbytes of data memory for Special Function Registers and up to 48 Kbytes of data memory for RAM). If an EA points to a location outside of this area, an all-zero word or byte is returned.

4.2.1 DATA SPACE WIDTH

The data memory space is organized in byte-addressable, 16-bit-wide blocks. Data is aligned in data memory and registers as 16-bit words, but all Data Space EAs resolve to bytes. The Least Significant Bytes (LSBs) of each word have even addresses, while the Most Significant Bytes (MSBs) have odd addresses.

4.2.2 DATA MEMORY ORGANIZATION AND ALIGNMENT

To maintain backward compatibility with PIC® MCU devices and improve Data Space memory usage efficiency, the dsPIC33EPXXXGP50X, dsPIC33EPXXXMC20X/50X and PIC24EPXXXGP/MC20X instruction set supports both word and byte operations. As a consequence of byte accessibility, all Effective Address calculations are internally scaled to step through word-aligned memory. For example, the core recognizes that Post-Modified Register Indirect Addressing mode [Ws++] results in a value of Ws + 1 for byte operations and Ws + 2 for word operations.

A data byte read, reads the complete word that contains the byte, using the LSb of any EA to determine which byte to select. The selected byte is placed onto the LSB of the data path. That is, data memory and registers are organized as two parallel, byte-wide entities with shared (word) address decode but separate write lines. Data byte writes only write to the corresponding side of the array or register that matches the byte address.

All word accesses must be aligned to an even address. Misaligned word data fetches are not supported, so care must be taken when mixing byte and word operations, or translating from 8-bit MCU code. If a misaligned read or write is attempted, an address error trap is generated. If the error occurred on a read, the instruction underway is completed. If the error occurred on a write, the instruction is executed but the write does not occur. In either case, a trap is then executed, allowing the system and/or user application to examine the machine state prior to execution of the address Fault.

All byte loads into any W register are loaded into the LSB. The MSB is not modified.

A Sign-Extend (`SE`) instruction is provided to allow user applications to translate 8-bit signed data to 16-bit signed values. Alternatively, for 16-bit unsigned data, user applications can clear the MSB of any W register by executing a Zero-Extend (`ZE`) instruction on the appropriate address.

4.2.3 SFR SPACE

The first 4 Kbytes of the Near Data Space, from 0x0000 to 0x0FFF, is primarily occupied by Special Function Registers (SFRs). These are used by the dsPIC33EPXXXGP50X, dsPIC33EPXXXMC20X/50X and PIC24EPXXXGP/MC20X core and peripheral modules for controlling the operation of the device.

SFRs are distributed among the modules that they control and are generally grouped together by module. Much of the SFR space contains unused addresses; these are read as '`0`'.

Note:	The actual set of peripheral features and interrupts varies by the device. Refer to the corresponding device tables and pinout diagrams for device-specific information.

4.2.4 NEAR DATA SPACE

The 8-Kbyte area, between 0x0000 and 0x1FFF, is referred to as the Near Data Space. Locations in this space are directly addressable through a 13-bit absolute address field within all memory direct instructions. Additionally, the whole Data Space is addressable using `MOV` instructions, which support Memory Direct Addressing mode with a 16-bit address field, or by using Indirect Addressing mode using a working register as an Address Pointer.

4.5 Instruction Addressing Modes

The addressing modes shown in Table 4-63 form the basis of the addressing modes optimized to support the specific features of individual instructions. The addressing modes provided in the `MAC` class of instructions differ from those in the other instruction types.

4.5.1 FILE REGISTER INSTRUCTIONS

Most file register instructions use a 13-bit address field (f) to directly address data present in the first 8192 bytes of data memory (Near Data Space). Most file register instructions employ a working register, W0, which is denoted as WREG in these instructions. The destination is typically either the same file register or WREG (with the exception of the `MUL` instruction), which writes the result to a register or register pair. The `MOV` instruction allows additional flexibility and can access the entire Data Space.

4.5.2 MCU INSTRUCTIONS

The three-operand MCU instructions are of the form:

`Operand 3 = Operand 1 <function> Operand 2`

where Operand 1 is always a working register (that is, the addressing mode can only be Register Direct), which is referred to as Wb. Operand 2 can be a W register fetched from data memory or a 5-bit literal. The result location can either be a W register or a data memory location. The following addressing modes are supported by MCU instructions:

- Register Direct
- Register Indirect
- Register Indirect Post-Modified
- Register Indirect Pre-Modified
- 5-Bit or 10-Bit Literal

Note: Not all instructions support all the addressing modes given above. Individual instructions can support different subsets of these addressing modes.

TABLE 4-63: FUNDAMENTAL ADDRESSING MODES SUPPORTED

Addressing Mode	Description
File Register Direct	The address of the file register is specified explicitly.
Register Direct	The contents of a register are accessed directly.
Register Indirect	The contents of Wn form the Effective Address (EA).
Register Indirect Post-Modified	The contents of Wn form the EA. Wn is post-modified (incremented or decremented) by a constant value.
Register Indirect Pre-Modified	Wn is pre-modified (incremented or decremented) by a signed constant value to form the EA.
Register Indirect with Register Offset (Register Indexed)	The sum of Wn and Wb forms the EA.
Register Indirect with Literal Offset	The sum of Wn and a literal forms the EA.

REGISTER 7-1: SR: CPU STATUS REGISTER(1)

R/W-0	R/W-0	R/W-0	R/W-0	R/C-0	R/C-0	R-0	R/W-0
OA	OB	SA	SB	OAB	SAB	DA	DC
bit 15							bit 8

R/W-0(3)	R/W-0(3)	R/W-0(3)	R-0	R/W-0	R/W-0	R/W-0	R/W-0
IPL<2:0>(2)			RA	N	OV	Z	C
bit 7							bit 0

Legend:	C = Clearable bit		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’= Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 7-5 **IPL<2:0>:** CPU Interrupt Priority Level Status bits(2,3)

`111` = CPU Interrupt Priority Level is 7 (15); user interrupts are disabled
`110` = CPU Interrupt Priority Level is 6 (14)
`101` = CPU Interrupt Priority Level is 5 (13)
`100` = CPU Interrupt Priority Level is 4 (12)
`011` = CPU Interrupt Priority Level is 3 (11)
`010` = CPU Interrupt Priority Level is 2 (10)
`001` = CPU Interrupt Priority Level is 1 (9)
`000` = CPU Interrupt Priority Level is 0 (8)

Note 1: For complete register details, see Register 3-1.

2: The IPL<2:0> bits are concatenated with the IPL<3> bit (CORCON<3>) to form the CPU Interrupt Priority Level. The value in parentheses indicates the IPL, if IPL<3> = `1`. User interrupts are disabled when IPL<3> = `1`.

3: The IPL<2:0> Status bits are read-only when the NSTDIS bit (INTCON1<15>) = `1`.

9.1 CPU Clocking System

The dsPIC33EPXXXGP50X, dsPIC33EPXXXMC20X/50X and PIC24EPXXXGP/MC20X family of devices provides six system clock options:

- Fast RC (FRC) Oscillator
- FRC Oscillator with Phase Locked Loop (PLL)
- FRC Oscillator with Postscaler
- Primary (XT, HS or EC) Oscillator
- Primary Oscillator with PLL
- Low-Power RC (LPRC) Oscillator

Instruction execution speed or device operating frequency, FCY, is given by Equation 9-1.

EQUATION 9-1: DEVICE OPERATING FREQUENCY

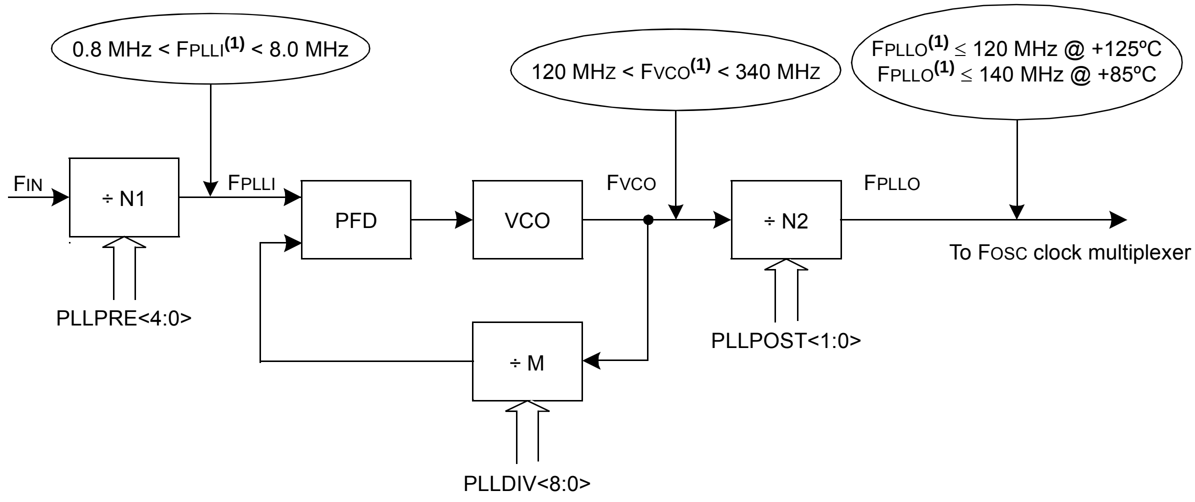
$$F_{CY} = F_{OSC}/2$$

Figure 9-2 is a block diagram of the PLL module.

Equation 9-2 provides the relationship between input frequency (FIN) and output frequency (FPLLO). In clock modes S1 and S3, when the PLL output is selected, FOSC = FPLLO.

Equation 9-3 provides the relationship between input frequency (FIN) and VCO frequency (FVCO).

FIGURE 9-2: PLL BLOCK DIAGRAM



Note 1: This frequency range must be met at all times.

EQUATION 9-2: FPLLO CALCULATION

$$F_{PLLO} = F_{IN} \times \left(\frac{M}{N1 \times N2}\right) = F_{IN} \times \left(\frac{(PLLDIV + 2)}{(PLLPRE + 2) \times 2(PLLPOST + 1)}\right)$$

Where:

$N1 = PLLPRE + 2$

$N2 = 2 \times (PLLPOST + 1)$

$M = PLLDIV + 2$

EQUATION 9-3: FVCO CALCULATION

$$F_{VCO} = F_{IN} \times \left(\frac{M}{N1}\right) = F_{IN} \times \left(\frac{(PLLDIV + 2)}{(PLLPRE + 2)}\right)$$

REGISTER 9-2: CLKDIV: CLOCK DIVISOR REGISTER (CONTINUED)

bit 4-0	**PLLPRE<4:0>:** PLL Phase Detector Input Divider Select bits (also denoted as ‘N1’, PLL prescaler) `11111` = Input divided by 33 • • • `00001` = Input divided by 3 `00000` = Input divided by 2 (default)

Note 1: The DOZE<2:0> bits can only be written to when the DOZEN bit is clear. If DOZEN = `1`, any writes to DOZE<2:0> are ignored.

2: This bit is cleared when the ROI bit is set and an interrupt occurs.

3: The DOZEN bit cannot be set if DOZE<2:0> = `000`. If DOZE<2:0> = `000`, any attempt by user software to set the DOZEN bit is ignored.

REGISTER 11-15: RPINR37: PERIPHERAL PIN SELECT INPUT REGISTER 37 (dsPIC33EPXXXMC20X/50X AND PIC24EPXXXMC20X DEVICES ONLY)

U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
—	SYNCI1R<6:0>						
bit 15							bit 8

U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
—	—	—	—	—	—	—	—
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 15	**Unimplemented:** Read as ‘`0`’
bit 14-8	**SYNCI1R<6:0>:** Assign PWM Synchronization Input 1 to the Corresponding RPn Pin bits (see Table 11-2 for input pin selection numbers) `1111001` = Input tied to RPI121 . . . `0000001` = Input tied to CMP1 `0000000` = Input tied to VSS
bit 7-0	**Unimplemented:** Read as ‘`0`’

REGISTER 17-2: QEI1IOC: QEI1 I/O CONTROL REGISTER (CONTINUED)

bit 2	**INDEX:** Status of INDXx Input Pin After Polarity Control `1` = Pin is at logic ‘`1`’ `0` = Pin is at logic ‘`0`’
bit 1	**QEB:** Status of QEBx Input Pin After Polarity Control And SWPAB Pin Swapping `1` = Pin is at logic ‘`1`’ `0` = Pin is at logic ‘`0`’
bit 0	**QEA:** Status of QEAx Input Pin After Polarity Control And SWPAB Pin Swapping `1` = Pin is at logic ‘`1`’ `0` = Pin is at logic ‘`0`’

REGISTER 17-3: QEI1STAT: QEI1 STATUS REGISTER (CONTINUED)

bit 2	**HOMIEN:** Home Input Event Interrupt Enable bit `1` = Interrupt is enabled `0` = Interrupt is disabled
bit 1	**IDXIRQ:** Status Flag for Index Event Status bit `1` = Index event has occurred `0` = No Index event has occurred
bit 0	**IDXIEN:** Index Input Event Interrupt Enable bit `1` = Interrupt is enabled `0` = Interrupt is disabled

Note 1: This status bit is only applicable to PIMOD<2:0> modes, ‘`011`’ and ‘`100`’.

REGISTER 23-3: AD1CON3: ADC1 CONTROL REGISTER 3

R/W-0	U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
ADRC	—	—	SAMC4(1)	SAMC3(1)	SAMC2(1)	SAMC1(1)	SAMC0(1)
bit 15							bit 8

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
ADCS7(2)	ADCS6(2)	ADCS5(2)	ADCS4(2)	ADCS3(2)	ADCS2(2)	ADCS1(2)	ADCS0(2)
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 15 **ADRC:** ADC1 Conversion Clock Source bit

`1` = ADC internal RC clock
`0` = Clock derived from system clock

bit 14-13 **Unimplemented:** Read as ‘`0`’

bit 12-8 **SAMC<4:0>:** Auto-Sample Time bits(1)

`11111` = 31 T_{AD}
•
•
•
`00001` = 1 T_{AD}
`00000` = 0 T_{AD}

bit 7-0 **ADCS<7:0>:** ADC1 Conversion Clock Select bits(2)

`11111111` = T_P • (ADCS<7:0> + 1) = T_P •256 = T_{AD}
•
•
•
`00000010` = T_P • (ADCS<7:0> + 1) = T_P •3 = T_{AD}
`00000001` = T_P • (ADCS<7:0> + 1) = T_P •2 = T_{AD}
`00000000` = T_P • (ADCS<7:0> + 1) = T_P •1 = T_{AD}

Note 1: This bit is only used if SSRC<2:0> (AD1CON1<7:5>) = `111` and SSRCG (AD1CON1<4>) = `0`.
2: This bit is not used if ADRC (AD1CON3<15>) = `1`.

REGISTER 23-7: AD1CSSH: ADC1 INPUT SCAN SELECT REGISTER HIGH(1)

R/W-0	R/W-0	U-0	U-0	U-0	R/W-0	R/W-0	R/W-0
CSS31	CSS30	—	—	—	CSS26(2)	CSS25(2)	CSS24(2)
bit 15							bit 8

U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
—	—	—	—	—	—	—	—
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 15 **CSS31:** ADC1 Input Scan Selection bit

`1` = Selects CTMU capacitive and time measurement for input scan (Open)
`0` = Skips CTMU capacitive and time measurement for input scan (Open)

bit 14 **CSS30:** ADC1 Input Scan Selection bit

`1` = Selects CTMU on-chip temperature measurement for input scan (CTMU TEMP)
`0` = Skips CTMU on-chip temperature measurement for input scan (CTMU TEMP)

bit 13-11 **Unimplemented:** Read as ‘`0`’

bit 10 **CSS26:** ADC1 Input Scan Selection bit(2)

`1` = Selects OA3/AN6 for input scan
`0` = Skips OA3/AN6 for input scan

bit 9 **CSS25:** ADC1 Input Scan Selection bit(2)

`1` = Selects OA2/AN0 for input scan
`0` = Skips OA2/AN0 for input scan

bit 8 **CSS24:** ADC1 Input Scan Selection bit(2)

`1` = Selects OA1/AN3 for input scan
`0` = Skips OA1/AN3 for input scan

bit 7-0 **Unimplemented:** Read as ‘`0`’

Note 1: All AD1CSSH bits can be selected by user software. However, inputs selected for scan, without a corresponding input on the device, convert VREFL.

2: The OAx input is used if the corresponding op amp is selected (OPMODE (CMxCON<10>) = `1`); otherwise, the ANx input is used.

TABLE 30-11: DC CHARACTERISTICS: I/O PIN INPUT SPECIFICATIONS

DC CHARACTERISTICS			**Standard Operating Conditions: 3.0V to 3.6V (unless otherwise stated)** Operating temperature -40°C ≤ TA ≤ +85°C for Industrial -40°C ≤ TA ≤ +125°C for Extended				
Param No.	**Symbol**	**Characteristic**	**Min.**	**Typ.**	**Max.**	**Units**	**Conditions**
	VIL	**Input Low Voltage**					
DI10		Any I/O Pin and $\overline{\text{MCLR}}$	VSS	—	0.2 VDD	V	
DI18		I/O Pins with SDAx, SCLx	VSS	—	0.3 VDD	V	SMBus disabled
DI19		I/O Pins with SDAx, SCLx	VSS	—	0.8	V	SMBus enabled
	VIH	**Input High Voltage**					
DI20		I/O Pins Not 5V Tolerant	0.8 VDD	—	VDD	V	**(Note 3)**
		I/O Pins 5V Tolerant and $\overline{\text{MCLR}}$	0.8 VDD	—	5.5	V	**(Note 3)**
		I/O Pins with SDAx, SCLx	0.8 VDD	—	5.5	V	SMBus disabled
		I/O Pins with SDAx, SCLx	2.1	—	5.5	V	SMBus enabled
	ICNPU	**Change Notification Pull-up Current**					
DI30			150	250	550	µA	VDD = 3.3V, VPIN = VSS
	ICNPD	**Change Notification Pull-Down Current(4)**					
DI31			20	50	100	µA	VDD = 3.3V, VPIN = VDD

Note 1: The leakage current on the $\overline{\text{MCLR}}$ pin is strongly dependent on the applied voltage level. The specified levels represent normal operating conditions. Higher leakage current can be measured at different input voltages.

2: Negative current is defined as current sourced by the pin.

3: See the **“Pin Diagrams”** section for the 5V tolerant I/O pins.

4: VIL source < (VSS – 0.3). Characterized but not tested.

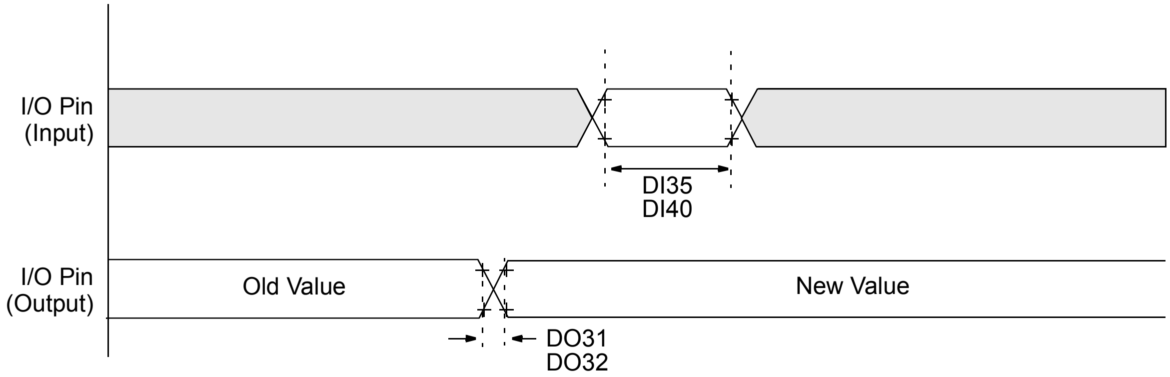
5: Non-5V tolerant pins VIH source > (VDD + 0.3), 5V tolerant pins VIH source > 5.5V. Characterized but not tested.

6: Digital 5V tolerant pins cannot tolerate any “positive” input injection current from input sources > 5.5V.

7: Non-zero injection currents can affect the ADC results by approximately 4-6 counts.

8: Any number and/or combination of I/O pins not excluded under IICL or IICH conditions are permitted provided the mathematical “absolute instantaneous” sum of the input injection currents from all pins do not exceed the specified limit. Characterized but not tested.

FIGURE 30-3: I/O TIMING CHARACTERISTICS



Note: Refer to Figure 30-1 for load conditions.

TABLE 30-21: I/O TIMING REQUIREMENTS

AC CHARACTERISTICS			**Standard Operating Conditions: 3.0V to 3.6V (unless otherwise stated)** Operating temperature -40°C ≤ TA ≤ +85°C for Industrial -40°C ≤ TA ≤ +125°C for Extended				
Param No.	**Symbol**	**Characteristic**	**Min.**	**Typ.(1)**	**Max.**	**Units**	**Conditions**
DO31	TIOR	Port Output Rise Time	—	5	10	ns	
DO32	TIOF	Port Output Fall Time	—	5	10	ns	
DI35	TINP	INTx Pin High or Low Time (input)	20	—	—	ns	
DI40	TRBP	CNx High or Low Time (input)	2	—	—	TCY	

Note 1: Data in “Typical” column is at 3.3V, +25°C unless otherwise stated.

FIGURE 30-4: BOR AND MASTER CLEAR RESET TIMING CHARACTERISTICS

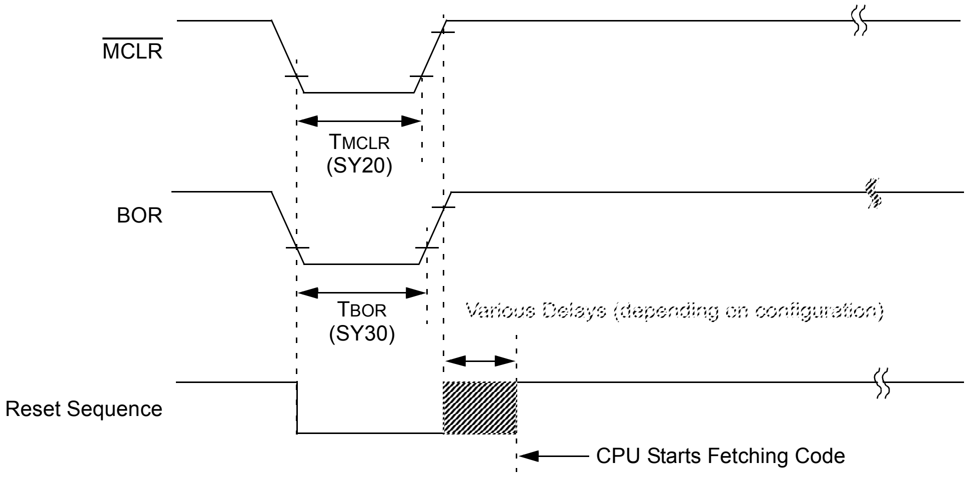
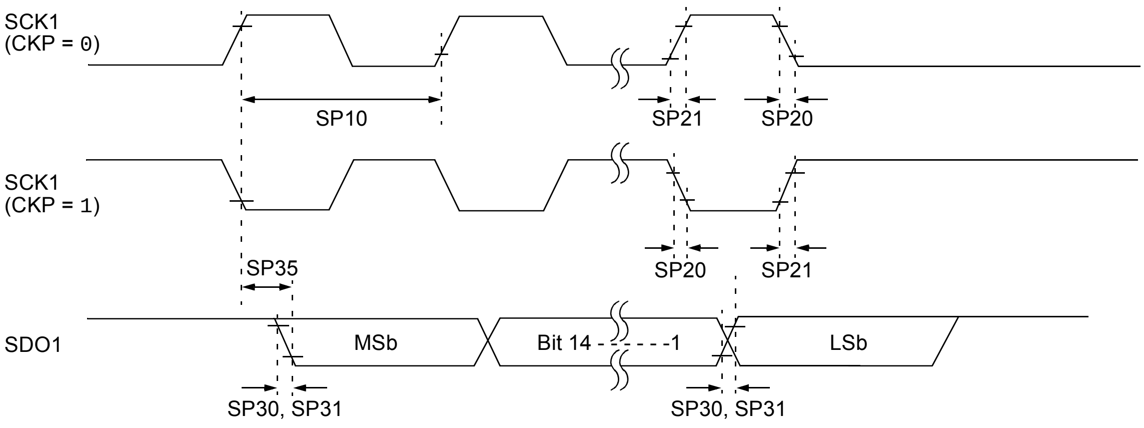


TABLE 30-41: SPI1 MAXIMUM DATA/CLOCK RATE SUMMARY

AC CHARACTERISTICS			**Standard Operating Conditions: 3.0V to 3.6V (unless otherwise stated)** Operating temperature -40°C ≤ TA ≤ +85°C for Industrial -40°C ≤ TA ≤ +125°C for Extended			
Maximum Data Rate	**Master Transmit Only (Half-Duplex)**	**Master Transmit/Receive (Full-Duplex)**	**Slave Transmit/Receive (Full-Duplex)**	**CKE**	**CKP**	**SMP**
15 MHz	Table 30-42	—	—	0,1	0,1	0,1
10 MHz	—	Table 30-43	—	1	0,1	1
10 MHz	—	Table 30-44	—	0	0,1	1
15 MHz	—	—	Table 30-45	1	0	0
11 MHz	—	—	Table 30-46	1	1	0
15 MHz	—	—	Table 30-47	0	1	0
11 MHz	—	—	Table 30-48	0	0	0

FIGURE 30-22: SPI1 MASTER MODE (HALF-DUPLEX, TRANSMIT ONLY, CKE = 0) TIMING CHARACTERISTICS



Note: Refer to Figure 30-1 for load conditions.

TABLE 30-47: SPI1 SLAVE MODE (FULL-DUPLEX, CKE = `0`, CKP = `1`, SMP = `0`) TIMING REQUIREMENTS

AC CHARACTERISTICS			**Standard Operating Conditions: 3.0V to 3.6V (unless otherwise stated)** Operating temperature -40°C ≤ T_A ≤ +85°C for Industrial -40°C ≤ T_A ≤ +125°C for Extended				
Param.	**Symbol**	**Characteristic[1]**	**Min.**	**Typ.[2]**	**Max.**	**Units**	**Conditions**
SP70	FscP	Maximum SCK1 Input Frequency	—	—	15	MHz	**(Note 3)**
SP72	TscF	SCK1 Input Fall Time	—	—	—	ns	See Parameter DO32 **(Note 4)**
SP73	TscR	SCK1 Input Rise Time	—	—	—	ns	See Parameter DO31 **(Note 4)**
SP30	TdoF	SDO1 Data Output Fall Time	—	—	—	ns	See Parameter DO32 **(Note 4)**
SP31	TdoR	SDO1 Data Output Rise Time	—	—	—	ns	See Parameter DO31 **(Note 4)**
SP35	TscH2doV, TscL2doV	SDO1 Data Output Valid after SCK1 Edge	—	6	20	ns	
SP36	TdoV2scH, TdoV2scL	SDO1 Data Output Setup to First SCK1 Edge	30	—	—	ns	
SP40	TdiV2scH, TdiV2scL	Setup Time of SDI1 Data Input to SCK1 Edge	30	—	—	ns	
SP41	TscH2diL, TscL2diL	Hold Time of SDI1 Data Input to SCK1 Edge	30	—	—	ns	
SP50	TssL2scH, TssL2scL	$\overline{\text{SS1}}$ ↓ to SCK1 ↑ or SCK1 ↓ Input	120	—	—	ns	
SP51	TssH2doZ	$\overline{\text{SS1}}$ ↑ to SDO1 Output High-Impedance	10	—	50	ns	**(Note 4)**
SP52	TscH2ssH, TscL2ssH	$\overline{\text{SS1}}$ ↑ after SCK1 Edge	1.5 T_{CY} + 40	—	—	ns	**(Note 4)**

Note 1: These parameters are characterized, but are not tested in manufacturing.

2: Data in “Typical” column is at 3.3V, +25°C unless otherwise stated.

3: The minimum clock period for SCK1 is 66.7 ns. Therefore, the SCK1 clock generated by the master must not violate this specification.

4: Assumes 50 pF load on all SPI1 pins.

32.0 DC AND AC DEVICE CHARACTERISTICS GRAPHS

Note: The graphs provided following this note are a statistical summary based on a limited number of samples and are provided for design guidance purposes only. The performance characteristics listed herein are not tested or guaranteed. In some graphs, the data presented may be outside the specified operating range (e.g., outside specified power supply range) and therefore, outside the warranted range.

FIGURE 32-1: VOH – 4x DRIVER PINS

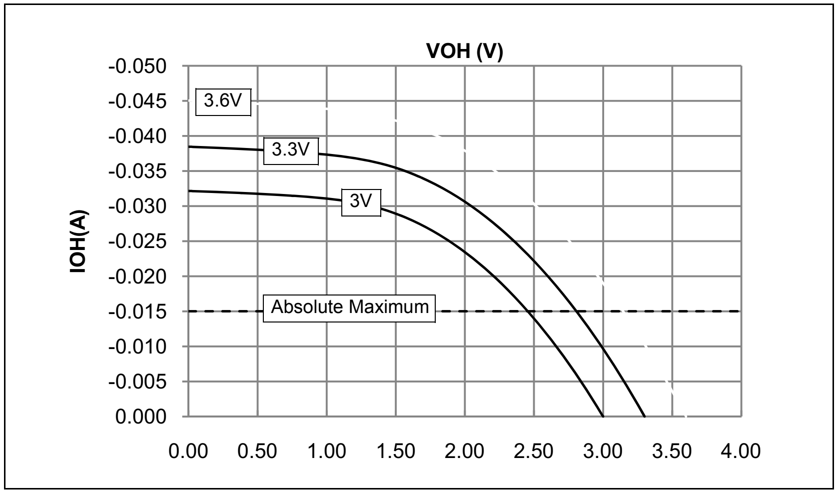


FIGURE 32-2: VOH – 8x DRIVER PINS

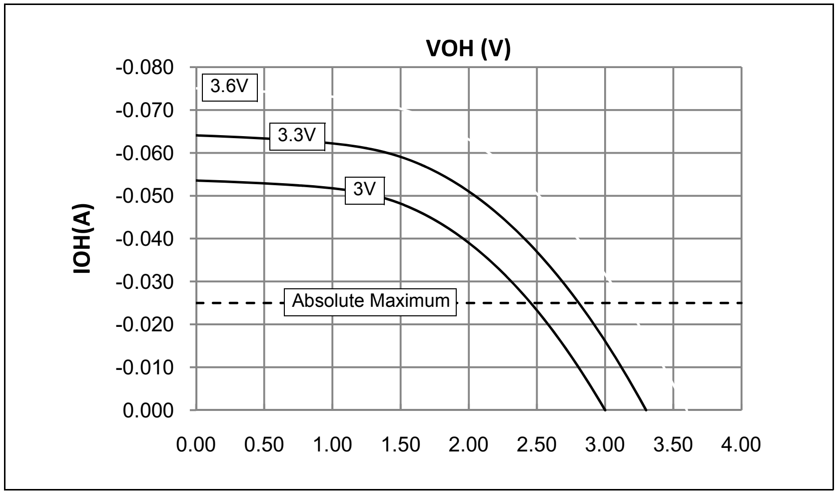


FIGURE 32-3: VOL – 4x DRIVER PINS

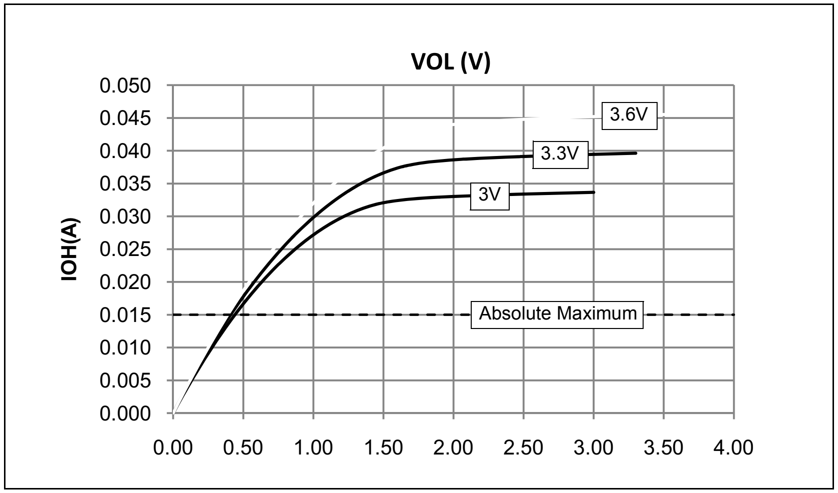
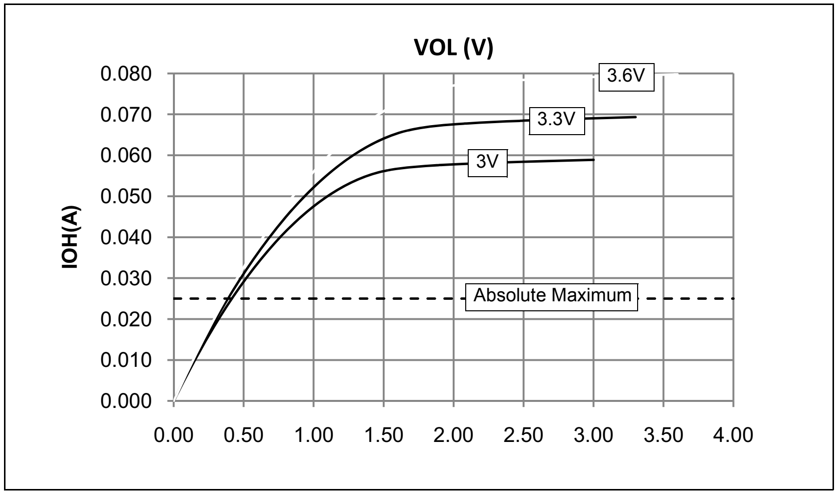


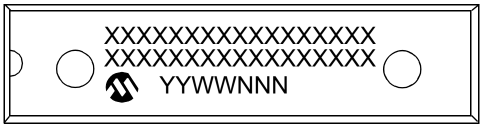
FIGURE 32-4: VOL – 8x DRIVER PINS



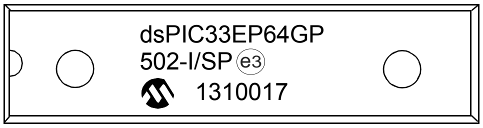
33.0 PACKAGING INFORMATION

33.1 Package Marking Information

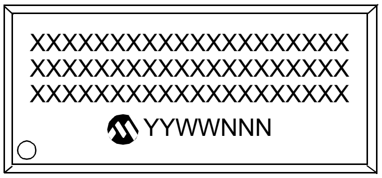
28-Lead SPDIP



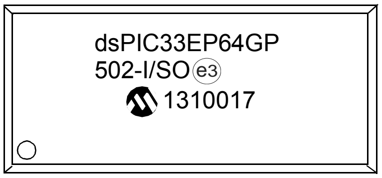
Example



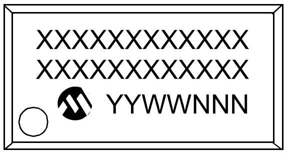
28-Lead SOIC (.300”)



Example

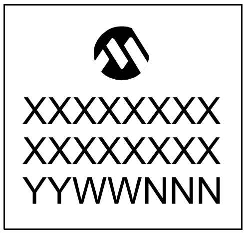


28-Lead SSOP



Example

28-Lead QFN-S (6x6x0.9 mm)



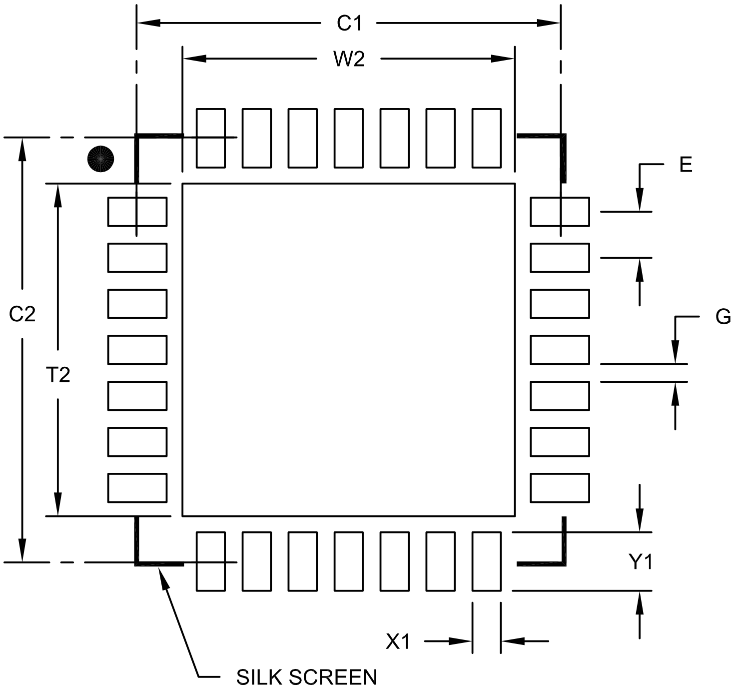
Example

Legend:	XX...X	Customer-specific information
	Y	Year code (last digit of calendar year)
	YY	Year code (last 2 digits of calendar year)
	WW	Week code (week of January 1 is week ‘01’)
	NNN	Alphanumeric traceability code
	e3	Pb-free JEDEC designator for Matte Tin (Sn)
	*	This package is Pb-free. The Pb-free JEDEC designator (e3) can be found on the outer packaging for this package.

Note: In the event the full Microchip part number cannot be marked on one line, it will be carried over to the next line, thus limiting the number of available characters for customer-specific information.

28-Lead Plastic Quad Flat, No Lead Package (MM) – 6x6x0.9 mm Body [QFN-S] with 0.40 mm Contact Length

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



RECOMMENDED LAND PATTERN

Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Contact Pitch	E	0.65 BSC		
Optional Center Pad Width	W2			4.70
Optional Center Pad Length	T2			4.70
Contact Pad Spacing	C1		6.00	
Contact Pad Spacing	C2		6.00	
Contact Pad Width (X28)	X1			0.40
Contact Pad Length (X28)	Y1			0.85
Distance Between Pads	G	0.25		

Notes:

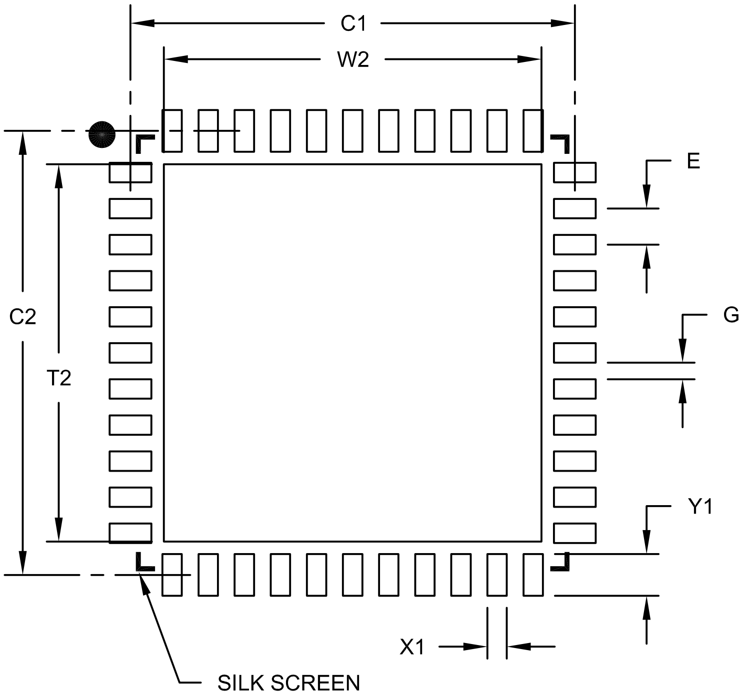
1. Dimensioning and tolerancing per ASME Y14.5M

BSC: Basic Dimension. Theoretically exact value shown without tolerances.

Microchip Technology Drawing No. C04-2124A

44-Lead Plastic Quad Flat, No Lead Package (ML) - 8x8 mm Body [QFN]

Note:	For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



RECOMMENDED LAND PATTERN

Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Contact Pitch	E	0.65 BSC		
Optional Center Pad Width	W2			6.60
Optional Center Pad Length	T2			6.60
Contact Pad Spacing	C1		8.00	
Contact Pad Spacing	C2		8.00	
Contact Pad Width (X44)	X1			0.35
Contact Pad Length (X44)	Y1			0.85
Distance Between Pads	G	0.25		

Notes:

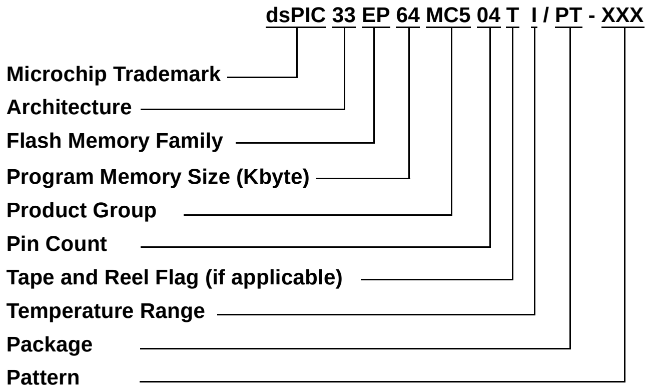
1. Dimensioning and tolerancing per ASME Y14.5M

BSC: Basic Dimension. Theoretically exact value shown without tolerances.

Microchip Technology Drawing No. C04-2103B

PRODUCT IDENTIFICATION SYSTEM

To order or obtain information, e.g., on pricing or delivery, refer to the factory or the listed sales office.



Examples:

dsPIC33EP64MC504-I/PT:
dsPIC33, Enhanced Performance,
64-Kbyte Program Memory,
Motor Control, 44-Pin,
Industrial Temperature,
TQFP package.

Architecture:	33	=	16-bit Digital Signal Controller
	24	=	16-bit Microcontroller
Flash Memory Family:	EP	=	Enhanced Performance
Product Group:	GP	=	General Purpose family
	MC	=	Motor Control family
Pin Count:	02	=	28-pin
	03	=	36-pin
	04	=	44-pin
	06	=	64-pin
Temperature Range:	I	=	-40°C to+85°C (Industrial)
	E	=	-40°C to+125°C (Extended)
Package:	ML	=	Plastic Quad, No Lead Package - (44-pin) 8x8 mm body (QFN)
	MM	=	Plastic Quad, No Lead Package - (28-pin) 6x6 mm body (QFN-S)
	MR	=	Plastic Quad, No Lead Package - (64-pin) 9x9 mm body (QFN)
	MV	=	Thin Quad, No Lead Package - (48-pin) 6x6 mm body (UQFN)
	PT	=	Plastic Thin Quad Flatpack - (44-pin) 10x10 mm body (TQFP)
	PT	=	Plastic Thin Quad Flatpack - (64-pin) 10x10 mm body (TQFP)
	SO	=	Plastic Small Outline, Wide - (28-pin) 7.50 mm body (SOIC)
	SP	=	Skinny Plastic Dual In-Line - (28-pin) 300 mil body (SPDIP)
	SS	=	Plastic Shrink Small Outline - (28-pin) 5.30 mm body (SSOP)
	TL	=	Very Thin Leadless Array - (36-pin) 5x5 mm body (VTLA)
	TL	=	Very Thin Leadless Array - (44-pin) 6x6 mm body (VTLA)