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"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "<u>Embedded -</u> <u>Microcontrollers</u>"

Details

E·XFI

Product Status	Obsolete
Core Processor	PIC
Core Size	16-Bit
Speed	60 MIPs
Connectivity	I ² C, IrDA, LINbus, QEI, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, DMA, Motor Control PWM, POR, PWM, WDT
Number of I/O	21
Program Memory Size	256КВ (85.5К х 24)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	16K x 16
Voltage - Supply (Vcc/Vdd)	3V ~ 3.6V
Data Converters	A/D 6x10b/12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 150°C (TA)
Mounting Type	Surface Mount
Package / Case	28-SOIC (0.295", 7.50mm Width)
Supplier Device Package	28-SOIC
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/pic24ep256mc202-h-so

Email: info@E-XFL.COM

Address: Room A, 16/F, Full Win Commercial Centre, 573 Nathan Road, Mongkok, Hong Kong



FIGURE 4-9: DATA MEMORY MAP FOR dsPIC33EP128MC20X/50X AND dsPIC33EP128GP50X DEVICES

				(,			
R/SO-0 ⁽¹	⁾ R/W-0 ⁽¹⁾	R/W-0 ⁽¹⁾	R/W-0	U-0	U-0	U-0	U-0
WR	WREN	WRERR	NVMSIDL ⁽²⁾			—	—
bit 15							bit 8
U-0	U-0	U-0	U-0	R/W-0 ⁽¹⁾	R/W-0 ⁽¹⁾	R/W-0 ⁽¹⁾	R/W-0 ⁽¹⁾
	—	—		NVMOP3 ^(3,4)	NVMOP2 ^(3,4)	NVMOP1 ^(3,4)	NVMOP0 ^(3,4)
bit 7							bit 0
						_	
Legend:		SO = Settab	le Only bit				
R = Reada	ble bit	W = Writable	e bit	U = Unimplem	ented bit, read	as '0'	
-n = Value	at POR	'1' = Bit is se	t	'0' = Bit is clea	ired	x = Bit is unkn	iown
bit 15	WR: Write Co 1 = Initiates a cleared by 0 = Program	ntrol bit ⁽¹⁾ a Flash memo y hardware o or erase oper	ory program or nce the operati ation is comple	erase operation on is complete ate and inactive	on; the operatio	n is self-timed	and the bit is
bit 14	WREN: Write 1 = Enables F 0 = Inhibits Fl	Enable bit ⁽¹⁾ ⁻ lash program ash program/	n/erase operati ⁄erase operatio	ons			
bit 13	WRERR: Writ 1 = An improp on any se 0 = The progr	e Sequence E per program of t attempt of th ram or erase	Error Flag bit ⁽¹⁾ rerase sequence e WR bit) operation comp	ce attempt or ter	mination has oc	curred (bit is se	t automatically
bit 12	NVMSIDL: N\ 1 = Flash volt 0 = Flash volt	/M Stop in Idl age regulator age regulator	e Control bit ⁽²⁾ goes into Star is active durin	ndby mode duri g Idle mode	ng Idle mode		
bit 11-4	Unimplement	ted: Read as	'0'	-			
bit 3-0 NVMOP<3:0>: NVM Operation Select bits ^(1,3,4) 1111 = Reserved 1100 = Reserved 1101 = Reserved 1010 = Reserved 1011 = Reserved 1010 = Reserved 1010 = Reserved 0011 = Memory page erase operation 0010 = Reserved 0011 = Memory double-word program operation ⁽⁵⁾ 0000 = Reserved							
Note 1: 2: 3: 4: 5:	These bits can only If this bit is set, the (TVREG) before Fla All other combination Execution of the PV Two adjacent word	/ be reset on a re will be mini sh memory be ons of NVMO wRSAV instruct s on a 4-word	a POR. mal power sav ecomes operat P<3:0> are uni tion is ignored I boundary are	rings (IIDLE) and ional. implemented. while any of the programmed d	d upon exiting lo e NVM operatio uring execution	the mode, there ns are in progra	is a delay ess. on.

REGISTER 5-1: NVMCON: NONVOLATILE MEMORY (NVM) CONTROL REGISTER

REGISTER 5-2: NV	MADRH: NONVOLATILE MEMORY ADDRESS REGISTER HIGH
------------------	---

U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
—	—	—	—	—	—	—	_
bit 15			•	•	•		bit 8
R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x
			NVMAD	R<23:16>			
bit 7							bit 0
Legend:							
R = Readable bit W = Writable bit		bit	U = Unimplemented bit, read as '0'				
-n = Value at POR '1' = Bit is set			'0' = Bit is cleared x = Bit is unknown			nown	
L							

bit 15-8 Unimplemented: Read as '0'

bit 7-0 **NVMADR<23:16>:** Nonvolatile Memory Write Address High bits Selects the upper 8 bits of the location to program or erase in program Flash memory. This register may be read or written by the user application.

REGISTER 5-3: NVMADRL: NONVOLATILE MEMORY ADDRESS REGISTER LOW

R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x
			NVMA	DR<15:8>			
bit 15							bit 8
R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x
			NVMA	DR<7:0>			
bit 7							bit 0
Legend:							
R = Readable bit W = Writable bit		oit	U = Unimplemented bit, read as '0'				
-n = Value at POR		'1' = Bit is set		'0' = Bit is cle	ared	x = Bit is unkr	nown

bit 15-0 NVMADR<15:0>: Nonvolatile Memory Write Address Low bits

Selects the lower 16 bits of the location to program or erase in program Flash memory. This register may be read or written by the user application.

REGISTER 5-4: NVMKEY: NONVOLATILE MEMORY KEY

U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
—	—	—	—	—	—	—	—
bit 15							bit 8
W-0	W-0	W-0	W-0	W-0	W-0	W-0	W-0
			NVMK	EY<7:0>			
bit 7							bit 0
Legend:							
R = Readable bit W = Writable bit		bit	U = Unimple	mented bit, rea	d as '0'		
-n = Value at POR '1' = Bit is set		٤	'0' = Bit is cle	eared	x = Bit is unk	nown	

bit 15-8 Unimplemented: Read as '0'

bit 7-0 **NVMKEY<7:0>:** Key Register (write-only) bits

R/W-0	R/W-0	R/W-0	R/W-0	R/C-0	R/C-0	R-0	R/W-0	
OA	OB	SA	SB	OAB	SAB	DA	DC	
bit 15							bit 8	
R/W-0 ⁽³⁾	R/W-0 ⁽³⁾	R/W-0 ⁽³⁾	R-0	R/W-0	R/W-0	R/W-0	R/W-0	
	IPL<2:0> ⁽²⁾		RA	Ν	OV	Z	С	
bit 7						-	bit 0	
								1

REGISTER 7-1: SR: CPU STATUS REGISTER⁽¹⁾

Legend:	C = Clearable bit		-
R = Readable bit	W = Writable bit	U = Unimplemented bit, read	l as '0'
-n = Value at POR	'1'= Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 7-5	IPL<2:0>: CPU Interrupt Priority Level Status bits ^(2,3)
	111 = CPU Interrupt Priority Level is 7 (15); user interrupts are disabled
	110 = CPU Interrupt Priority Level is 6 (14)
	101 = CPU Interrupt Priority Level is 5 (13)
	100 = CPU Interrupt Priority Level is 4 (12)
	011 = CPU Interrupt Priority Level is 3 (11)
	010 = CPU Interrupt Priority Level is 2 (10)
	001 = CPU Interrupt Priority Level is 1 (9)
	000 = CPU Interrupt Priority Level is 0 (8)

- **Note 1:** For complete register details, see Register 3-1.
 - 2: The IPL<2:0> bits are concatenated with the IPL<3> bit (CORCON<3>) to form the CPU Interrupt Priority Level. The value in parentheses indicates the IPL, if IPL<3> = 1. User interrupts are disabled when IPL<3> = 1.
 - **3:** The IPL<2:0> Status bits are read-only when the NSTDIS bit (INTCON1<15>) = 1.

R/W-0	U-0	R/W-0	R/W-0	R/W-0	R-0	R-0	R-0
VAR	—	US1	US0	EDT	DL2	DL1	DL0
bit 15							bit 8
R/W-0	R/W-0	R/W-1	R/W-0	R/C-0	R-0	R/W-0	R/W-0
SATA	SATB	SATDW	ACCSAT	IPL3 ⁽²⁾	SFA	RND	IF
bit 7							bit 0

REGISTER 7-2: CORCON: CORE CONTROL REGISTER⁽¹⁾

Legend:	C = Clearable bit		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read	1 as '0'
-n = Value at POR	'1'= Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit

bit 15	VAR: Variable Exception Processing Latency Control
	1 = Variable exception processing is enabled
	0 = Fixed exception processing is enabled
bit 3	IPL3: CPU Interrupt Priority Level Status bit 3 ⁽²⁾
	1 = CPU Interrupt Priority Level is greater than 7
	0 = CPU Interrupt Priority Level is 7 or less

Note 1: For complete register details, see Register 3-2.

2: The IPL3 bit is concatenated with the IPL<2:0> bits (SR<7:5>) to form the CPU Interrupt Priority Level.

REGISTER 8-9: DSADRH: DMA MOST RECENT RAM HIGH ADDRESS REGISTER

U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
—	_	—	—	_	—	—	—
bit 15							bit 8
R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0
			DSADR	<23:16>			
bit 7							bit 0
Legend:							
R = Readable I	bit	W = Writable bi	t	U = Unimpler	mented bit, read	as '0'	

R = Readable bit	W = Writable bit	U = Unimplemented bit, read	as '0'
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15-8 Unimplemented: Read as '0'

bit 7-0 DSADR<23:16>: Most Recent DMA Address Accessed by DMA bits

REGISTER 8-10: DSADRL: DMA MOST RECENT RAM LOW ADDRESS REGISTER

R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0
			DSAI	DR<15:8>			
bit 15							bit 8
R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0
			DSA	DR<7:0>			
bit 7							bit 0
Legend:							
R = Readable	bit	W = Writable bit		U = Unimplemer	nted bit, re	ad as '0'	
-n = Value at P	OR	'1' = Bit is set		'0' = Bit is cleare	d	x = Bit is unknown	

bit 15-0 DSADR<15:0>: Most Recent DMA Address Accessed by DMA bits

12.1 Timer1 Resources

Many useful resources are provided on the main product page of the Microchip web site for the devices listed in this data sheet. This product page, which can be accessed using this link, contains the latest updates and additional information.

Note:	In the event you are not able to access the
	product page using the link above, enter
	this URL in your browser:
	http://www.microchip.com/wwwproducts/
	Devices.aspx?dDocName=en555464

12.1.1 KEY RESOURCES

- "Timers" (DS70362) in the "dsPIC33/PIC24 Family Reference Manual"
- · Code Samples
- Application Notes
- · Software Libraries
- Webinars
- All Related "dsPIC33/PIC24 Family Reference Manual" Sections
- Development Tools

12.2 Timer1 Control Register

R/W-0	U-0	R/W-0	U-0	U-0	U-0	U-0	U-0						
TON ⁽¹⁾	—	TSIDL	—	_	—	—	—						
bit 15 bi													
U-0	R/W-0	R/W-0	R/W-0	U-0	R/W-0	R/W-0	U-0						
	TGATE	TCKPS1	TCKPS0	_	TSYNC ⁽¹⁾	TCS ⁽¹⁾	—						
bit 7							bit 0						
Legend:													
R = Readab	ole bit	W = Writable	bit	U = Unimpler	mented bit, read	as '0'							
-n = Value a	at POR	'1' = Bit is set		'0' = Bit is cle	ared	x = Bit is unkn	own						
		(1)											
bit 15	TON: Timer1	On bit ⁽¹⁾											
	1 = Starts 16-	bit Limer1 bit Timer1											
bit 1/	Unimplement	ted: Pead as '	ı'										
bit 13		1 Stop in Idle N	/ode hit										
DIC 15	1 = Discontinu	i stop in lae k	eration when a	device enters l	dle mode								
	0 = Continues	module opera	tion in Idle mo	ode									
bit 12-7	Unimplement	ted: Read as ')'										
bit 6	TGATE: Time	TGATE: Timer1 Gated Time Accumulation Enable bit											
	When TCS =	<u>1:</u> prod											
	When TCS =	0. 0.											
	1 = Gated tim	<u>e</u> accumulatior	n is enabled										
	0 = Gated tim	e accumulatior	n is disabled										
bit 5-4	TCKPS<1:0>	: Timer1 Input	Clock Prescal	e Select bits									
	11 = 1:256												
	10 = 1:64 01 = 1:8												
	01 = 1.0 00 = 1.1												
bit 3	Unimplement	ted: Read as ')'										
bit 2	TSYNC: Time	er1 External Clo	ock Input Sync	chronization Se	elect bit ⁽¹⁾								
	When TCS =	1:											
	1 = Synchroni	izes external cl	ock input										
	0 = Does not	synchronize ex	ternal clock in	nput									
	This bit is jand	<u>ored</u> .											
bit 1	TCS: Timer1 (Clock Source S	Select bit ⁽¹⁾										
	1 = External c	lock is from pir	n, T1CK (on th	ne rising edge)									
	0 = Internal cl	ock (FP)		5 5-7									
bit 0	Unimplement	ted: Read as ')'										
Note 1: \	When Timer1 is en attempts by user so	abled in Exterr oftware to write	al Synchrono to the TMR1	us Counter mo register are ig	ode (TCS = 1, T nored.	lote 1: When Timer1 is enabled in External Synchronous Counter mode (TCS = 1, TSYNC = 1, TON = 1), any attempts by user software to write to the TMR1 register are ignored.							

REGISTER 12-1: T1CON: TIMER1 CONTROL REGISTER

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15.0 OUTPUT COMPARE

- Note 1: This data sheet summarizes the features of the dsPIC33EPXXXGP50X, dsPIC33EPXXXMC20X/50X and PIC24EPXXXGP/MC20X families of devices. It is not intended to be a comprehensive reference source. To complement the information in this data sheet, refer to "Output Compare" (DS70358) in the "dsPIC33/PIC24 Family Reference Manual", which is available from the Microchip web site (www.microchip.com).
 - 2: Some registers and associated bits described in this section may not be available on all devices. Refer to Section 4.0 "Memory Organization" in this data sheet for device-specific register and bit information.

The output compare module can select one of seven available clock sources for its time base. The module compares the value of the timer with the value of one or two compare registers depending on the operating mode selected. The state of the output pin changes when the timer value matches the compare register value. The output compare module generates either a single output pulse or a sequence of output pulses, by changing the state of the output pin on the compare match events. The output compare module can also generate interrupts on compare match events and trigger DMA data transfers.

Note: See "Output Compare" (DS70358) in the "dsPIC33/PIC24 Family Reference Manual" for OCxR and OCxRS register restrictions.





REGISTER 17-1: QEI1CON: QEI1 CONTROL REGISTER (CONTINUED)

bit 6-4	INTDIV<2:0>: Timer Input Clock Prescale Select bits (interval timer, main timer (position counter), velocity counter and index counter internal clock divider select) ⁽³⁾						
	<pre>111 = 1:128 prescale value 110 = 1:64 prescale value 101 = 1:32 prescale value 100 = 1:16 prescale value 011 = 1:8 prescale value 010 = 1:4 prescale value 001 = 1:2 prescale value 000 = 1:1 prescale value</pre>						
bit 3	CNTPOL: Position and Index Counter/Timer Direction Select bit						
	 0 = Counter direction is positive unless modified by external up/down signal 						
bit 2	GATEN: External Count Gate Enable bit						
	 1 = External gate signal controls position counter operation 0 = External gate signal does not affect position counter/timer operation 						
bit 1-0	CCM<1:0>: Counter Control Mode Selection bits						
	 11 = Internal Timer mode with optional external count is selected 10 = External clock count with optional external count is selected 01 = External clock count with external up/down direction is selected 00 = Quadrature Encoder Interface (x4 mode) Count mode is selected 						
Note 1:	When CCM<1:0> = 10 or 11, all of the QEI counters operate as timers and the PIMOD<2:0> bits are ignored.						

- 2: When CCM<1:0> = 00, and QEA and QEB values match the Index Match Value (IMV), the POSCNTH and POSCNTL registers are reset. QEA/QEB signals used for the index match have swap and polarity values applied, as determined by the SWPAB and QEAPOL/QEBPOL bits.
- 3: The selected clock rate should be at least twice the expected maximum quadrature count rate.

REGISTER 25-5: CMxMSKCON: COMPARATOR x MASK GATING CONTROL REGISTER (CONTINUED)

bit 3 ABEN: AND Gate B Input Enable bit 1 = MBI is connected to AND gate 0 = MBI is not connected to AND gate bit 2 ABNEN: AND Gate B Input Inverted Enable bit 1 = Inverted MBI is connected to AND gate 0 = Inverted MBI is not connected to AND gate bit 1 AAEN: AND Gate A Input Enable bit 1 = MAI is connected to AND gate 0 = MAI is not connected to AND gate bit 0 AANEN: AND Gate A Input Inverted Enable bit 1 = Inverted MAI is connected to AND gate 0 = Inverted MAI is not connected to AND gate

Field	Description					
Wm,Wn	Dividend, Divisor working register pair (direct addressing)					
Wm*Wm	Multiplicand and Multiplier working register pair for Square instructions ∈ {W4 * W4,W5 * W5,W6 * W6,W7 * W7}					
Wm*Wn	Multiplicand and Multiplier working register pair for DSP instructions ∈ {W4 * W5,W4 * W6,W4 * W7,W5 * W6,W5 * W7,W6 * W7}					
Wn	One of 16 working registers ∈ {W0W15}					
Wnd	One of 16 destination working registers ∈ {W0W15}					
Wns	One of 16 source working registers ∈ {W0W15}					
WREG	W0 (working register used in file register instructions)					
Ws	Source W register ∈ { Ws, [Ws], [Ws++], [Ws], [++Ws], [Ws] }					
Wso	Source W register ∈ { Wns, [Wns], [Wns++], [Wns], [++Wns], [Wns], [Wns+Wb] }					
Wx	X Data Space Prefetch Address register for DSP instructions ∈ {[W8] + = 6, [W8] + = 4, [W8] + = 2, [W8], [W8] - = 6, [W8] - = 4, [W8] - = 2, [W9] + = 6, [W9] + = 4, [W9] + = 2, [W9], [W9] - = 6, [W9] - = 4, [W9] - = 2, [W9 + W12], none}					
Wxd	X Data Space Prefetch Destination register for DSP instructions ∈ {W4W7}					
Wy	Y Data Space Prefetch Address register for DSP instructions ∈ {[W10] + = 6, [W10] + = 4, [W10] + = 2, [W10], [W10] - = 6, [W10] - = 4, [W10] - = 2, [W11] + = 6, [W11] + = 4, [W11] + = 2, [W11], [W11] - = 6, [W11] - = 4, [W11] - = 2, [W11 + W12], none}					
Wyd	Y Data Space Prefetch Destination register for DSP instructions ∈ {W4W7}					

TABLE 28-1:	SYMBOLS USED IN OPCODE DESCRIPTIONS ((CONTINUED)

AC CHARACTERISTICS			Standard Operating Conditions: 3.0V to 3.6V(unless otherwise stated)Operating temperature $-40^{\circ}C \le TA \le +85^{\circ}C$ for Industrial $40^{\circ}C \le TA \le +125^{\circ}C$ for Extended					
Param No.	Symbol	Characteristic ⁽¹⁾	Min.	Typ. ⁽²⁾	Max.	Units	Conditions	
SY00	Τρυ	Power-up Period	—	400	600	μS		
SY10	Tost	Oscillator Start-up Time	_	1024 Tosc			Tosc = OSC1 period	
SY12	Twdt	Watchdog Timer Time-out Period	0.81	0.98	1.22	ms	WDTPRE = 0, WDTPOST<3:0> = 0000, using LPRC tolerances indicated in F21 (see Table 30-20) at +85°C	
			3.26	3.91	4.88	ms	WDTPRE = 1, WDTPOST<3:0> = 0000, using LPRC tolerances indicated in F21 (see Table 30-20) at +85°C	
SY13	Tioz	I/O High-Impedance from MCLR Low or Watchdog Timer Reset	0.68	0.72	1.2	μS		
SY20	TMCLR	MCLR Pulse Width (low)	2	—	_	μS		
SY30	TBOR	BOR Pulse Width (low)	1	_	_	μS		
SY35	TFSCM	Fail-Safe Clock Monitor Delay	—	500	900	μS	-40°C to +85°C	
SY36	TVREG	Voltage Regulator Standby-to-Active mode Transition Time	—	_	30	μS		
SY37	Toscdfrc	FRC Oscillator Start-up Delay	46	48	54	μS		
SY38	TOSCDLPRC	LPRC Oscillator Start-up Delay	—	_	70	μS		

TABLE 30-22:RESET, WATCHDOG TIMER, OSCILLATOR START-UP TIMER, POWER-UP TIMERTIMING REQUIREMENTS

Note 1: These parameters are characterized but not tested in manufacturing.

2: Data in "Typical" column is at 3.3V, +25°C unless otherwise stated.

AC CHARACTERISTICS				Standard Oper (unless otherw Operating temp	ating Co vise stat perature	onditions: 3.0V ed) -40°C ≤ TA ≤ + -40°C ≤ TA ≤ +	to 3.6V -85°C foi -125°C fo	r Industrial pr Extended
Param No.	Symbol	Characteristic ⁽¹⁾		Min.	Тур.	Max.	Units	Conditions
ТВ10	TtxH	TxCK High Time	Synchronous mode	Greater of: 20 or (TcY + 20)/N		_	ns	Must also meet Parameter TB15, N = prescale value (1, 8, 64, 256)
TB11	TtxL	TxCK Low Time	Synchronous mode	Greater of: 20 or (Tcy + 20)/N	_	_	ns	Must also meet Parameter TB15, N = prescale value (1, 8, 64, 256)
TB15	TtxP	TxCK Input Period	Synchronous mode	Greater of: 40 or (2 Tcy + 40)/N		_	ns	N = prescale value (1, 8, 64, 256)
TB20	TCKEXTMRL	Delay from External TxCK Clock Edge to Timer Increment		0.75 Tcy + 40		1.75 Tcy + 40	ns	

TABLE 30-24:	TIMER2 AND TI	MER4 (TYPE B TIM	ER) EXTERNAL CLOC	K TIMING REQUIREMENTS
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Note 1: These parameters are characterized, but are not tested in manufacturing.

TABLE 30-25: TIMER3 AND TIMER5 (TYPE C TIMER) EXTERNAL CLOCK TIMING REQUIREMENTS

AC CHARACTERISTICS				$\begin{array}{l} \mbox{Standard Operating Conditions: 3.0V to 3.6V} \\ \mbox{(unless otherwise stated)} \\ \mbox{Operating temperature} & -40^{\circ}C \leq TA \leq +85^{\circ}C \mbox{ for Industrial} \\ & -40^{\circ}C \leq TA \leq +125^{\circ}C \mbox{ for Extended} \end{array}$				
Param No.	Symbol	Characteristic ⁽¹⁾		Min.	Тур.	Max.	Units	Conditions
TC10	TtxH	TxCK High Time	Synchronous	Tcy + 20	—	—	ns	Must also meet Parameter TC15
TC11	TtxL	TxCK Low Time	Synchronous	Tcy + 20	—	—	ns	Must also meet Parameter TC15
TC15	TtxP	TxCK Input Period	Synchronous, with prescaler	2 Tcy + 40	—	_	ns	N = prescale value (1, 8, 64, 256)
TC20	TCKEXTMRL	Delay from External TxCK Clock Edge to Timer Increment		0.75 Tcy + 40		1.75 Tcy + 40	ns	

Note 1: These parameters are characterized, but are not tested in manufacturing.



FIGURE 30-13: QEI MODULE INDEX PULSE TIMING CHARACTERISTICS (dsPIC33EPXXXMC20X/50X and PIC24EPXXXMC20X DEVICES ONLY)

TABLE 30-32: QEI INDEX PULSE TIMING REQUIREMENTS (dsPIC33EPXXXMC20X/50X and PIC24EPXXXMC20X DEVICES ONLY)

AC CHARACTERISTICS			$\begin{tabular}{lllllllllllllllllllllllllllllllllll$				
Param No.	Symbol	Characteristic ⁽¹⁾	Min.	Conditions			
TQ50	TqiL	Filter Time to Recognize Low, with Digital Filter	3 * N * Tcy	_	ns	N = 1, 2, 4, 16, 32, 64, 128 and 256 (Note 2)	
TQ51	TqiH	Filter Time to Recognize High, with Digital Filter	3 * N * Tcy	—	ns	N = 1, 2, 4, 16, 32, 64, 128 and 256 (Note 2)	
TQ55	Tqidxr	Index Pulse Recognized to Position Counter Reset (ungated index)	3 TCY	—	ns		

Note 1: These parameters are characterized but not tested in manufacturing.

2: Alignment of index pulses to QEA and QEB is shown for position counter Reset timing only. Shown for forward direction only (QEA leads QEB). Same timing applies for reverse direction (QEA lags QEB) but index pulse recognition occurs on the falling edge.

TABLE 30-39:SPI2 SLAVE MODE (FULL-DUPLEX, CKE = 0, CKP = 1, SMP = 0)TIMING REQUIREMENTS

AC CHARACTERISTICS			$\begin{array}{l} \mbox{Standard Operating Conditions: 3.0V to 3.6V} \\ \mbox{(unless otherwise stated)} \\ \mbox{Operating temperature} & -40^{\circ}C \leq TA \leq +85^{\circ}C \mbox{ for Industrial} \\ & -40^{\circ}C \leq TA \leq +125^{\circ}C \mbox{ for Extended} \end{array}$				
Param.	Symbol	Characteristic ⁽¹⁾	Min.	Typ. ⁽²⁾	Max.	Units	Conditions
SP70	FscP	Maximum SCK2 Input Frequency			15	MHz	(Note 3)
SP72	TscF	SCK2 Input Fall Time	—		_	ns	See Parameter DO32 (Note 4)
SP73	TscR	SCK2 Input Rise Time	—		_	ns	See Parameter DO31 (Note 4)
SP30	TdoF	SDO2 Data Output Fall Time	—		—	ns	See Parameter DO32 (Note 4)
SP31	TdoR	SDO2 Data Output Rise Time	—		_	ns	See Parameter DO31 (Note 4)
SP35	TscH2doV, TscL2doV	SDO2 Data Output Valid after SCK2 Edge	—	6	20	ns	
SP36	TdoV2scH, TdoV2scL	SDO2 Data Output Setup to First SCK2 Edge	30	_	_	ns	
SP40	TdiV2scH, TdiV2scL	Setup Time of SDI2 Data Input to SCK2 Edge	30	_	_	ns	
SP41	TscH2diL, TscL2diL	Hold Time of SDI2 Data Input to SCK2 Edge	30		_	ns	
SP50	TssL2scH, TssL2scL	$\overline{SS2}$ ↓ to SCK2 ↑ or SCK2 ↓ Input	120		_	ns	
SP51	TssH2doZ	SS2 ↑ to SDO2 Output High-Impedance	10	_	50	ns	(Note 4)
SP52	TscH2ssH TscL2ssH	SS2 ↑ after SCK2 Edge	1.5 Tcy + 40	_	_	ns	(Note 4)

Note 1: These parameters are characterized, but are not tested in manufacturing.

2: Data in "Typical" column is at 3.3V, +25°C unless otherwise stated.

3: The minimum clock period for SCK2 is 66.7 ns. Therefore, the SCK2 clock generated by the master must not violate this specification.

4: Assumes 50 pF load on all SPI2 pins.

TABLE 30-46:SPI1 SLAVE MODE (FULL-DUPLEX, CKE = 1, CKP = 1, SMP = 0)TIMING REQUIREMENTS

AC CHARACTERISTICS			$\begin{array}{l} \mbox{Standard Operating Conditions: 3.0V to 3.6V} \\ \mbox{(unless otherwise stated)} \\ \mbox{Operating temperature} & -40^{\circ}C \leq TA \leq +85^{\circ}C \mbox{ for Industrial} \\ & -40^{\circ}C \leq TA \leq +125^{\circ}C \mbox{ for Extended} \end{array}$					
Param.	Symbol	Characteristic ⁽¹⁾	aracteristic ⁽¹⁾ Min. Typ. ⁽²⁾ Max. Units					
SP70	FscP	Maximum SCK1 Input Frequency	—	—	Lesserof FP or 11	MHz	(Note 3)	
SP72	TscF	SCK1 Input Fall Time	—	_	_	ns	See Parameter DO32 (Note 4)	
SP73	TscR	SCK1 Input Rise Time	—	_	_	ns	See Parameter DO31 (Note 4)	
SP30	TdoF	SDO1 Data Output Fall Time	—	—	—	ns	See Parameter DO32 (Note 4)	
SP31	TdoR	SDO1 Data Output Rise Time	—	-	—	ns	See Parameter DO31 (Note 4)	
SP35	TscH2doV, TscL2doV	SDO1 Data Output Valid after SCK1 Edge	—	6	20	ns		
SP36	TdoV2scH, TdoV2scL	SDO1 Data Output Setup to First SCK1 Edge	30	—	_	ns		
SP40	TdiV2scH, TdiV2scL	Setup Time of SDI1 Data Input to SCK1 Edge	30	-	—	ns		
SP41	TscH2diL, TscL2diL	Hold Time of SDI1 Data Input to SCK1 Edge	30	-	—	ns		
SP50	TssL2scH, TssL2scL	$\overline{SS1}$ ↓ to SCK1 ↑ or SCK1 ↓ Input	120	—	—	ns		
SP51	TssH2doZ	SS1 ↑ to SDO1 Output High-Impedance	10	—	50	ns	(Note 4)	
SP52	TscH2ssH, TscL2ssH	SS1 ↑ after SCK1 Edge	1.5 Tcy + 40	—	—	ns	(Note 4)	
SP60	TssL2doV	SDO1 Data Output Valid after SS1 Edge	—	—	50	ns		

Note 1: These parameters are characterized, but are not tested in manufacturing.

2: Data in "Typical" column is at 3.3V, +25°C unless otherwise stated.

3: The minimum clock period for SCK1 is 91 ns. Therefore, the SCK1 clock generated by the master must not violate this specification.

4: Assumes 50 pF load on all SPI1 pins.









FIGURE 30-34: ECAN_x MODULE I/O TIMING CHARACTERISTICS

TABLE 30-51: ECANx MODULE I/O TIMING REQUIREMENTS

AC CHARACTERISTICS			$\begin{array}{l} \mbox{Standard Operating Conditions: 3.0V to 3.6V} \\ \mbox{(unless otherwise stated)} \\ \mbox{Operating temperature} & -40^\circ C \leq TA \leq +85^\circ C \mbox{ for Industrial} \\ & -40^\circ C \leq TA \leq +125^\circ C \mbox{ for Extended} \end{array}$				
Param No.	Symbol	Characteristic ⁽¹⁾	Min.	Тур. ⁽²⁾	Max.	Units	Conditions
CA10	TIOF	Port Output Fall Time		_	_	ns	See Parameter DO32
CA11	TIOR	Port Output Rise Time		_	_	ns	See Parameter DO31
CA20	TCWF	Pulse Width to Trigger CAN Wake-up Filter	120			ns	

Note 1: These parameters are characterized but not tested in manufacturing.

2: Data in "Typical" column is at 3.3V, +25°C unless otherwise stated. Parameters are for design guidance only and are not tested.

FIGURE 30-35: UARTX MODULE I/O TIMING CHARACTERISTICS



TABLE 30-52: UARTX MODULE I/O TIMING REQUIREMENTS

AC CHARACTERISTICS				Standard Operating Conditions: 3.0V to 3.6V (unless otherwise stated) Operating temperature -40°C \leq TA \leq +125°C				
Param No. Symbol Characteristic ⁽¹⁾			Min.	Тур. ⁽²⁾	Max.	Units	Conditions	
UA10	TUABAUD	UARTx Baud Time	66.67	_	_	ns		
UA11	FBAUD	UARTx Baud Frequency	—	—	15	Mbps		
UA20	TCWF	Start Bit Pulse Width to Trigger UARTx Wake-up	500	_	_	ns		

Note 1: These parameters are characterized but not tested in manufacturing.

2: Data in "Typical" column is at 3.3V, +25°C unless otherwise stated. Parameters are for design guidance only and are not tested.

DC CHARACTERISTICS			Standard Operating Conditions: 3.0V to 3.6V(unless otherwise stated)(1)Operating temperature $-40^{\circ}C \le TA \le +85^{\circ}C$ for Industrial						
			-40°C \leq TA \leq +125°C for Extended						
Param No.	Symbol	Characteristic	Min.	Тур. ⁽²⁾	Max.	Units	Conditions		
Compa	rator AC Ch	naracteristics							
CM10	Tresp	Response Time ⁽³⁾	_	19	_	ns	V+ input step of 100 mV, V- input held at VDD/2		
CM11	Тмс2о∨	Comparator Mode Change to Output Valid		_	10	μs			
Compa	rator DC Ch	naracteristics							
CM30	VOFFSET	Comparator Offset Voltage	—	±10	40	mV			
CM31	VHYST	Input Hysteresis Voltage ⁽³⁾	_	30	—	mV			
CM32	Trise/ Tfall	Comparator Output Rise/ Fall Time ⁽³⁾	—	20	—	ns	1 pF load capacitance on input		
CM33	Vgain	Open-Loop Voltage Gain ⁽³⁾	—	90	—	db			
CM34	VICM	Input Common-Mode Voltage	AVss	—	AVdd	V			
Op Am	p AC Chara	cteristics							
CM20	SR	Slew Rate ⁽³⁾		9		V/µs	10 pF load		
CM21a	Рм	Phase Margin (Configuration A) ^(3,4)	_	55	—	Degree	G = 100V/V; 10 pF load		
CM21b	Рм	Phase Margin (Configuration B) ^(3,5)	_	40	—	Degree	G = 100V/V; 10 pF load		
CM22	Gм	Gain Margin ⁽³⁾	_	20	—	db	G = 100V/V; 10 pF load		
CM23a	Gвw	Gain Bandwidth (Configuration A) ^(3,4)	_	10	—	MHz	10 pF load		
CM23b	Gвw	Gain Bandwidth (Configuration B) ^(3,5)	—	6	—	MHz	10 pF load		

TABLE 30-53: OP AMP/COMPARATOR SPECIFICATIONS

Note 1: Device is functional at VBORMIN < VDD < VDDMIN, but will have degraded performance. Device functionality is tested, but not characterized. Analog modules (ADC, op amp/comparator and comparator voltage reference) may have degraded performance. Refer to Parameter BO10 in Table 30-13 for the minimum and maximum BOR values.

- 2: Data in "Typ" column is at 3.3V, +25°C unless otherwise stated.
- 3: Parameter is characterized but not tested in manufacturing.
- 4: See Figure 25-6 for configuration information.
- 5: See Figure 25-7 for configuration information.
- 6: Resistances can vary by ±10% between op amps.