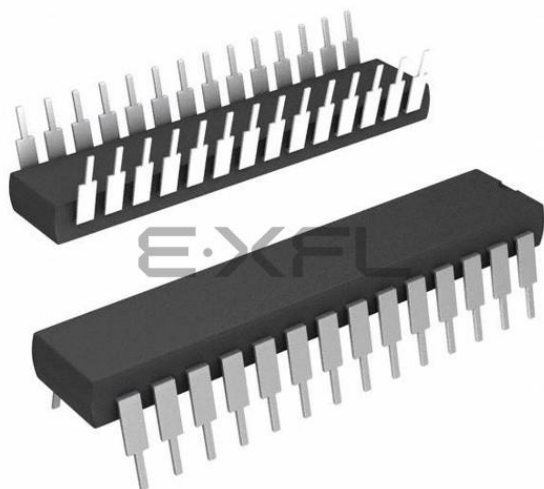




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Details

Product Status	Obsolete
Core Processor	PIC
Core Size	16-Bit
Speed	60 MIPS
Connectivity	I ² C, IrDA, LINbus, QEI, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, DMA, Motor Control PWM, POR, PWM, WDT
Number of I/O	21
Program Memory Size	256KB (85.5K x 24)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	16K x 16
Voltage - Supply (Vcc/Vdd)	3V ~ 3.6V
Data Converters	A/D 6x10b/12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 150°C (TA)
Mounting Type	Through Hole
Package / Case	28-DIP (0.300", 7.62mm)
Supplier Device Package	28-SPDIP
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/pic24ep256mc202-h-sp

TABLE 1-1: PINOUT I/O DESCRIPTIONS (CONTINUED)

Pin Name ⁽⁴⁾	Pin Type	Buffer Type	PPS	Description
C1IN1- C1IN2- C1IN1+ OA1OUT C1OUT	I I I O O	Analog Analog Analog Analog —	No No No No Yes	Op Amp/Comparator 1 Negative Input 1. Comparator 1 Negative Input 2. Op Amp/Comparator 1 Positive Input 1. Op Amp 1 output. Comparator 1 output.
C2IN1- C2IN2- C2IN1+ OA2OUT C2OUT	I I I O O	Analog Analog Analog Analog —	No No No No Yes	Op Amp/Comparator 2 Negative Input 1. Comparator 2 Negative Input 2. Op Amp/Comparator 2 Positive Input 1. Op Amp 2 output. Comparator 2 output.
C3IN1- C3IN2- C3IN1+ OA3OUT C3OUT	I I I O O	Analog Analog Analog Analog —	No No No No Yes	Op Amp/Comparator 3 Negative Input 1. Comparator 3 Negative Input 2. Op Amp/Comparator 3 Positive Input 1. Op Amp 3 output. Comparator 3 output.
C4IN1- C4IN1+ C4OUT	I I O	Analog Analog —	No No Yes	Comparator 4 Negative Input 1. Comparator 4 Positive Input 1. Comparator 4 output.
CVREF10 CVREF20	O O	Analog Analog	No No	Op amp/comparator voltage reference output. Op amp/comparator voltage reference divided by 2 output.
PGED1 PGEC1 PGED2 PGEC2 PGED3 PGEC3	I/O I I/O I I/O I	ST ST ST ST ST ST	No No No No No No	Data I/O pin for Programming/Debugging Communication Channel 1. Clock input pin for Programming/Debugging Communication Channel 1. Data I/O pin for Programming/Debugging Communication Channel 2. Clock input pin for Programming/Debugging Communication Channel 2. Data I/O pin for Programming/Debugging Communication Channel 3. Clock input pin for Programming/Debugging Communication Channel 3.
MCLR	I/P	ST	No	Master Clear (Reset) input. This pin is an active-low Reset to the device.
AVDD	P	P	No	Positive supply for analog modules. This pin must be connected at all times.
AVSS	P	P	No	Ground reference for analog modules. This pin must be connected at all times.
VDD	P	—	No	Positive supply for peripheral logic and I/O pins.
VCAP	P	—	No	CPU logic filter capacitor connection.
VSS	P	—	No	Ground reference for logic and I/O pins.
VREF+	I	Analog	No	Analog voltage reference (high) input.
VREF-	I	Analog	No	Analog voltage reference (low) input.

Legend: CMOS = CMOS compatible input or output Analog = Analog input P = Power
ST = Schmitt Trigger input with CMOS levels O = Output I = Input
PPS = Peripheral Pin Select TTL = TTL input buffer

- Note 1:** This pin is available on dsPIC33EPXXXMC20X/50X and PIC24EPXXXMC20X devices only.
- Note 2:** This pin is available on dsPIC33EPXXXGP/MC50X devices only.
- Note 3:** This is the default Fault on Reset for dsPIC33EPXXXMC20X/50X and PIC24EPXXXMC20X devices. See **Section 16.0 “High-Speed PWM Module (dsPIC33EPXXXMC20X/50X and PIC24EPXXXMC20X Devices Only)”** for more information.
- Note 4:** Not all pins are available in all packages variants. See the “Pin Diagrams” section for pin availability.
- Note 5:** There is an internal pull-up resistor connected to the TMS pin when the JTAG interface is active. See the JTAGEN bit field in Table 27-2.

TABLE 4-2: CPU CORE REGISTER MAP FOR PIC24EPXXXGP/MC20X DEVICES ONLY

File Name	Addr.	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	All Resets	
W0	0000	W0 (WREG)																XXXX	
W1	0002	W1																XXXX	
W2	0004	W2																XXXX	
W3	0006	W3																XXXX	
W4	0008	W4																XXXX	
W5	000A	W5																XXXX	
W6	000C	W6																XXXX	
W7	000E	W7																XXXX	
W8	0010	W8																XXXX	
W9	0012	W9																XXXX	
W10	0014	W10																XXXX	
W11	0016	W11																XXXX	
W12	0018	W12																XXXX	
W13	001A	W13																XXXX	
W14	001C	W14																XXXX	
W15	001E	W15																XXXX	
SPLIM	0020	SPLIM<15:0>																0000	
PCL	002E	PCL<15:1>																—	0000
PCH	0030	—	—	—	—	—	—	—	—	—	PCH<6:0>							0000	
DSRPAG	0032	—	—	—	—	—	—	DSRPAG<9:0>										0001	
DSWPAG	0034	—	—	—	—	—	—	—	DSWPAG<8:0>										0001
RCOUNT	0036	RCOUNT<15:0>																0000	
SR	0042	—	—	—	—	—	—	—	DC	IPL2	IPL1	IPL0	RA	N	OV	Z	C	0000	
CORCON	0044	VAR	—	—	—	—	—	—	—	—	—	—	—	IPL3	SFA	—	—	0020	
DISICNT	0052	—	—	DISICNT<13:0>														0000	
TBLPAG	0054	—	—	—	—	—	—	—	—	TBLPAG<7:0>									0000
MSTRPR	0058	MSTRPR<15:0>																0000	

Legend: x = unknown value on Reset, — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

4.4.1 PAGED MEMORY SCHEME

The dsPIC33EPXXXGP50X, dsPIC33EPXXXMC20X/50X and PIC24EPXXXGP/MC20X architecture extends the available Data Space through a paging scheme, which allows the available Data Space to be accessed using MOV instructions in a linear fashion for pre-modified and post-modified Effective Addresses (EA). The upper half of the base Data Space address is used in conjunction with the Data Space Page registers, the 10-bit Read Page register (DSRPAG) or the 9-bit Write Page register (DSWPAG), to form an Extended Data Space (EDS)

address or Program Space Visibility (PSV) address. The Data Space Page registers are located in the SFR space.

Construction of the EDS address is shown in Example 4-1. When DSRPAG<9> = 0 and the base address bit, EA<15> = 1, the DSRPAG<8:0> bits are concatenated onto EA<14:0> to form the 24-bit EDS read address. Similarly, when base address bit, EA<15> = 1, DSWPAG<8:0> are concatenated onto EA<14:0> to form the 24-bit EDS write address.

EXAMPLE 4-1: EXTENDED DATA SPACE (EDS) READ ADDRESS GENERATION

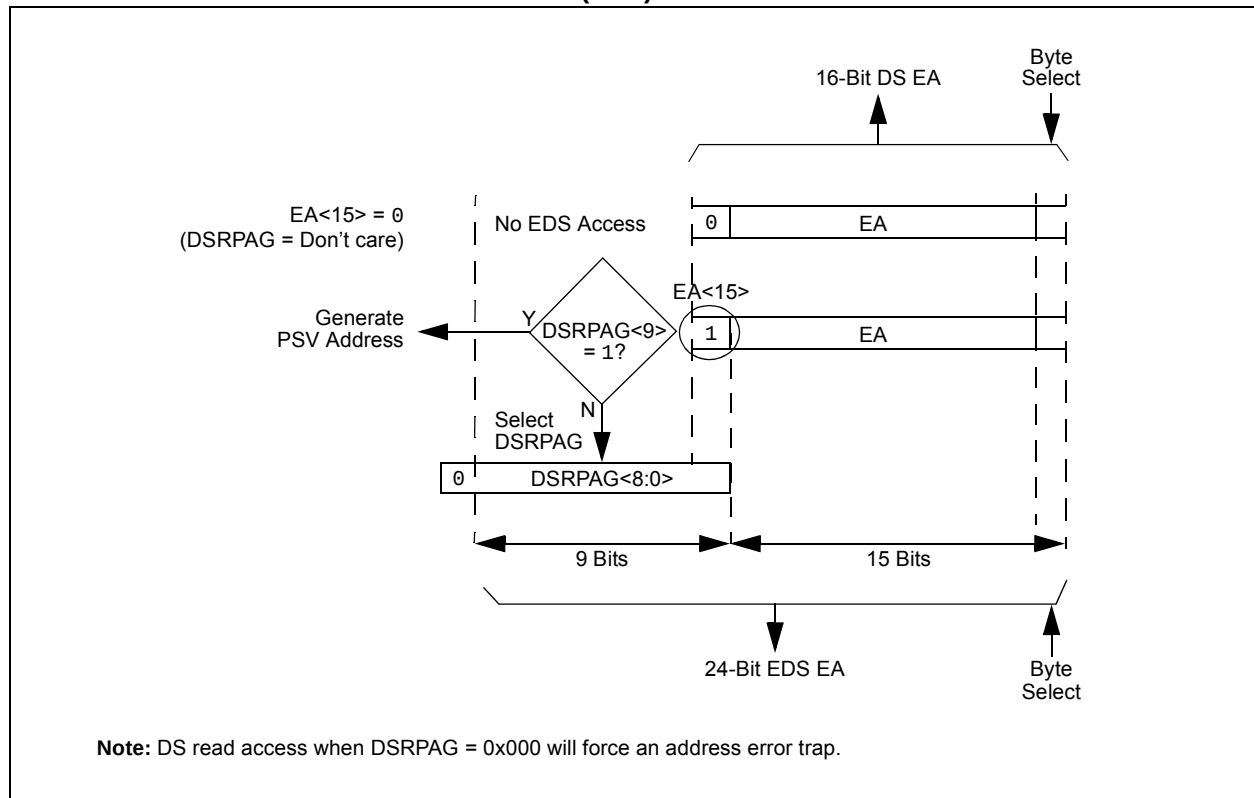


TABLE 7-1: INTERRUPT VECTOR DETAILS

Interrupt Source	Vector #	IRQ #	IVT Address	Interrupt Bit Location		
				Flag	Enable	Priority
Highest Natural Order Priority						
INT0 – External Interrupt 0	8	0	0x000014	IFS0<0>	IEC0<0>	IPC0<2:0>
IC1 – Input Capture 1	9	1	0x000016	IFS0<1>	IEC0<1>	IPC0<6:4>
OC1 – Output Compare 1	10	2	0x000018	IFS0<2>	IEC0<2>	IPC0<10:8>
T1 – Timer1	11	3	0x00001A	IFS0<3>	IEC0<3>	IPC0<14:12>
DMA0 – DMA Channel 0	12	4	0x00001C	IFS0<4>	IEC0<4>	IPC1<2:0>
IC2 – Input Capture 2	13	5	0x00001E	IFS0<5>	IEC0<5>	IPC1<6:4>
OC2 – Output Compare 2	14	6	0x000020	IFS0<6>	IEC0<6>	IPC1<10:8>
T2 – Timer2	15	7	0x000022	IFS0<7>	IEC0<7>	IPC1<14:12>
T3 – Timer3	16	8	0x000024	IFS0<8>	IEC0<8>	IPC2<2:0>
SPI1E – SPI1 Error	17	9	0x000026	IFS0<9>	IEC0<9>	IPC2<6:4>
SPI1 – SPI1 Transfer Done	18	10	0x000028	IFS0<10>	IEC0<10>	IPC2<10:8>
U1RX – UART1 Receiver	19	11	0x00002A	IFS0<11>	IEC0<11>	IPC2<14:12>
U1TX – UART1 Transmitter	20	12	0x00002C	IFS0<12>	IEC0<12>	IPC3<2:0>
AD1 – ADC1 Convert Done	21	13	0x00002E	IFS0<13>	IEC0<13>	IPC3<6:4>
DMA1 – DMA Channel 1	22	14	0x000030	IFS0<14>	IEC0<14>	IPC3<10:8>
Reserved	23	15	0x000032	—	—	—
SI2C1 – I2C1 Slave Event	24	16	0x000034	IFS1<0>	IEC1<0>	IPC4<2:0>
MI2C1 – I2C1 Master Event	25	17	0x000036	IFS1<1>	IEC1<1>	IPC4<6:4>
CM – Comparator Combined Event	26	18	0x000038	IFS1<2>	IEC1<2>	IPC4<10:8>
CN – Input Change Interrupt	27	19	0x00003A	IFS1<3>	IEC1<3>	IPC4<14:12>
INT1 – External Interrupt 1	28	20	0x00003C	IFS1<4>	IEC1<4>	IPC5<2:0>
Reserved	29-31	21-23	0x00003E-0x000042	—	—	—
DMA2 – DMA Channel 2	32	24	0x000044	IFS1<8>	IEC1<8>	IPC6<2:0>
OC3 – Output Compare 3	33	25	0x000046	IFS1<9>	IEC1<9>	IPC6<6:4>
OC4 – Output Compare 4	34	26	0x000048	IFS1<10>	IEC1<10>	IPC6<10:8>
T4 – Timer4	35	27	0x00004A	IFS1<11>	IEC1<11>	IPC6<14:12>
T5 – Timer5	36	28	0x00004C	IFS1<12>	IEC1<12>	IPC7<2:0>
INT2 – External Interrupt 2	37	29	0x00004E	IFS1<13>	IEC1<13>	IPC7<6:4>
U2RX – UART2 Receiver	38	30	0x000050	IFS1<14>	IEC1<14>	IPC7<10:8>
U2TX – UART2 Transmitter	39	31	0x000052	IFS1<15>	IEC1<15>	IPC7<14:12>
SPI2E – SPI2 Error	40	32	0x000054	IFS2<0>	IEC2<0>	IPC8<2:0>
SPI2 – SPI2 Transfer Done	41	33	0x000056	IFS2<1>	IEC2<1>	IPC8<6:4>
C1RX – CAN1 RX Data Ready ⁽¹⁾	42	34	0x000058	IFS2<2>	IEC2<2>	IPC8<10:8>
C1 – CAN1 Event ⁽¹⁾	43	35	0x00005A	IFS2<3>	IEC2<3>	IPC8<14:12>
DMA3 – DMA Channel 3	44	36	0x00005C	IFS2<4>	IEC2<4>	IPC9<2:0>
IC3 – Input Capture 3	45	37	0x00005E	IFS2<5>	IEC2<5>	IPC9<6:4>
IC4 – Input Capture 4	46	38	0x000060	IFS2<6>	IEC2<6>	IPC9<10:8>
Reserved	47-56	39-48	0x000062-0x000074	—	—	—
SI2C2 – I2C2 Slave Event	57	49	0x000076	IFS3<1>	IEC3<1>	IPC12<6:4>
MI2C2 – I2C2 Master Event	58	50	0x000078	IFS3<2>	IEC3<2>	IPC12<10:8>
Reserved	59-64	51-56	0x00007A-0x000084	—	—	—
PSEM – PWM Special Event Match ⁽²⁾	65	57	0x000086	IFS3<9>	IEC3<9>	IPC14<6:4>

Note 1: This interrupt source is available on dsPIC33EPXXXGP50X and dsPIC33EPXXXMC50X devices only.

Note 2: This interrupt source is available on dsPIC33EPXXXMC20X/50X and PIC24EPXXXMC20X devices only.

REGISTER 7-3: INTCON1: INTERRUPT CONTROL REGISTER 1

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
NSTDIS	OVAERR ⁽¹⁾	OVBERR ⁽¹⁾	COVAERR ⁽¹⁾	COVBERR ⁽¹⁾	OVATE ⁽¹⁾	OVBTE ⁽¹⁾	COVTE ⁽¹⁾
bit 15							bit 8

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	U-0
SFTACERR ⁽¹⁾	DIV0ERR	DMACERR	MATHERR	ADDRERR	STKERR	OSCFail	—
bit 7							bit 0

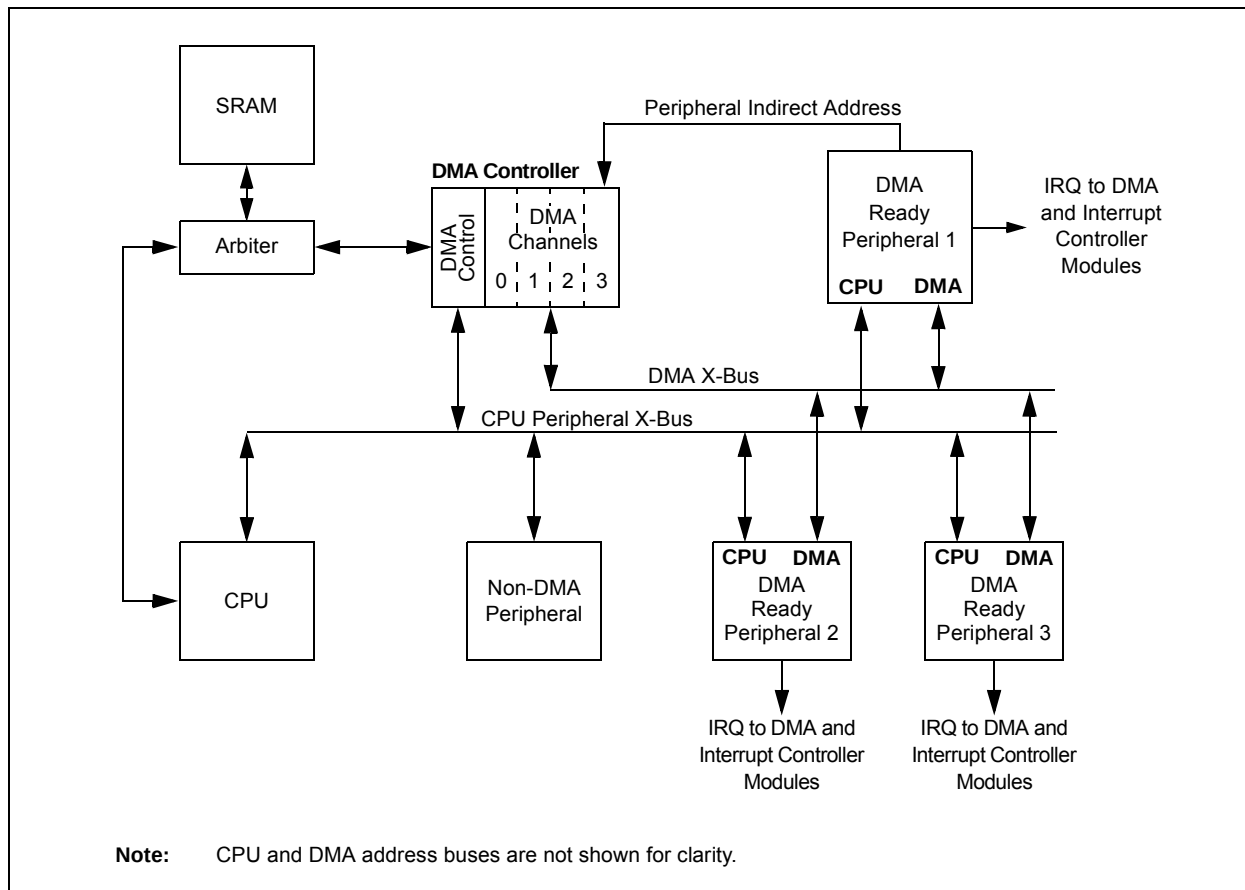
Legend:

R = Readable bit W = Writable bit U = Unimplemented bit, read as '0'
 -n = Value at POR '1' = Bit is set '0' = Bit is cleared x = Bit is unknown

- bit 15 **NSTDIS:** Interrupt Nesting Disable bit
 1 = Interrupt nesting is disabled
 0 = Interrupt nesting is enabled
- bit 14 **OVAERR:** Accumulator A Overflow Trap Flag bit⁽¹⁾
 1 = Trap was caused by overflow of Accumulator A
 0 = Trap was not caused by overflow of Accumulator A
- bit 13 **OVBERR:** Accumulator B Overflow Trap Flag bit⁽¹⁾
 1 = Trap was caused by overflow of Accumulator B
 0 = Trap was not caused by overflow of Accumulator B
- bit 12 **COVAERR:** Accumulator A Catastrophic Overflow Trap Flag bit⁽¹⁾
 1 = Trap was caused by catastrophic overflow of Accumulator A
 0 = Trap was not caused by catastrophic overflow of Accumulator A
- bit 11 **COVBERR:** Accumulator B Catastrophic Overflow Trap Flag bit⁽¹⁾
 1 = Trap was caused by catastrophic overflow of Accumulator B
 0 = Trap was not caused by catastrophic overflow of Accumulator B
- bit 10 **OVATE:** Accumulator A Overflow Trap Enable bit⁽¹⁾
 1 = Trap overflow of Accumulator A
 0 = Trap is disabled
- bit 9 **OVBTE:** Accumulator B Overflow Trap Enable bit⁽¹⁾
 1 = Trap overflow of Accumulator B
 0 = Trap is disabled
- bit 8 **COVTE:** Catastrophic Overflow Trap Enable bit⁽¹⁾
 1 = Trap on catastrophic overflow of Accumulator A or B is enabled
 0 = Trap is disabled
- bit 7 **SFTACERR:** Shift Accumulator Error Status bit⁽¹⁾
 1 = Math error trap was caused by an invalid accumulator shift
 0 = Math error trap was not caused by an invalid accumulator shift
- bit 6 **DIV0ERR:** Divide-by-Zero Error Status bit
 1 = Math error trap was caused by a divide-by-zero
 0 = Math error trap was not caused by a divide-by-zero
- bit 5 **DMACERR:** DMAC Trap Flag bit
 1 = DMAC trap has occurred
 0 = DMAC trap has not occurred

Note 1: These bits are available on dsPIC33EPXXXMC20X/50X and dsPIC33EPXXXGP50X devices only.

FIGURE 8-2: DMA CONTROLLER BLOCK DIAGRAM



8.1 DMA Resources

Many useful resources are provided on the main product page of the Microchip web site for the devices listed in this data sheet. This product page, which can be accessed using this link, contains the latest updates and additional information.

Note: In the event you are not able to access the product page using the link above, enter this URL in your browser:
<http://www.microchip.com/wwwproducts/Devices.aspx?dDocName=en555464>

8.1.1 KEY RESOURCES

- **Section 22. "Direct Memory Access (DMA)"** (DS70348) in the *"dsPIC33/PIC24 Family Reference Manual"*
- Code Samples
- Application Notes
- Software Libraries
- Webinars
- All Related *"dsPIC33/PIC24 Family Reference Manual"* Sections
- Development Tools

8.2 DMAC Registers

Each DMAC Channel x (where $x = 0$ through 3) contains the following registers:

- 16-Bit DMA Channel Control register (DMAxCON)
- 16-Bit DMA Channel IRQ Select register (DMAxREQ)
- 32-Bit DMA RAM Primary Start Address register (DMAxSTA)
- 32-Bit DMA RAM Secondary Start Address register (DMAxSTB)
- 16-Bit DMA Peripheral Address register (DMAxPAD)
- 14-Bit DMA Transfer Count register (DMAxCNT)

Additional status registers (DMAPWC, DMARQC, DMAPPS, DMALCA and DSADR) are common to all DMAC channels. These status registers provide information on write and request collisions, as well as on last address and channel access information.

The interrupt flags (DMAxIF) are located in an IFSx register in the interrupt controller. The corresponding interrupt enable control bits (DMAxIE) are located in an IECx register in the interrupt controller, and the corresponding interrupt priority control bits (DMAxIP) are located in an IPCx register in the interrupt controller.

14.2 Input Capture Registers

REGISTER 14-1: ICxCON1: INPUT CAPTURE x CONTROL REGISTER 1

U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	U-0	U-0
—	—	ICSIDL	ICTSEL2	ICTSEL1	ICTSEL0	—	—
bit 15						bit 8	

U-0	R/W-0	R/W-0	R/HC/HS-0	R/HC/HS-0	R/W-0	R/W-0	R/W-0
—	IC11	IC10	ICOV	ICBNE	ICM2	ICM1	ICM0
bit 7						bit 0	

Legend:	HC = Hardware Clearable bit	HS = Hardware Settable bit
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared x = Bit is unknown

bit 15-14 **Unimplemented:** Read as '0'

bit 13 **ICSIDL:** Input Capture Stop in Idle Control bit
 1 = Input capture will Halt in CPU Idle mode
 0 = Input capture will continue to operate in CPU Idle mode

bit 12-10 **ICTSEL<2:0>:** Input Capture Timer Select bits
 111 = Peripheral clock (FP) is the clock source of the ICx
 110 = Reserved
 101 = Reserved
 100 = T1CLK is the clock source of the ICx (only the synchronous clock is supported)
 011 = T5CLK is the clock source of the ICx
 010 = T4CLK is the clock source of the ICx
 001 = T2CLK is the clock source of the ICx
 000 = T3CLK is the clock source of the ICx

bit 9-7 **Unimplemented:** Read as '0'

bit 6-5 **IC1<1:0>:** Number of Captures per Interrupt Select bits (this field is not used if ICM<2:0> = 001 or 111)
 11 = Interrupt on every fourth capture event
 10 = Interrupt on every third capture event
 01 = Interrupt on every second capture event
 00 = Interrupt on every capture event

bit 4 **ICOV:** Input Capture Overflow Status Flag bit (read-only)
 1 = Input capture buffer overflow occurred
 0 = No input capture buffer overflow occurred

bit 3 **ICBNE:** Input Capture Buffer Not Empty Status bit (read-only)
 1 = Input capture buffer is not empty, at least one more capture value can be read
 0 = Input capture buffer is empty

bit 2-0 **ICM<2:0>:** Input Capture Mode Select bits
 111 = Input capture functions as interrupt pin only in CPU Sleep and Idle modes (rising edge detect only, all other control bits are not applicable)
 110 = Unused (module is disabled)
 101 = Capture mode, every 16th rising edge (Prescaler Capture mode)
 100 = Capture mode, every 4th rising edge (Prescaler Capture mode)
 011 = Capture mode, every rising edge (Simple Capture mode)
 010 = Capture mode, every falling edge (Simple Capture mode)
 001 = Capture mode, every edge rising and falling (Edge Detect mode (IC1<1:0>) is not used in this mode)
 000 = Input capture module is turned off

REGISTER 16-15: FCLCONx: PWMx FAULT CURRENT-LIMIT CONTROL REGISTER⁽¹⁾

- bit 7-3 **FLTSRC<4:0>**: Fault Control Signal Source Select for PWM Generator # bits
- 11111 = Fault 32 (**default**)
 - 11110 = Reserved
 - .
 - .
 - .
 - 01100 = Reserved
 - 01011 = Comparator 4
 - 01010 = Op Amp/Comparator 3
 - 01001 = Op Amp/Comparator 2
 - 01000 = Op Amp/Comparator 1
 - 00111 = Reserved
 - 00110 = Reserved
 - 00101 = Reserved
 - 00100 = Reserved
 - 00011 = Fault 4
 - 00010 = Fault 3
 - 00001 = Fault 2
 - 00000 = Fault 1
- bit 2 **FLTPOL**: Fault Polarity for PWM Generator # bit⁽²⁾
- 1 = The selected Fault source is active-low
 - 0 = The selected Fault source is active-high
- bit 1-0 **FLTMOD<1:0>**: Fault Mode for PWM Generator # bits
- 11 = Fault input is disabled
 - 10 = Reserved
 - 01 = The selected Fault source forces PWMxH, PWMxL pins to FLTDAT values (cycle)
 - 00 = The selected Fault source forces PWMxH, PWMxL pins to FLTDAT values (latched condition)

- Note 1:** If the PWMLOCK Configuration bit (FOSCSEL<6>) is a '1', the IOCONx register can only be written after the unlock sequence has been executed.
- 2:** These bits should be changed only when PTEN = 0. Changing the clock selection during operation will yield unpredictable results.

18.0 SERIAL PERIPHERAL INTERFACE (SPI)

Note 1: This data sheet summarizes the features of the dsPIC33EPXXXGP50X, dsPIC33EPXXXMC20X/50X and PIC24EPXXXGP/MC20X families of devices. It is not intended to be a comprehensive reference source. To complement the information in this data sheet, refer to “**Serial Peripheral Interface (SPI)**” (DS70569) in the “*dsPIC33/PIC24 Family Reference Manual*”, which is available from the Microchip web site (www.microchip.com).

2: Some registers and associated bits described in this section may not be available on all devices. Refer to **Section 4.0 “Memory Organization”** in this data sheet for device-specific register and bit information.

The SPI module is a synchronous serial interface, useful for communicating with other peripheral or microcontroller devices. These peripheral devices can be serial EEPROMs, shift registers, display drivers, ADC Converters, etc. The SPI module is compatible with Motorola® SPI and SIOP interfaces.

The dsPIC33EPXXXGP50X, dsPIC33EPXXXMC20X/50X and PIC24EPXXXGP/MC20X device family offers two SPI modules on a single device. These modules, which are designated as SPI1 and SPI2, are functionally identical. Each SPI module includes an eight-word FIFO buffer and allows DMA bus connections. When using the SPI module with DMA, FIFO operation can be disabled.

Note: In this section, the SPI modules are referred to together as SPIx, or separately as SPI1 and SPI2. Special Function Registers follow a similar notation. For example, SPIxCON refers to the control register for the SPI1 and SPI2 modules.

The SPI1 module uses dedicated pins which allow for a higher speed when using SPI1. The SPI2 module takes advantage of the Peripheral Pin Select (PPS) feature to allow for greater flexibility in pin configuration of the SPI2 module, but results in a lower maximum speed for SPI2. See **Section 30.0 “Electrical Characteristics”** for more information.

The SPIx serial interface consists of four pins, as follows:

- SDIx: Serial Data Input
- SDOx: Serial Data Output
- SCKx: Shift Clock Input or Output
- SSx/FSYNCx: Active-Low Slave Select or Frame Synchronization I/O Pulse

The SPIx module can be configured to operate with two, three or four pins. In 3-pin mode, SSx is not used. In 2-pin mode, neither SDOx nor SSx is used.

Figure 18-1 illustrates the block diagram of the SPIx module in Standard and Enhanced modes.

REGISTER 21-5: CxFIFO: ECANx FIFO STATUS REGISTER

U-0	U-0	R-0	R-0	R-0	R-0	R-0	R-0
—	—	FBP5	FBP4	FBP3	FBP2	FBP1	FBP0
bit 15							bit 8

U-0	U-0	R-0	R-0	R-0	R-0	R-0	R-0
—	—	FNRB5	FNRB4	FNRB3	FNRB2	FNRB1	FNRB0
bit 7							bit 0

Legend:

R = Readable bit

W = Writable bit

U = Unimplemented bit, read as '0'

-n = Value at POR

'1' = Bit is set

'0' = Bit is cleared

x = Bit is unknown

bit 15-14 **Unimplemented:** Read as '0'

bit 13-8 **FBP<5:0>:** FIFO Buffer Pointer bits

011111 = RB31 buffer

011110 = RB30 buffer

•
•
•

000001 = TRB1 buffer

000000 = TRB0 buffer

bit 7-6 **Unimplemented:** Read as '0'

bit 5-0 **FNRB<5:0>:** FIFO Next Read Buffer Pointer bits

011111 = RB31 buffer

011110 = RB30 buffer

•
•
•

000001 = TRB1 buffer

000000 = TRB0 buffer

22.2 CTMU Control Registers

REGISTER 22-1: CTMUCON1: CTMU CONTROL REGISTER 1

R/W-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
CTMUEN	—	CTMUSIDL	TGEN	EDGEN	EDGSEQEN	IDISSEN ⁽¹⁾	CTTRIG
bit 15							bit 8

U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
—	—	—	—	—	—	—	—
bit 7							bit 0

Legend:

R = Readable bit

W = Writable bit

U = Unimplemented bit, read as '0'

-n = Value at POR

'1' = Bit is set

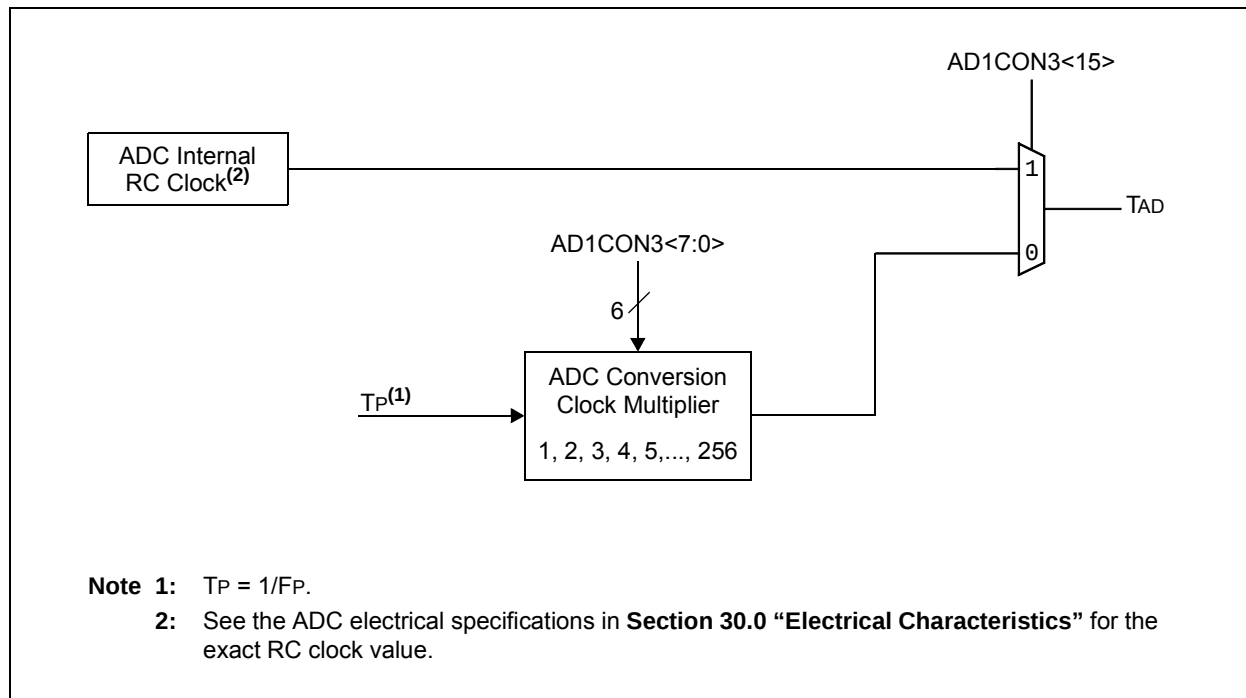
'0' = Bit is cleared

x = Bit is unknown

- bit 15 **CTMUEN:** CTMU Enable bit
 1 = Module is enabled
 0 = Module is disabled
- bit 14 **Unimplemented:** Read as '0'
- bit 13 **CTMUSIDL:** CTMU Stop in Idle Mode bit
 1 = Discontinues module operation when device enters Idle mode
 0 = Continues module operation in Idle mode
- bit 12 **TGEN:** Time Generation Enable bit
 1 = Enables edge delay generation
 0 = Disables edge delay generation
- bit 11 **EDGEN:** Edge Enable bit
 1 = Hardware modules are used to trigger edges (TMRx, CTEDx, etc.)
 0 = Software is used to trigger edges (manual set of EDGxSTAT)
- bit 10 **EDGSEQEN:** Edge Sequence Enable bit
 1 = Edge 1 event must occur before Edge 2 event can occur
 0 = No edge sequence is needed
- bit 9 **IDISSEN:** Analog Current Source Control bit⁽¹⁾
 1 = Analog current source output is grounded
 0 = Analog current source output is not grounded
- bit 8 **CTTRIG:** ADC Trigger Control bit
 1 = CTMU triggers ADC start of conversion
 0 = CTMU does not trigger ADC start of conversion
- bit 7-0 **Unimplemented:** Read as '0'

Note 1: The ADC module Sample-and-Hold capacitor is not automatically discharged between sample/conversion cycles. Software using the ADC as part of a capacitance measurement must discharge the ADC capacitor before conducting the measurement. The IDISSEN bit, when set to '1', performs this function. The ADC must be sampling while the IDISSEN bit is active to connect the discharge sink to the capacitor array.

FIGURE 23-2: ADC CONVERSION CLOCK PERIOD BLOCK DIAGRAM



REGISTER 23-3: AD1CON3: ADC1 CONTROL REGISTER 3

R/W-0	U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
ADRC	—	—	SAMC4 ⁽¹⁾	SAMC3 ⁽¹⁾	SAMC2 ⁽¹⁾	SAMC1 ⁽¹⁾	SAMC0 ⁽¹⁾
bit 15							bit 8

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
ADCS7 ⁽²⁾	ADCS6 ⁽²⁾	ADCS5 ⁽²⁾	ADCS4 ⁽²⁾	ADCS3 ⁽²⁾	ADCS2 ⁽²⁾	ADCS1 ⁽²⁾	ADCS0 ⁽²⁾
bit 7							bit 0

Legend:

R = Readable bit

W = Writable bit

U = Unimplemented bit, read as '0'

-n = Value at POR

'1' = Bit is set

'0' = Bit is cleared

x = Bit is unknown

bit 15 **ADRC:** ADC1 Conversion Clock Source bit

1 = ADC internal RC clock

0 = Clock derived from system clock

bit 14-13 **Unimplemented:** Read as '0'

bit 12-8 **SAMC<4:0>:** Auto-Sample Time bits⁽¹⁾

11111 = 31 TAD

•

•

•

00001 = 1 TAD

00000 = 0 TAD

bit 7-0 **ADCS<7:0>:** ADC1 Conversion Clock Select bits⁽²⁾

11111111 = $T_P \cdot (ADCS<7:0> + 1) = T_P \cdot 256 = T_{AD}$

•

•

•

00000010 = $T_P \cdot (ADCS<7:0> + 1) = T_P \cdot 3 = T_{AD}$

00000001 = $T_P \cdot (ADCS<7:0> + 1) = T_P \cdot 2 = T_{AD}$

00000000 = $T_P \cdot (ADCS<7:0> + 1) = T_P \cdot 1 = T_{AD}$

Note 1: This bit is only used if SSRC<2:0> (AD1CON1<7:5>) = 111 and SSRCG (AD1CON1<4>) = 0.

2: This bit is not used if ADRC (AD1CON3<15>) = 1.

REGISTER 23-6: AD1CHS0: ADC1 INPUT CHANNEL 0 SELECT REGISTER

R/W-0	U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
CH0NB	—	—	CH0SB4 ⁽¹⁾	CH0SB3 ⁽¹⁾	CH0SB2 ⁽¹⁾	CH0SB1 ⁽¹⁾	CH0SB0 ⁽¹⁾
bit 15							bit 8

R/W-0	U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
CH0NA	—	—	CH0SA4 ⁽¹⁾	CH0SA3 ⁽¹⁾	CH0SA2 ⁽¹⁾	CH0SA1 ⁽¹⁾	CH0SA0 ⁽¹⁾
bit 7							bit 0

Legend:

R = Readable bit W = Writable bit U = Unimplemented bit, read as '0'
 -n = Value at POR '1' = Bit is set '0' = Bit is cleared x = Bit is unknown

- bit 15 **CH0NB:** Channel 0 Negative Input Select for Sample MUXB bit
 1 = Channel 0 negative input is AN1⁽¹⁾
 0 = Channel 0 negative input is VREFL
- bit 14-13 **Unimplemented:** Read as '0'
- bit 12-8 **CH0SB<4:0>:** Channel 0 Positive Input Select for Sample MUXB bits⁽¹⁾
 11111 = Open; use this selection with CTMU capacitive and time measurement
 11110 = Channel 0 positive input is connected to the CTMU temperature measurement diode (CTMU TEMP)
 11101 = Reserved
 11100 = Reserved
 11011 = Reserved
 11010 = Channel 0 positive input is the output of OA3/AN6^(2,3)
 11001 = Channel 0 positive input is the output of OA2/AN0⁽²⁾
 11000 = Channel 0 positive input is the output of OA1/AN3⁽²⁾
 10111 = Reserved
 .
 .
 .
 10000 = Reserved
 01111 = Channel 0 positive input is AN15⁽³⁾
 01110 = Channel 0 positive input is AN14⁽³⁾
 01101 = Channel 0 positive input is AN13⁽³⁾
 .
 .
 .
 00010 = Channel 0 positive input is AN2⁽³⁾
 00001 = Channel 0 positive input is AN1⁽³⁾
 00000 = Channel 0 positive input is AN0⁽³⁾
- bit 7 **CH0NA:** Channel 0 Negative Input Select for Sample MUXA bit
 1 = Channel 0 negative input is AN1⁽¹⁾
 0 = Channel 0 negative input is VREFL
- bit 6-5 **Unimplemented:** Read as '0'

- Note 1:** AN0 through AN7 are repurposed when comparator and op amp functionality is enabled. See Figure 23-1 to determine how enabling a particular op amp or comparator affects selection choices for Channels 1, 2 and 3.
- 2:** The OAx input is used if the corresponding op amp is selected (OPMODE (CMxCON<10>) = 1); otherwise, the ANx input is used.
- 3:** See the “Pin Diagrams” section for the available analog channels for each device.

26.3 Programmable CRC Registers

REGISTER 26-1: CRCCON1: CRC CONTROL REGISTER 1

R/W-0	U-0	R/W-0	R-0	R-0	R-0	R-0	R-0
CRCEN	—	CSIDL	VWORD4	VWORD3	VWORD2	VWORD1	VWORD0
bit 15							bit 8

R-0	R-1	R/W-0	R/W-0	R/W-0	U-0	U-0	U-0
CRCFUL	CRCMPT	CRCISEL	CRCGO	LENDIAN	—	—	—
bit 7							bit 0

Legend:

R = Readable bit

W = Writable bit

U = Unimplemented bit, read as '0'

-n = Value at POR

'1' = Bit is set

'0' = Bit is cleared

x = Bit is unknown

- bit 15 **CRCEN:** CRC Enable bit
 1 = CRC module is enabled
 0 = CRC module is disabled; all state machines, pointers and CRCWDAT/CRCDAT are reset, other SFRs are not reset
- bit 14 **Unimplemented:** Read as '0'
- bit 13 **CSIDL:** CRC Stop in Idle Mode bit
 1 = Discontinues module operation when device enters Idle mode
 0 = Continues module operation in Idle mode
- bit 12-8 **VWORD<4:0>:** Pointer Value bits
 Indicates the number of valid words in the FIFO. Has a maximum value of 8 when PLEN<4:0> > 7 or 16 when PLEN<4:0> ≤ 7.
- bit 7 **CRCFUL:** CRC FIFO Full bit
 1 = FIFO is full
 0 = FIFO is not full
- bit 6 **CRCMPT:** CRC FIFO Empty Bit
 1 = FIFO is empty
 0 = FIFO is not empty
- bit 5 **CRCISEL:** CRC Interrupt Selection bit
 1 = Interrupt on FIFO is empty; final word of data is still shifting through CRC
 0 = Interrupt on shift is complete and CRCWDAT results are ready
- bit 4 **CRCGO:** Start CRC bit
 1 = Starts CRC serial shifter
 0 = CRC serial shifter is turned off
- bit 3 **LENDIAN:** Data Word Little-Endian Configuration bit
 1 = Data word is shifted into the CRC starting with the LSb (little endian)
 0 = Data word is shifted into the CRC starting with the MSb (big endian)
- bit 2-0 **Unimplemented:** Read as '0'

TABLE 30-61: ADC CONVERSION (10-BIT MODE) TIMING REQUIREMENTS

AC CHARACTERISTICS			Standard Operating Conditions: 3.0V to 3.6V (unless otherwise stated) ⁽¹⁾ Operating temperature -40°C ≤ TA ≤ +85°C for Industrial -40°C ≤ TA ≤ +125°C for Extended				
Param No.	Symbol	Characteristic	Min.	Typ.	Max.	Units	Conditions
Clock Parameters							
AD50	TAD	ADC Clock Period	76	—	—	ns	
AD51	tRC	ADC Internal RC Oscillator Period ⁽²⁾	—	250	—	ns	
Conversion Rate							
AD55	tCONV	Conversion Time	—	12 TAD	—	—	
AD56	FCNV	Throughput Rate	—	—	1.1	Msp/s	Using simultaneous sampling
AD57a	TSAMP	Sample Time when Sampling any ANx Input	2 TAD	—	—	—	
AD57b	TSAMP	Sample Time when Sampling the Op Amp Outputs (Configuration A and Configuration B) ^(4,5)	4 TAD	—	—	—	
Timing Parameters							
AD60	tPCS	Conversion Start from Sample Trigger ^(2,3)	2 TAD	—	3 TAD	—	Auto-convert trigger is not selected
AD61	tPSS	Sample Start from Setting Sample (SAMP) bit ^(2,3)	2 TAD	—	3 TAD	—	
AD62	tCSS	Conversion Completion to Sample Start (ASAM = 1) ^(2,3)	—	0.5 TAD	—	—	
AD63	tDPU	Time to Stabilize Analog Stage from ADC Off to ADC On ^(2,3)	—	—	20	μs	(Note 6)

Note 1: Device is functional at VBORMIN < VDD < VDDMIN, but will have degraded performance. Device functionality is tested, but not characterized. Analog modules (ADC, op amp/comparator and comparator voltage reference) may have degraded performance. Refer to Parameter BO10 in Table 30-13 for the minimum and maximum BOR values.

2: Parameters are characterized but not tested in manufacturing.

3: Because the sample caps will eventually lose charge, clock rates below 10 kHz may affect linearity performance, especially at elevated temperatures.

4: See Figure 25-6 for configuration information.

5: See Figure 25-7 for configuration information.

6: The parameter, tDPU, is the time required for the ADC module to stabilize at the appropriate level when the module is turned on (ADON (AD1CON1<15>) = 1). During this time, the ADC result is indeterminate.

TABLE 30-62: DMA MODULE TIMING REQUIREMENTS

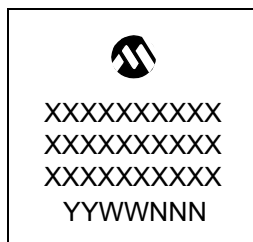
AC CHARACTERISTICS		Standard Operating Conditions: 3.0V to 3.6V (unless otherwise stated) Operating temperature -40°C ≤ TA ≤ +85°C for Industrial -40°C ≤ TA ≤ +125°C for Extended				
Param No.	Characteristic	Min.	Typ. ⁽¹⁾	Max.	Units	Conditions
DM1	DMA Byte/Word Transfer Latency	1 Tcy ⁽²⁾	—	—	ns	

Note 1: These parameters are characterized, but not tested in manufacturing.

2: Because DMA transfers use the CPU data bus, this time is dependent on other functions on the bus.

33.1 Package Marking Information (Continued)

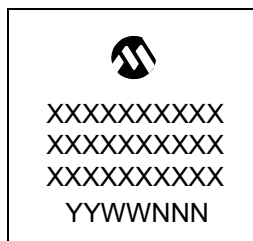
36-Lead VTLA (TLA)



Example



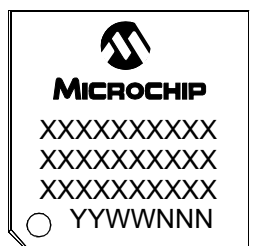
44-Lead VTLA (TLA)



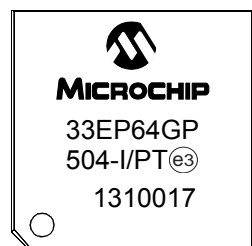
Example



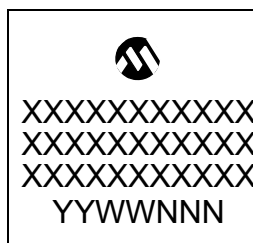
44-Lead TQFP



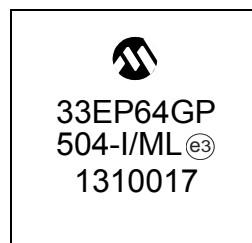
Example



44-Lead QFN (8x8x0.9 mm)

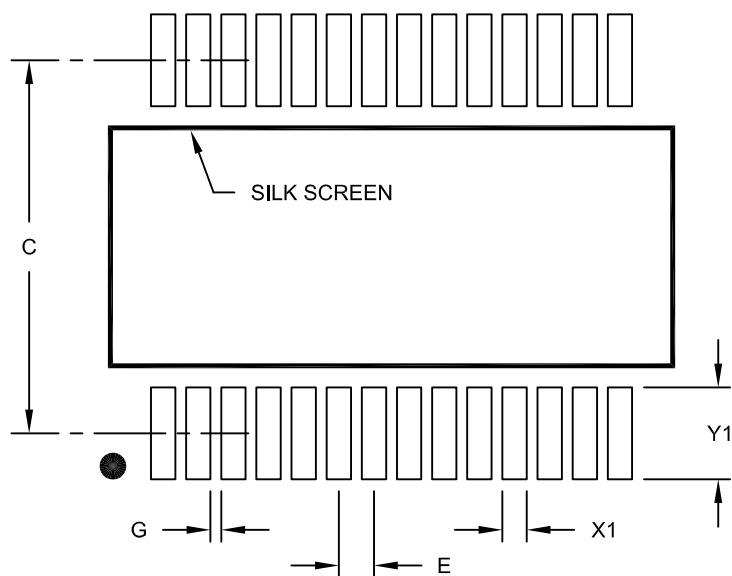


Example



28-Lead Plastic Shrink Small Outline (SS) - 5.30 mm Body [SSOP]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at <http://www.microchip.com/packaging>



RECOMMENDED LAND PATTERN

Units		MILLIMETERS		
Dimension	Limits	MIN	NOM	MAX
Contact Pitch	E	0.65 BSC		
Contact Pad Spacing	C	7.20		
Contact Pad Width (X28)	X1			0.45
Contact Pad Length (X28)	Y1			1.75
Distance Between Pads	G	0.20		

Notes:

1. Dimensioning and tolerancing per ASME Y14.5M

BSC: Basic Dimension. Theoretically exact value shown without tolerances.

Microchip Technology Drawing No. C04-2073A

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