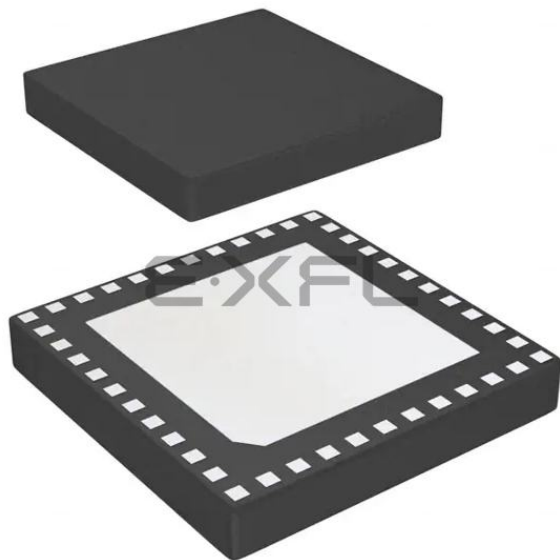




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Details

Product Status	Obsolete
Core Processor	PIC
Core Size	16-Bit
Speed	70 MIPS
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Peripherals	Brown-out Detect/Reset, DMA, Motor Control PWM, POR, PWM, WDT
Number of I/O	35
Program Memory Size	256KB (85.5K x 24)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	16K x 16
Voltage - Supply (Vcc/Vdd)	3V ~ 3.6V
Data Converters	A/D 9x10b/12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	44-VFTLA Exposed Pad
Supplier Device Package	44-VTLA (6x6)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/pic24ep256mc204-i-tl

3.7 CPU Control Registers

REGISTER 3-1: SR: CPU STATUS REGISTER

R/W-0	R/W-0	R/W-0	R/W-0	R/C-0	R/C-0	R-0	R/W-0
OA ⁽¹⁾	OB ⁽¹⁾	SA ^(1,4)	SB ^(1,4)	OAB ⁽¹⁾	SAB ⁽¹⁾	DA ⁽¹⁾	DC
bit 15							bit 8

R/W-0 ^(2,3)	R/W-0 ^(2,3)	R/W-0 ^(2,3)	R-0	R/W-0	R/W-0	R/W-0	R/W-0
IPL2	IPL1	IPL0	RA	N	OV	Z	C
bit 7							bit 0

Legend:	C = Clearable bit
R = Readable bit	W = Writable bit
-n = Value at POR	'1' = Bit is set
	U = Unimplemented bit, read as '0'
	'0' = Bit is cleared
	x = Bit is unknown

- bit 15 **OA:** Accumulator A Overflow Status bit⁽¹⁾
 1 = Accumulator A has overflowed
 0 = Accumulator A has not overflowed
- bit 14 **OB:** Accumulator B Overflow Status bit⁽¹⁾
 1 = Accumulator B has overflowed
 0 = Accumulator B has not overflowed
- bit 13 **SA:** Accumulator A Saturation 'Sticky' Status bit^(1,4)
 1 = Accumulator A is saturated or has been saturated at some time
 0 = Accumulator A is not saturated
- bit 12 **SB:** Accumulator B Saturation 'Sticky' Status bit^(1,4)
 1 = Accumulator B is saturated or has been saturated at some time
 0 = Accumulator B is not saturated
- bit 11 **OAB:** OA || OB Combined Accumulator Overflow Status bit⁽¹⁾
 1 = Accumulators A or B have overflowed
 0 = Neither Accumulators A or B have overflowed
- bit 10 **SAB:** SA || SB Combined Accumulator 'Sticky' Status bit⁽¹⁾
 1 = Accumulators A or B are saturated or have been saturated at some time
 0 = Neither Accumulators A or B are saturated
- bit 9 **DA:** D0 Loop Active bit⁽¹⁾
 1 = D0 loop is in progress
 0 = D0 loop is not in progress
- bit 8 **DC:** MCU ALU Half Carry/Borrow bit
 1 = A carry-out from the 4th low-order bit (for byte-sized data) or 8th low-order bit (for word-sized data) of the result occurred
 0 = No carry-out from the 4th low-order bit (for byte-sized data) or 8th low-order bit (for word-sized data) of the result occurred

- Note 1:** This bit is available on dsPIC33EPXXXMC20X/50X and dsPIC33EPXXXGP50X devices only.
- Note 2:** The IPL<2:0> bits are concatenated with the IPL<3> bit (CORCON<3>) to form the CPU Interrupt Priority Level. The value in parentheses indicates the IPL, if IPL<3> = 1. User interrupts are disabled when IPL<3> = 1.
- Note 3:** The IPL<2:0> Status bits are read-only when the NSTDIS bit (INTCON1<15>) = 1.
- Note 4:** A data write to the SR register can modify the SA and SB bits by either a data write to SA and SB or by clearing the SAB bit. To avoid a possible SA or SB bit write race condition, the SA and SB bits should not be modified using bit operations.

FIGURE 4-2: PROGRAM MEMORY MAP FOR dsPIC33EP64GP50X, dsPIC33EP64MC20X/50X AND PIC24EP64GP/MC20X DEVICES

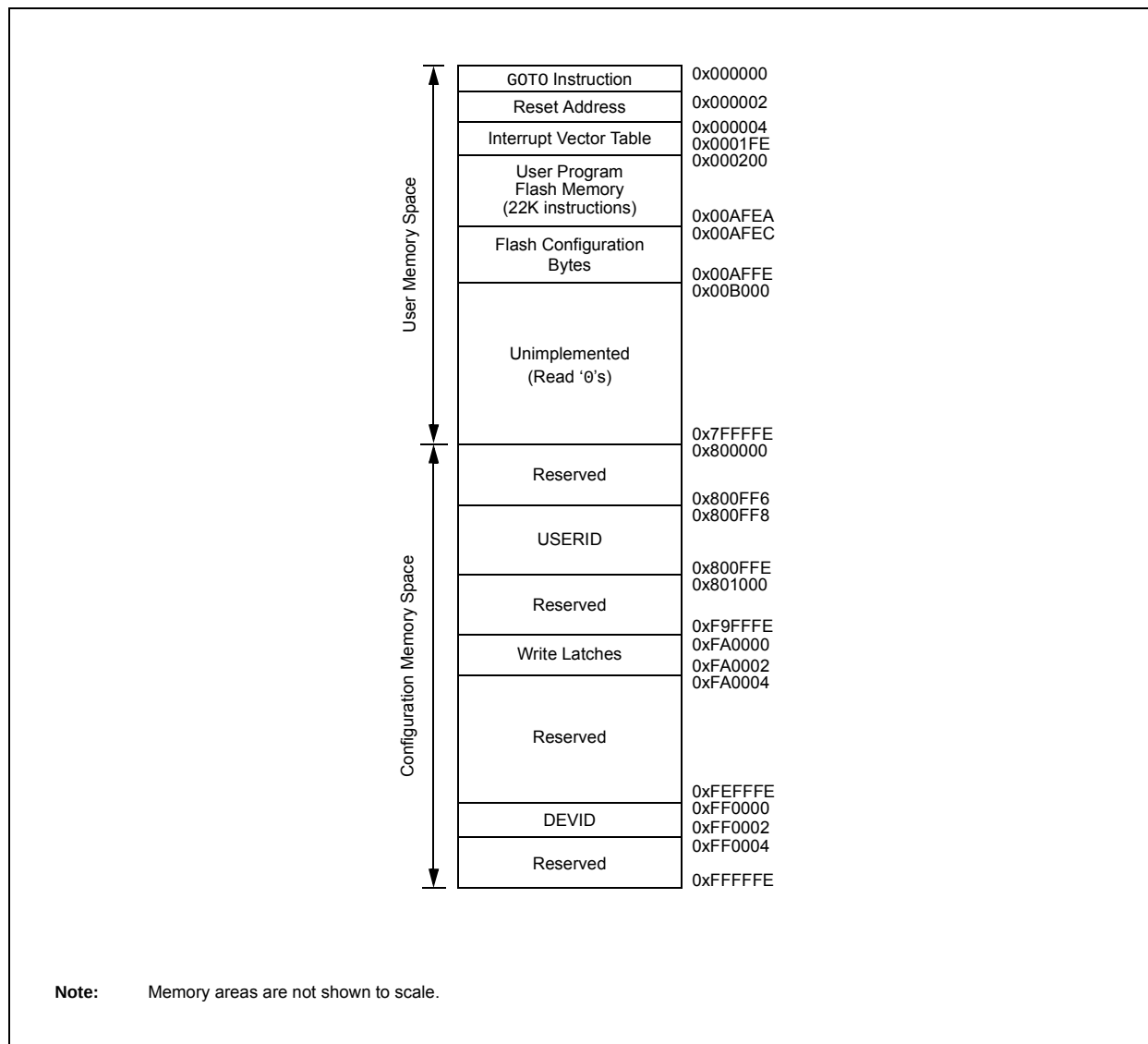


TABLE 4-5: INTERRUPT CONTROLLER REGISTER MAP FOR dsPIC33EPXXXGP50X DEVICES ONLY

File Name	Addr.	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	All Resets
IFS0	0800	—	DMA1IF	AD1IF	U1TXIF	U1RXIF	SPI1IF	SPI1EIF	T3IF	T2IF	OC2IF	IC2IF	DMA0IF	T1IF	OC1IF	IC1IF	INT0IF	0000
IFS1	0802	U2TXIF	U2RXIF	INT2IF	T5IF	T4IF	OC4IF	OC3IF	DMA2IF	—	—	—	INT1IF	CNIF	CMIF	MI2C1IF	SI2C1IF	0000
IFS2	0804	—	—	—	—	—	—	—	—	—	IC4IF	IC3IF	DMA3IF	C1IF	C1RXIF	SPI2IF	SPI2EIF	0000
IFS3	0806	—	—	—	—	—	—	—	—	—	—	—	—	—	MI2C2IF	SI2C2IF	—	0000
IFS4	0808	—	—	CTMUIF	—	—	—	—	—	—	C1TXIF	—	—	CRCIF	U2EIF	U1EIF	—	0000
IFS6	080C	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	PWM3IF	0000
IFS8	0810	JTAGIF	ICDIF	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
IFS9	0812	—	—	—	—	—	—	—	—	—	PTG3IF	PTG2IF	PTG1IF	PTG0IF	PTGWDTIF	PTGSTIEIF	—	0000
IEC0	0820	—	DMA1IE	AD1IE	U1TXIE	U1RXIE	SPI1IE	SPI1EIE	T3IE	T2IE	OC2IE	IC2IE	DMA0IE	T1IE	OC1IE	IC1IE	INT0IE	0000
IEC1	0822	U2TXIE	U2RXIE	INT2IE	T5IE	T4IE	OC4IE	OC3IE	DMA2IE	—	—	—	INT1IE	CNIE	CMIE	MI2C1IE	SI2C1IE	0000
IEC2	0824	—	—	—	—	—	—	—	—	—	IC4IE	IC3IE	DMA3IE	C1IE	C1RXIE	SPI2IE	SPI2EIE	0000
IEC3	0826	—	—	—	—	—	—	—	—	—	—	—	—	—	MI2C2IE	SI2C2IE	—	0000
IEC4	0828	—	—	CTMUIE	—	—	—	—	—	—	C1TXIE	—	—	CRCIE	U2EIE	U1EIE	—	0000
IEC8	0830	JTAGIE	ICDIE	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
IEC9	0832	—	—	—	—	—	—	—	—	—	PTG3IE	PTG2IE	PTG1IE	PTG0IE	PTGWDTIE	PTGSTIEIE	—	0000
IPC0	0840	—	T1IP<2:0>			—	OC1IP<2:0>			—	IC1IP<2:0>			—	INT0IP<2:0>			4444
IPC1	0842	—	T2IP<2:0>			—	OC2IP<2:0>			—	IC2IP<2:0>			—	DMA0IP<2:0>			4444
IPC2	0844	—	U1RXIP<2:0>			—	SPI1IP<2:0>			—	SPI1EIP<2:0>			—	T3IP<2:0>			4444
IPC3	0846	—	—	—	—	—	DMA1IP<2:0>			—	AD1IP<2:0>			—	U1TXIP<2:0>			0444
IPC4	0848	—	CNIP<2:0>			—	CMIP<2:0>			—	MI2C1IP<2:0>			—	SI2C1IP<2:0>			4444
IPC5	084A	—	—	—	—	—	—	—	—	—	—	—	—	—	INT1IP<2:0>			0004
IPC6	084C	—	T4IP<2:0>			—	OC4IP<2:0>			—	OC3IP<2:0>			—	DMA2IP<2:0>			4444
IPC7	084E	—	U2TXIP<2:0>			—	U2RXIP<2:0>			—	INT2IP<2:0>			—	T5IP<2:0>			4444
IPC8	0850	—	C1IP<2:0>			—	C1RXIP<2:0>			—	SPI2IP<2:0>			—	SPI2EIP<2:0>			4444
IPC9	0852	—	—	—	—	—	IC4IP<2:0>			—	IC3IP<2:0>			—	DMA3IP<2:0>			0444
IPC11	0856	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
IPC12	0858	—	—	—	—	—	MI2C2IP<2:0>			—	SI2C2IP<2:0>			—	—	—	—	0440
IPC16	0860	—	CRCIP<2:0>			—	U2EIP<2:0>			—	U1EIP<2:0>			—	—	—	—	4440
IPC17	0862	—	—	—	—	—	C1TXIP<2:0>			—	—	—	—	—	—	—	—	0400
IPC19	0866	—	—	—	—	—	—	—	—	—	CTMUIP<2:0>			—	—	—	—	0040
IPC35	0886	—	JTAGIP<2:0>			—	ICDIP<2:0>			—	—	—	—	—	—	—	—	4400
IPC36	0888	—	PTG0IP<2:0>			—	PTGWDIP<2:0>			—	PTGSTIEIP<2:0>			—	—	—	—	4440
IPC37	088A	—	—	—	—	—	PTG3IP<2:0>			—	PTG2IP<2:0>			—	PTG1IP<2:0>			0444

Legend: — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

TABLE 4-11: PTG REGISTER MAP

File Name	Addr.	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	All Resets
PTGCST	0AC0	PTGEN	—	PTGSIDL	PTGTOGL	—	PTGSWT	PTGSSEN	PTGIVIS	PTGSTRT	PTGWTO	—	—	—	—	PTGITM<1:0>		0000
PTGCON	0AC2	PTGCLK<2:0>			PTGDIV<4:0>					PTGPWD<3:0>				—	PTGWDT<2:0>			0000
PTGBTE	0AC4	ADCTS<4:1>				IC4TSS	IC3TSS	IC2TSS	IC1TSS	OC4CS	OC3CS	OC2CS	OC1CS	OC4TSS	OC3TSS	OC2TSS	OC1TSS	0000
PTGHOLD	0AC6	PTGHOLD<15:0>																0000
PTGT0LIM	0AC8	PTGT0LIM<15:0>																0000
PTGT1LIM	0ACA	PTGT1LIM<15:0>																0000
PTGSDLIM	0ACC	PTGSDLIM<15:0>																0000
PTGC0LIM	0ACE	PTGC0LIM<15:0>																0000
PTGC1LIM	0AD0	PTGC1LIM<15:0>																0000
PTGADJ	0AD2	PTGADJ<15:0>																0000
PTGL0	0AD4	PTGL0<15:0>																0000
PTGQPTR	0AD6	—	—	—	—	—	—	—	—	—	—	—	PTGQPTR<4:0>					0000
PTGQUE0	0AD8	STEP1<7:0>								STEP0<7:0>								0000
PTGQUE1	0ADA	STEP3<7:0>								STEP2<7:0>								0000
PTGQUE2	0ADC	STEP5<7:0>								STEP4<7:0>								0000
PTGQUE3	0ADE	STEP7<7:0>								STEP6<7:0>								0000
PTGQUE4	0AE0	STEP9<7:0>								STEP8<7:0>								0000
PTGQUE5	0AE2	STEP11<7:0>								STEP10<7:0>								0000
PTGQUE6	0AE4	STEP13<7:0>								STEP12<7:0>								0000
PTGQUE7	0AE6	STEP15<7:0>								STEP14<7:0>								0000

Legend: — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

TABLE 4-16: QE1 REGISTER MAP FOR dsPIC33EPXXXMC20X/50X AND PIC24EPXXXMC20X DEVICES ONLY

File Name	Addr.	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	All Resets
QE1CON	01C0	QE1EN	—	QE1SIDL	PIMOD<2:0>			IMV<1:0>		—	INTDIV<2:0>			CNTPOL	GATEN	CCM<1:0>		0000
QE1IOC	01C2	QCAPEN	FLTREN	QFDIV<2:0>			OUTFNC<1:0>		SWPAB	HOMPOL	IDXPOL	QEBPOL	QEAPOL	HOME	INDEX	QEB	QEA	000x
QE1STAT	01C4	—	—	PCHEQIRQ	PCHEQIEN	PCLEQIRQ	PCLEQIEN	POSOVIRQ	POSOVIEN	PCIIRQ	PCIEN	VELOVIRQ	VELOVIEN	HOMIRQ	HOMIEN	IDXIRQ	IDXIEN	0000
POS1CNTL	01C6	POSCNT<15:0>																0000
POS1CNTH	01C8	POSCNT<31:16>																0000
POS1HLD	01CA	POSHLD<15:0>																0000
VEL1CNT	01CC	VELCNT<15:0>																0000
INT1TMRL	01CE	INTTMR<15:0>																0000
INT1TMRH	01D0	INTTMR<31:16>																0000
INT1HLDL	01D2	INTHLD<15:0>																0000
INT1HLDH	01D4	INTHLD<31:16>																0000
INDX1CNTL	01D6	INDXCNT<15:0>																0000
INDX1CNTH	01D8	INDXCNT<31:16>																0000
INDX1HLD	01DA	INDXHLD<15:0>																0000
QE1GECL	01DC	QEIGEC<15:0>																0000
QE1ICL	01DC	QEIIC<15:0>																0000
QE1GECH	01DE	QEIGEC<31:16>																0000
QE1ICH	01DE	QEIIC<31:16>																0000
QE1LECL	01E0	QEILEC<15:0>																0000
QE1LECH	01E2	QEILEC<31:16>																0000

Legend: x = unknown value on Reset, — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

TABLE 4-27: PERIPHERAL PIN SELECT OUTPUT REGISTER MAP FOR dsPIC33EPXXXGP/MC204/504 AND PIC24EPXXXGP/MC204 DEVICES ONLY

File Name	Addr.	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	All Resets
RPOR0	0680	—	—	RP35R<5:0>						—	—	RP20R<5:0>						0000
RPOR1	0682	—	—	RP37R<5:0>						—	—	RP36R<5:0>						0000
RPOR2	0684	—	—	RP39R<5:0>						—	—	RP38R<5:0>						0000
RPOR3	0686	—	—	RP41R<5:0>						—	—	RP40R<5:0>						0000
RPOR4	0688	—	—	RP43R<5:0>						—	—	RP42R<5:0>						0000
RPOR5	068A	—	—	RP55R<5:0>						—	—	RP54R<5:0>						0000
RPOR6	068C	—	—	RP57R<5:0>						—	—	RP56R<5:0>						0000

Legend: — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

TABLE 4-28: PERIPHERAL PIN SELECT OUTPUT REGISTER MAP FOR dsPIC33EPXXXGP/MC206/506 AND PIC24EPXXXGP/MC206 DEVICES ONLY

File Name	Addr.	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	All Resets
RPOR0	0680	—	—	RP35R<5:0>						—	—	RP20R<5:0>						0000
RPOR1	0682	—	—	RP37R<5:0>						—	—	RP36R<5:0>						0000
RPOR2	0684	—	—	RP39R<5:0>						—	—	RP38R<5:0>						0000
RPOR3	0686	—	—	RP41R<5:0>						—	—	RP40R<5:0>						0000
RPOR4	0688	—	—	RP43R<5:0>						—	—	RP42R<5:0>						0000
RPOR5	068A	—	—	RP55R<5:0>						—	—	RP54R<5:0>						0000
RPOR6	068C	—	—	RP57R<5:0>						—	—	RP56R<5:0>						0000
RPOR7	068E	—	—	RP97R<5:0>						—	—	—	—	—	—	—	—	0000
RPOR8	0690	—	—	RP118R<5:0>						—	—	—	—	—	—	—	—	0000
RPOR9	0692	—	—	—	—	—	—	—	—	—	—	RP120R<5:0>						0000

Legend: — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

9.3 Oscillator Control Registers

REGISTER 9-1: OSCCON: OSCILLATOR CONTROL REGISTER⁽¹⁾

U-0	R-0	R-0	R-0	U-0	R/W-y	R/W-y	R/W-y
—	COSC2	COSC1	COSC0	—	NOSC2 ⁽²⁾	NOSC1 ⁽²⁾	NOSC0 ⁽²⁾
bit 15				bit 8			

R/W-0	R/W-0	R-0	U-0	R/W-0	U-0	U-0	R/W-0
CLKLOCK	IOLOCK	LOCK	—	CF ⁽³⁾	—	—	OSWEN
bit 7				bit 0			

Legend:	y = Value set from Configuration bits on POR		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15 **Unimplemented:** Read as '0'

bit 14-12 **COSC<2:0>:** Current Oscillator Selection bits (read-only)

- 111 = Fast RC Oscillator (FRC) with Divide-by-n
- 110 = Fast RC Oscillator (FRC) with Divide-by-16
- 101 = Low-Power RC Oscillator (LPRC)
- 100 = Reserved
- 011 = Primary Oscillator (XT, HS, EC) with PLL
- 010 = Primary Oscillator (XT, HS, EC)
- 001 = Fast RC Oscillator (FRC) with Divide-by-N and PLL (FRCPLL)
- 000 = Fast RC Oscillator (FRC)

bit 11 **Unimplemented:** Read as '0'

bit 10-8 **NOSC<2:0>:** New Oscillator Selection bits⁽²⁾

- 111 = Fast RC Oscillator (FRC) with Divide-by-n
- 110 = Fast RC Oscillator (FRC) with Divide-by-16
- 101 = Low-Power RC Oscillator (LPRC)
- 100 = Reserved
- 011 = Primary Oscillator (XT, HS, EC) with PLL
- 010 = Primary Oscillator (XT, HS, EC)
- 001 = Fast RC Oscillator (FRC) with Divide-by-N and PLL (FRCPLL)
- 000 = Fast RC Oscillator (FRC)

bit 7 **CLKLOCK:** Clock Lock Enable bit

- 1 = If (FCKSM0 = 1), then clock and PLL configurations are locked; if (FCKSM0 = 0), then clock and PLL configurations may be modified
- 0 = Clock and PLL selections are not locked, configurations may be modified

bit 6 **IOLOCK:** I/O Lock Enable bit

- 1 = I/O lock is active
- 0 = I/O lock is not active

bit 5 **LOCK:** PLL Lock Status bit (read-only)

- 1 = Indicates that PLL is in lock or PLL start-up timer is satisfied
- 0 = Indicates that PLL is out of lock, start-up timer is in progress or PLL is disabled

Note 1: Writes to this register require an unlock sequence. Refer to “**Oscillator**” (DS70580) in the “*dsPIC33/PIC24 Family Reference Manual*” (available from the Microchip web site) for details.

2: Direct clock switches between any primary oscillator mode with PLL and FRCPLL mode are not permitted. This applies to clock switches in either direction. In these instances, the application must switch to FRC mode as a transitional clock source between the two PLL modes.

3: This bit should only be cleared in software. Setting the bit in software (= 1) will have the same effect as an actual oscillator failure and trigger an oscillator failure trap.

TABLE 11-1: SELECTABLE INPUT SOURCES (MAPS INPUT TO FUNCTION)

Input Name ⁽¹⁾	Function Name	Register	Configuration Bits
External Interrupt 1	INT1	RPINR0	INT1R<6:0>
External Interrupt 2	INT2	RPINR1	INT2R<6:0>
Timer2 External Clock	T2CK	RPINR3	T2CKR<6:0>
Input Capture 1	IC1	RPINR7	IC1R<6:0>
Input Capture 2	IC2	RPINR7	IC2R<6:0>
Input Capture 3	IC3	RPINR8	IC3R<6:0>
Input Capture 4	IC4	RPINR8	IC4R<6:0>
Output Compare Fault A	OCFA	RPINR11	OCFAR<6:0>
PWM Fault 1 ⁽³⁾	FLT1	RPINR12	FLT1R<6:0>
PWM Fault 2 ⁽³⁾	FLT2	RPINR12	FLT2R<6:0>
QE11 Phase A ⁽³⁾	QEA1	RPINR14	QEA1R<6:0>
QE11 Phase B ⁽³⁾	QEB1	RPINR14	QEB1R<6:0>
QE11 Index ⁽³⁾	INDX1	RPINR15	INDX1R<6:0>
QE11 Home ⁽³⁾	HOME1	RPINR15	HOM1R<6:0>
UART1 Receive	U1RX	RPINR18	U1RXR<6:0>
UART2 Receive	U2RX	RPINR19	U2RXR<6:0>
SPI2 Data Input	SDI2	RPINR22	SDI2R<6:0>
SPI2 Clock Input	SCK2	RPINR22	SCK2R<6:0>
SPI2 Slave Select	SS2	RPINR23	SS2R<6:0>
CAN1 Receive ⁽²⁾	C1RX	RPINR26	C1RXR<6:0>
PWM Sync Input 1 ⁽³⁾	SYNCI1	RPINR37	SYNCI1R<6:0>
PWM Dead-Time Compensation 1 ⁽³⁾	DTCMP1	RPINR38	DTCMP1R<6:0>
PWM Dead-Time Compensation 2 ⁽³⁾	DTCMP2	RPINR39	DTCMP2R<6:0>
PWM Dead-Time Compensation 3 ⁽³⁾	DTCMP3	RPINR39	DTCMP3R<6:0>

Note 1: Unless otherwise noted, all inputs use the Schmitt Trigger input buffers.

2: This input source is available on dsPIC33EPXXXGP/MC50X devices only.

3: This input source is available on dsPIC33EPXXXMC20X/50X and PIC24EPXXXMC20X devices only.

REGISTER 11-6: RPINR11: PERIPHERAL PIN SELECT INPUT REGISTER 11

U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
—	—	—	—	—	—	—	—
bit 15							bit 8

U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
—	OCFAR<6:0>						
bit 7							bit 0

Legend:

R = Readable bit

W = Writable bit

U = Unimplemented bit, read as '0'

-n = Value at POR

'1' = Bit is set

'0' = Bit is cleared

x = Bit is unknown

bit 15-7 **Unimplemented:** Read as '0'bit 6-0 **OCFAR<6:0>:** Assign Output Compare Fault A (OCFA) to the Corresponding RPn Pin bits
(see Table 11-2 for input pin selection numbers)

1111001 = Input tied to RPI121

.

.

.

0000001 = Input tied to CMP1

0000000 = Input tied to Vss

REGISTER 11-13: RPINR23: PERIPHERAL PIN SELECT INPUT REGISTER 23

U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
—	—	—	—	—	—	—	—
bit 15							bit 8

U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
—	SS2R<6:0>						
bit 7							bit 0

Legend:

R = Readable bit

W = Writable bit

U = Unimplemented bit, read as '0'

-n = Value at POR

'1' = Bit is set

'0' = Bit is cleared

x = Bit is unknown

bit 15-7 **Unimplemented:** Read as '0'

bit 6-0 **SS2R<6:0>:** Assign SPI2 Slave Select ($\overline{SS2}$) to the Corresponding RPn Pin bits (see Table 11-2 for input pin selection numbers)

1111001 = Input tied to RPI121

.

.

.

0000001 = Input tied to CMP1

0000000 = Input tied to Vss

**REGISTER 11-14: RPINR26: PERIPHERAL PIN SELECT INPUT REGISTER 26
(dsPIC33EPXXXGP/MC50X DEVICES ONLY)**

U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
—	—	—	—	—	—	—	—
bit 15							bit 8

U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
—	C1RXR<6:0>						
bit 7							bit 0

Legend:

R = Readable bit

W = Writable bit

U = Unimplemented bit, read as '0'

-n = Value at POR

'1' = Bit is set

'0' = Bit is cleared

x = Bit is unknown

bit 15-7 **Unimplemented:** Read as '0'

bit 6-0 **C1RXR<6:0>:** Assign CAN1 RX Input (CRX1) to the Corresponding RPn Pin bits (see Table 11-2 for input pin selection numbers)

1111001 = Input tied to RPI121

.

.

.

0000001 = Input tied to CMP1

0000000 = Input tied to Vss

REGISTER 21-19: CxFMSKSEL2: ECANx FILTER 15-8 MASK SELECTION REGISTER 2

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
F15MSK<1:0>		F14MSK<1:0>		F13MSK<1:0>		F12MSK<1:0>	
bit 15							bit 8

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
F11MSK<1:0>		F10MSK<1:0>		F9MSK<1:0>		F8MSK<1:0>	
bit 7							bit 0

Legend:

R = Readable bit

W = Writable bit

U = Unimplemented bit, read as '0'

-n = Value at POR

'1' = Bit is set

'0' = Bit is cleared

x = Bit is unknown

bit 15-14 **F15MSK<1:0>**: Mask Source for Filter 15 bits

11 = Reserved

10 = Acceptance Mask 2 registers contain mask

01 = Acceptance Mask 1 registers contain mask

00 = Acceptance Mask 0 registers contain mask

bit 13-12 **F14MSK<1:0>**: Mask Source for Filter 14 bits (same values as bits<15:14>)bit 11-10 **F13MSK<1:0>**: Mask Source for Filter 13 bits (same values as bits<15:14>)bit 9-8 **F12MSK<1:0>**: Mask Source for Filter 12 bits (same values as bits<15:14>)bit 7-6 **F11MSK<1:0>**: Mask Source for Filter 11 bits (same values as bits<15:14>)bit 5-4 **F10MSK<1:0>**: Mask Source for Filter 10 bits (same values as bits<15:14>)bit 3-2 **F9MSK<1:0>**: Mask Source for Filter 9 bits (same values as bits<15:14>)bit 1-0 **F8MSK<1:0>**: Mask Source for Filter 8 bits (same values as bits<15:14>)

22.0 CHARGE TIME MEASUREMENT UNIT (CTMU)

Note 1: This data sheet summarizes the features of the dsPIC33EPXXXGP50X, dsPIC33EPXXXMC20X/50X and PIC24EPXXXGP/MC20X family of devices. It is not intended to be a comprehensive reference source. To complement the information in this data sheet, refer to “**Charge Time Measurement Unit (CTMU)**” (DS70661) in the “*dsPIC33/PIC24 Family Reference Manual*”, which is available on the Microchip web site (www.microchip.com).

2: Some registers and associated bits described in this section may not be available on all devices. Refer to **Section 4.0 “Memory Organization”** in this data sheet for device-specific register and bit information.

The Charge Time Measurement Unit is a flexible analog module that provides accurate differential time measurement between pulse sources, as well as asynchronous pulse generation. Its key features include:

- Four Edge Input Trigger Sources
- Polarity Control for Each Edge Source
- Control of Edge Sequence
- Control of Response to Edges
- Precise Time Measurement Resolution of 1 ns
- Accurate Current Source Suitable for Capacitive Measurement
- On-Chip Temperature Measurement using a Built-in Diode

Together with other on-chip analog modules, the CTMU can be used to precisely measure time, measure capacitance, measure relative changes in capacitance or generate output pulses that are independent of the system clock.

The CTMU module is ideal for interfacing with capacitive-based sensors. The CTMU is controlled through three registers: CTMUCON1, CTMUCON2 and CTMUICON. CTMUCON1 and CTMUCON2 enable the module and control edge source selection, edge source polarity selection and edge sequencing. The CTMUICON register controls the selection and trim of the current source.

REGISTER 25-3: CM4CON: COMPARATOR 4 CONTROL REGISTER

R/W-0	R/W-0	R/W-0	U-0	U-0	U-0	R/W-0	R/W-0
CON	COE	CPOL	—	—	—	CEVT	COUT
bit 15						bit 8	

R/W-0	R/W-0	U-0	R/W-0	U-0	U-0	R/W-0	R/W-0
EVPOL1	EVPOL0	—	CREF ⁽¹⁾	—	—	CCH1 ⁽¹⁾	CCH0 ⁽¹⁾
bit 7						bit 0	

Legend:

R = Readable bit

W = Writable bit

U = Unimplemented bit, read as '0'

-n = Value at POR

'1' = Bit is set

'0' = Bit is cleared

x = Bit is unknown

- bit 15 **CON:** Comparator Enable bit
1 = Comparator is enabled
0 = Comparator is disabled
- bit 14 **COE:** Comparator Output Enable bit
1 = Comparator output is present on the CxOUT pin
0 = Comparator output is internal only
- bit 13 **CPOL:** Comparator Output Polarity Select bit
1 = Comparator output is inverted
0 = Comparator output is not inverted
- bit 12-10 **Unimplemented:** Read as '0'
- bit 9 **CEVT:** Comparator Event bit
1 = Comparator event according to EVPOL<1:0> settings occurred; disables future triggers and interrupts until the bit is cleared
0 = Comparator event did not occur
- bit 8 **COUT:** Comparator Output bit
When CPOL = 0 (non-inverted polarity):
1 = VIN+ > VIN-
0 = VIN+ < VIN-
When CPOL = 1 (inverted polarity):
1 = VIN+ < VIN-
0 = VIN+ > VIN-
- bit 7-6 **EVPOL<1:0>:** Trigger/Event/Interrupt Polarity Select bits
11 = Trigger/event/interrupt generated on any change of the comparator output (while CEVT = 0)
10 = Trigger/event/interrupt generated only on high-to-low transition of the polarity selected comparator output (while CEVT = 0)
 If CPOL = 1 (inverted polarity):
 Low-to-high transition of the comparator output.
 If CPOL = 0 (non-inverted polarity):
 High-to-low transition of the comparator output.
01 = Trigger/event/interrupt generated only on low-to-high transition of the polarity selected comparator output (while CEVT = 0)
 If CPOL = 1 (inverted polarity):
 High-to-low transition of the comparator output.
 If CPOL = 0 (non-inverted polarity):
 Low-to-high transition of the comparator output.
00 = Trigger/event/interrupt generation is disabled

Note 1: Inputs that are selected and not available will be tied to Vss. See the “Pin Diagrams” section for available inputs for each package.

27.2 User ID Words

dsPIC33EPXXXGP50X, dsPIC33EPXXXMC20X/50X and PIC24EPXXXGP/MC20X devices contain four User ID Words, located at addresses, 0x800FF8 through 0x800FFE. The User ID Words can be used for storing product information such as serial numbers, system manufacturing dates, manufacturing lot numbers and other application-specific information.

The User ID Words register map is shown in Table 27-3.

TABLE 27-3: USER ID WORDS REGISTER MAP

File Name	Address	Bits 23-16	Bits 15-0
FUID0	0x800FF8	—	UID0
FUID1	0x800FFA	—	UID1
FUID2	0x800FFC	—	UID2
FUID3	0x800FFE	—	UID3

Legend: — = unimplemented, read as '1'.

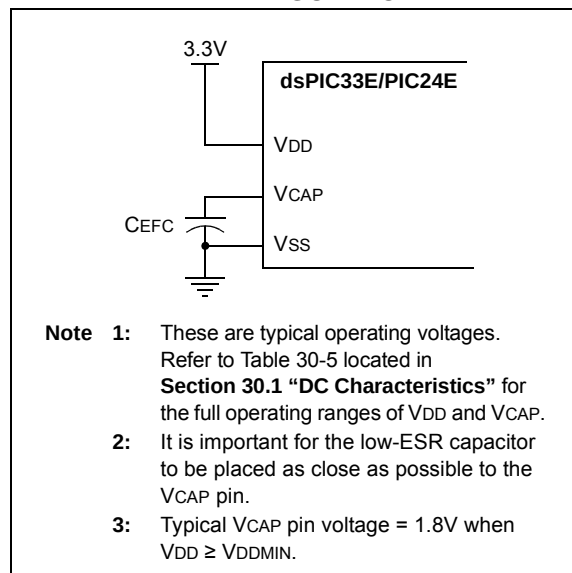
27.3 On-Chip Voltage Regulator

All of the dsPIC33EPXXXGP50X, dsPIC33EPXXXMC20X/50X and PIC24EPXXXGP/MC20X devices power their core digital logic at a nominal 1.8V. This can create a conflict for designs that are required to operate at a higher typical voltage, such as 3.3V. To simplify system design, all devices in the dsPIC33EPXXXGP50X, dsPIC33EPXXXMC20X/50X and PIC24EPXXXGP/MC20X family incorporate an on-chip regulator that allows the device to run its core logic from VDD.

The regulator provides power to the core from the other VDD pins. A low-ESR (less than 1 Ohm) capacitor (such as tantalum or ceramic) must be connected to the VCAP pin (Figure 27-1). This helps to maintain the stability of the regulator. The recommended value for the filter capacitor is provided in Table 30-5 located in Section 30.0 "Electrical Characteristics".

Note: It is important for the low-ESR capacitor to be placed as close as possible to the VCAP pin.

FIGURE 27-1: CONNECTIONS FOR THE ON-CHIP VOLTAGE REGULATOR^(1,2,3)



27.4 Brown-out Reset (BOR)

The Brown-out Reset (BOR) module is based on an internal voltage reference circuit that monitors the regulated supply voltage, VCAP. The main purpose of the BOR module is to generate a device Reset when a brown-out condition occurs. Brown-out conditions are generally caused by glitches on the AC mains (for example, missing portions of the AC cycle waveform due to bad power transmission lines or voltage sags due to excessive current draw when a large inductive load is turned on).

A BOR generates a Reset pulse, which resets the device. The BOR selects the clock source, based on the device Configuration bit values (FNOSC<2:0> and POSCMD<1:0>).

If an oscillator mode is selected, the BOR activates the Oscillator Start-up Timer (OST). The system clock is held until OST expires. If the PLL is used, the clock is held until the LOCK bit (OSCCON<5>) is '1'.

Concurrently, the PWRT Time-out (TPWRT) is applied before the internal Reset is released. If TPWRT = 0 and a crystal oscillator is being used, then a nominal delay of TFSCM is applied. The total delay in this case is TFSCM. Refer to Parameter SY35 in Table 30-22 of Section 30.0 "Electrical Characteristics" for specific TFSCM values.

The BOR status bit (RCON<1>) is set to indicate that a BOR has occurred. The BOR circuit continues to operate while in Sleep or Idle modes and resets the device should VDD fall below the BOR threshold voltage.

TABLE 30-4: DC TEMPERATURE AND VOLTAGE SPECIFICATIONS

DC CHARACTERISTICS			Standard Operating Conditions (see Note 1): 3.0V to 3.6V (unless otherwise stated) Operating temperature -40°C ≤ TA ≤ +85°C for Industrial -40°C ≤ TA ≤ +125°C for Extended				
Param No.	Symbol	Characteristic	Min.	Typ.	Max.	Units	Conditions
Operating Voltage							
DC10	VDD	Supply Voltage	3.0	—	3.6	V	
DC16	VPOR	VDD Start Voltage to Ensure Internal Power-on Reset Signal	—	—	VSS	V	
DC17	SVDD	VDD Rise Rate to Ensure Internal Power-on Reset Signal	0.03	—	—	V/ms	0V-1V in 100 ms

Note 1: Device is functional at VBORMIN < VDD < VDDMIN. Analog modules (ADC, op amp/comparator and comparator voltage reference) may have degraded performance. Device functionality is tested but not characterized. Refer to Parameter BO10 in Table 30-13 for the minimum and maximum BOR values.

TABLE 30-5: FILTER CAPACITOR (CEFC) SPECIFICATIONS

Standard Operating Conditions (unless otherwise stated): Operating temperature -40°C ≤ TA ≤ +85°C for Industrial -40°C ≤ TA ≤ +125°C for Extended							
Param No.	Symbol	Characteristics	Min.	Typ.	Max.	Units	Comments
	CEFC	External Filter Capacitor Value ⁽¹⁾	4.7	10	—	μF	Capacitor must have a low series resistance (< 1 Ohm)

Note 1: Typical VCAP voltage = 1.8 volts when VDD ≥ VDDMIN.

TABLE 30-7: DC CHARACTERISTICS: IDLE CURRENT (I_{IDLE})

DC CHARACTERISTICS			Standard Operating Conditions: 3.0V to 3.6V (unless otherwise stated) Operating temperature -40°C ≤ TA ≤ +85°C for Industrial -40°C ≤ TA ≤ +125°C for Extended			
Parameter No.	Typ.	Max.	Units	Conditions		
Idle Current (IDLE) ⁽¹⁾						
DC40d	3	8	mA	-40°C	3.3V	10 MIPS
DC40a	3	8	mA	+25°C		
DC40b	3	8	mA	+85°C		
DC40c	3	8	mA	+125°C		
DC42d	6	12	mA	-40°C	3.3V	20 MIPS
DC42a	6	12	mA	+25°C		
DC42b	6	12	mA	+85°C		
DC42c	6	12	mA	+125°C		
DC44d	11	18	mA	-40°C	3.3V	40 MIPS
DC44a	11	18	mA	+25°C		
DC44b	11	18	mA	+85°C		
DC44c	11	18	mA	+125°C		
DC45d	17	27	mA	-40°C	3.3V	60 MIPS
DC45a	17	27	mA	+25°C		
DC45b	17	27	mA	+85°C		
DC45c	17	27	mA	+125°C		
DC46d	20	35	mA	-40°C	3.3V	70 MIPS
DC46a	20	35	mA	+25°C		
DC46b	20	35	mA	+85°C		

Note 1: Base Idle current (I_{IDLE}) is measured as follows:

- CPU core is off, oscillator is configured in EC mode and external clock is active; OSC1 is driven with external square wave from rail-to-rail (EC clock overshoot/undershoot < 250 mV required)
- CLKO is configured as an I/O input pin in the Configuration Word
- All I/O pins are configured as inputs and pulled to V_{SS}
- $\overline{\text{MCLR}} = \text{V}_{\text{DD}}$, WDT and FSCM are disabled
- No peripheral modules are operating; however, every peripheral is being clocked (all PMD_x bits are zeroed)
- The NVMSIDL bit (NVMCON<12>) = 1 (i.e., Flash regulator is set to standby while the device is in Idle mode)
- The VREGSF bit (RCON<11>) = 0 (i.e., Flash regulator is set to standby while the device is in Sleep mode)
- JTAG is disabled

TABLE 31-12: ADC MODULE SPECIFICATIONS (12-BIT MODE)

AC CHARACTERISTICS			Standard Operating Conditions: 3.0V to 3.6V (unless otherwise stated) Operating temperature $-40^{\circ}\text{C} \leq T_A \leq +150^{\circ}\text{C}$				
Param No.	Symbol	Characteristic	Min	Typ	Max	Units	Conditions
ADC Accuracy (12-Bit Mode) ⁽¹⁾							
HAD20a	Nr	Resolution ⁽³⁾	12 Data Bits			bits	
HAD21a	INL	Integral Nonlinearity	-5.5	—	5.5	LSb	V _{INL} = AV _{SS} = V _{REFL} = 0V, AV _{DD} = V _{REFH} = 3.6V
HAD22a	DNL	Differential Nonlinearity	-1	—	1	LSb	V _{INL} = AV _{SS} = V _{REFL} = 0V, AV _{DD} = V _{REFH} = 3.6V
HAD23a	GERR	Gain Error	-10	—	10	LSb	V _{INL} = AV _{SS} = V _{REFL} = 0V, AV _{DD} = V _{REFH} = 3.6V
HAD24a	EOFF	Offset Error	-5	—	5	LSb	V _{INL} = AV _{SS} = V _{REFL} = 0V, AV _{DD} = V _{REFH} = 3.6V
Dynamic Performance (12-Bit Mode) ⁽²⁾							
HAD33a	FNYQ	Input Signal Bandwidth	—	—	200	kHz	

Note 1: These parameters are characterized, but are tested at 20 ksp/s only.

2: These parameters are characterized by similarity, but are not tested in manufacturing.

3: Injection currents $> |0|$ can affect the ADC results by approximately 4-6 counts.

TABLE 31-13: ADC MODULE SPECIFICATIONS (10-BIT MODE)

AC CHARACTERISTICS			Standard Operating Conditions: 3.0V to 3.6V (unless otherwise stated) Operating temperature $-40^{\circ}\text{C} \leq T_A \leq +150^{\circ}\text{C}$				
Param No.	Symbol	Characteristic	Min	Typ	Max	Units	Conditions
ADC Accuracy (10-Bit Mode) ⁽¹⁾							
HAD20b	Nr	Resolution ⁽³⁾	10 Data Bits			bits	
HAD21b	INL	Integral Nonlinearity	-1.5	—	1.5	LSb	V _{INL} = AV _{SS} = V _{REFL} = 0V, AV _{DD} = V _{REFH} = 3.6V
HAD22b	DNL	Differential Nonlinearity	-0.25	—	0.25	LSb	V _{INL} = AV _{SS} = V _{REFL} = 0V, AV _{DD} = V _{REFH} = 3.6V
HAD23b	GERR	Gain Error	-2.5	—	2.5	LSb	V _{INL} = AV _{SS} = V _{REFL} = 0V, AV _{DD} = V _{REFH} = 3.6V
HAD24b	EOFF	Offset Error	-1.25	—	1.25	LSb	V _{INL} = AV _{SS} = V _{REFL} = 0V, AV _{DD} = V _{REFH} = 3.6V
Dynamic Performance (10-Bit Mode) ⁽²⁾							
HAD33b	FNYQ	Input Signal Bandwidth	—	—	400	kHz	

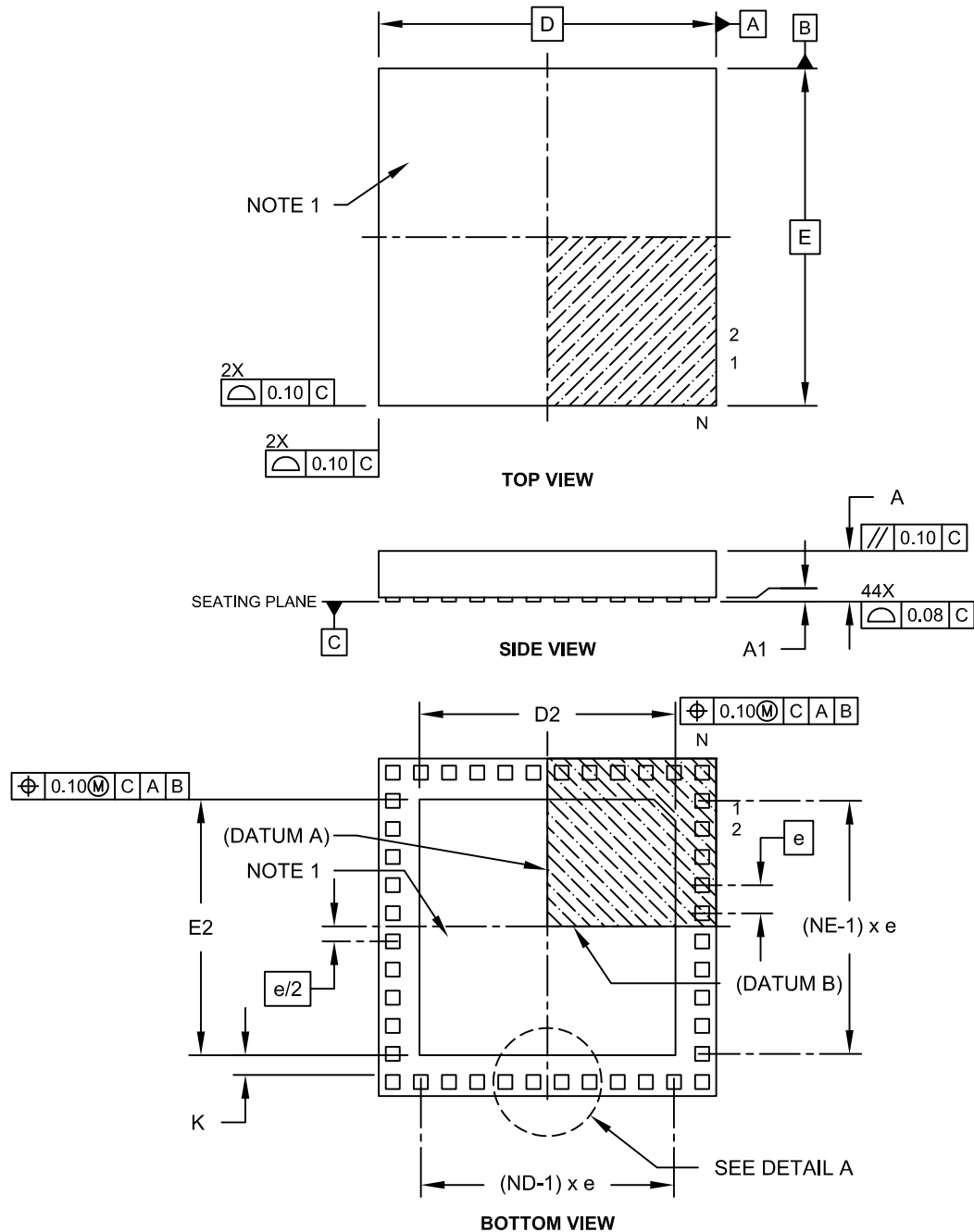
Note 1: These parameters are characterized, but are tested at 20 ksp/s only.

2: These parameters are characterized by similarity, but are not tested in manufacturing.

3: Injection currents $> |0|$ can affect the ADC results by approximately 4-6 counts.

44-Terminal Very Thin Leadless Array Package (TL) – 6x6x0.9 mm Body With Exposed Pad [VTLA]

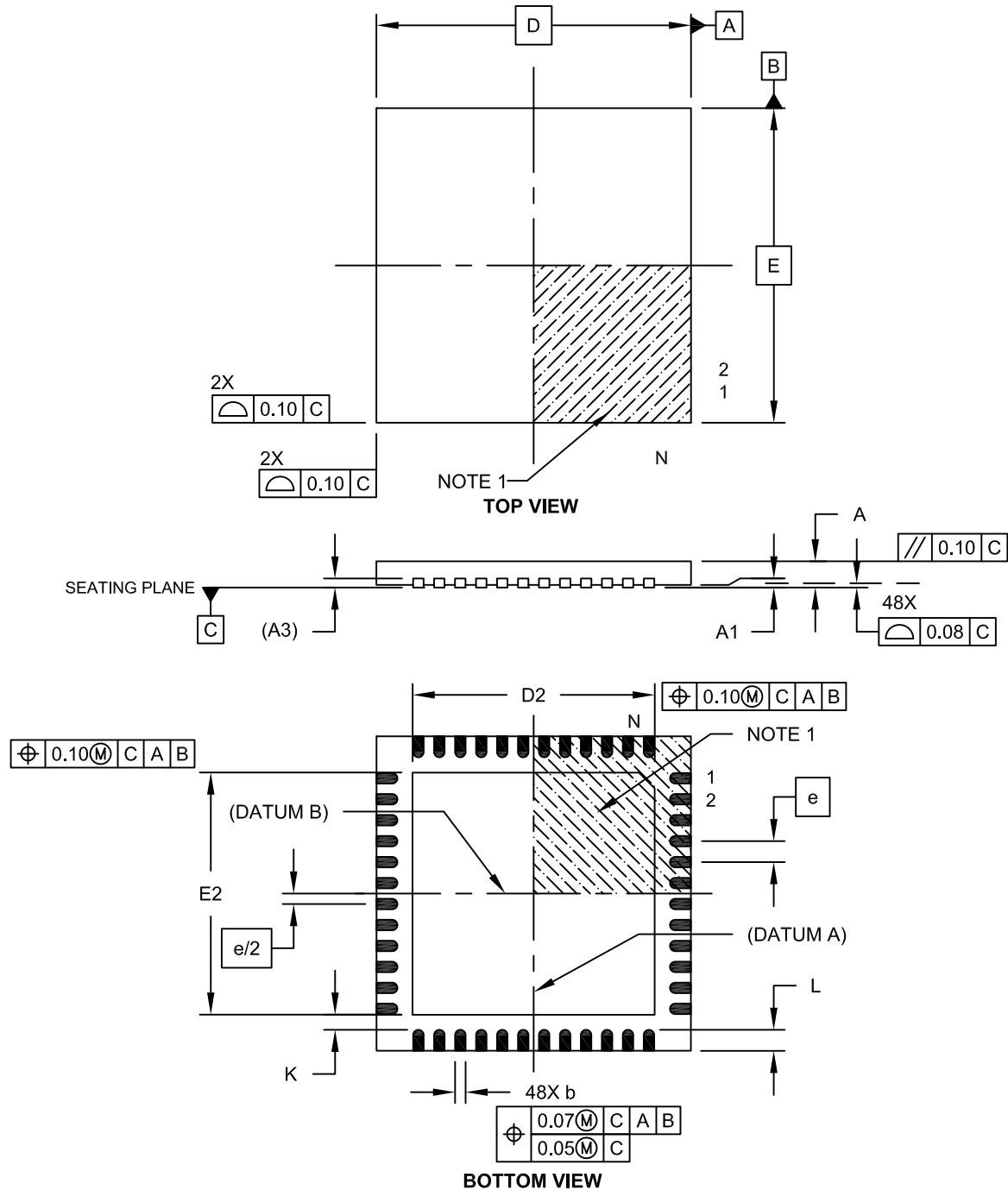
Note: For the most current package drawings, please see the Microchip Packaging Specification located at <http://www.microchip.com/packaging>



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48-Lead Plastic Ultra Thin Quad Flat, No Lead Package (MV) – 6x6x0.5 mm Body [UQFN]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at <http://www.microchip.com/packaging>



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