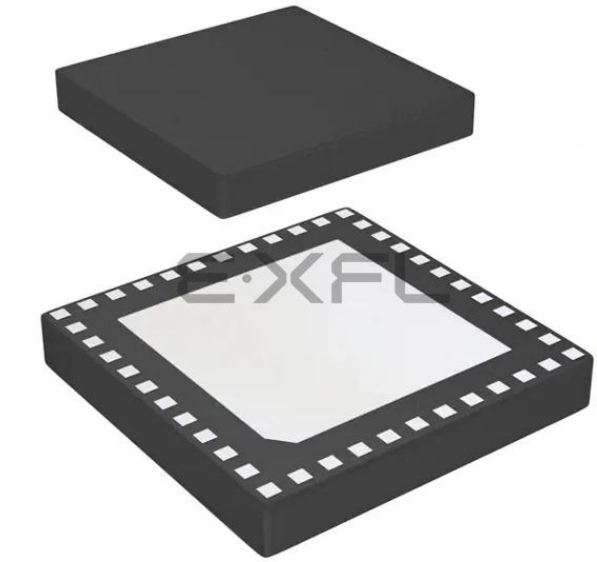

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Details	
Product Status	Obsolete
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Speed	60 MIPs
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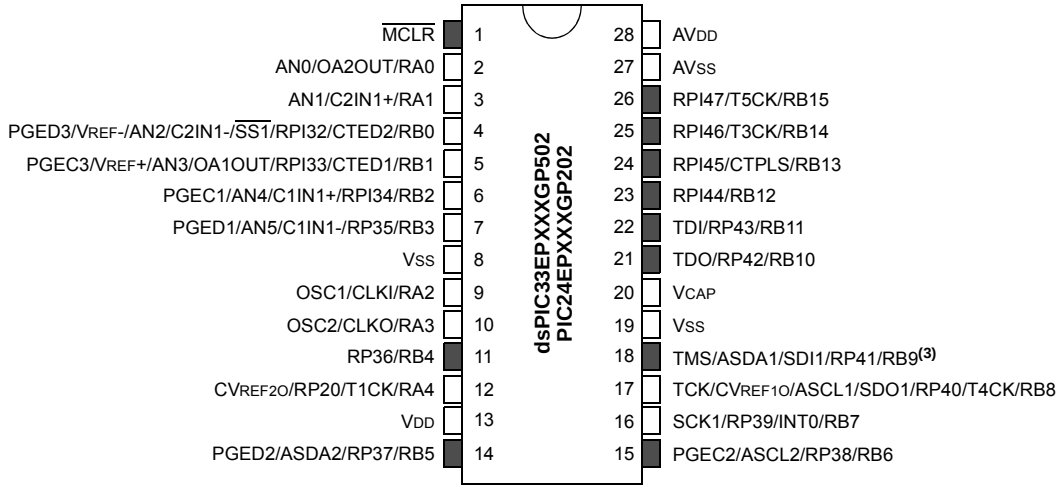
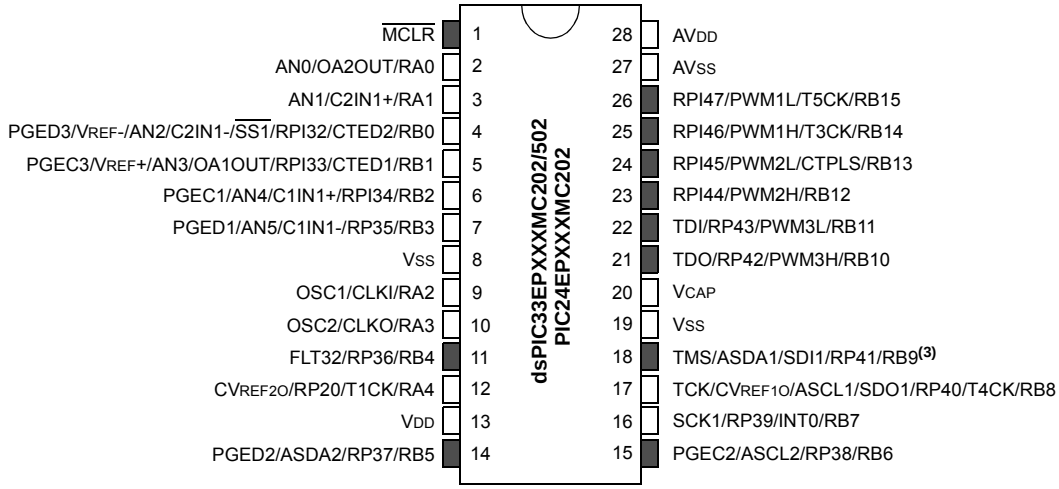
Peripherals	Brown-out Detect/Reset, DMA, Motor Control PWM, POR, PWM, WDT
Number of I/O	35
Program Memory Size	256KB (85.5K x 24)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	16K x 16
Voltage - Supply (Vcc/Vdd)	3V ~ 3.6V
Data Converters	A/D 9x10b/12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 125°C (TA)
Mounting Type	Surface Mount
Package / Case	44-VFTLA Exposed Pad
Supplier Device Package	44-VTLA (6x6)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/pic24ep256mc204t-e-tl

Pin Diagrams

28-Pin SPDIP/SOIC/SSOP(1,2)

■ = Pins are up to 5V tolerant





Note 1: The RPn/RPIn pins can be used by any remappable peripheral with some limitation. See **Section 11.4 "Peripheral Pin Select (PPS)"** for available peripherals and for information on limitations.

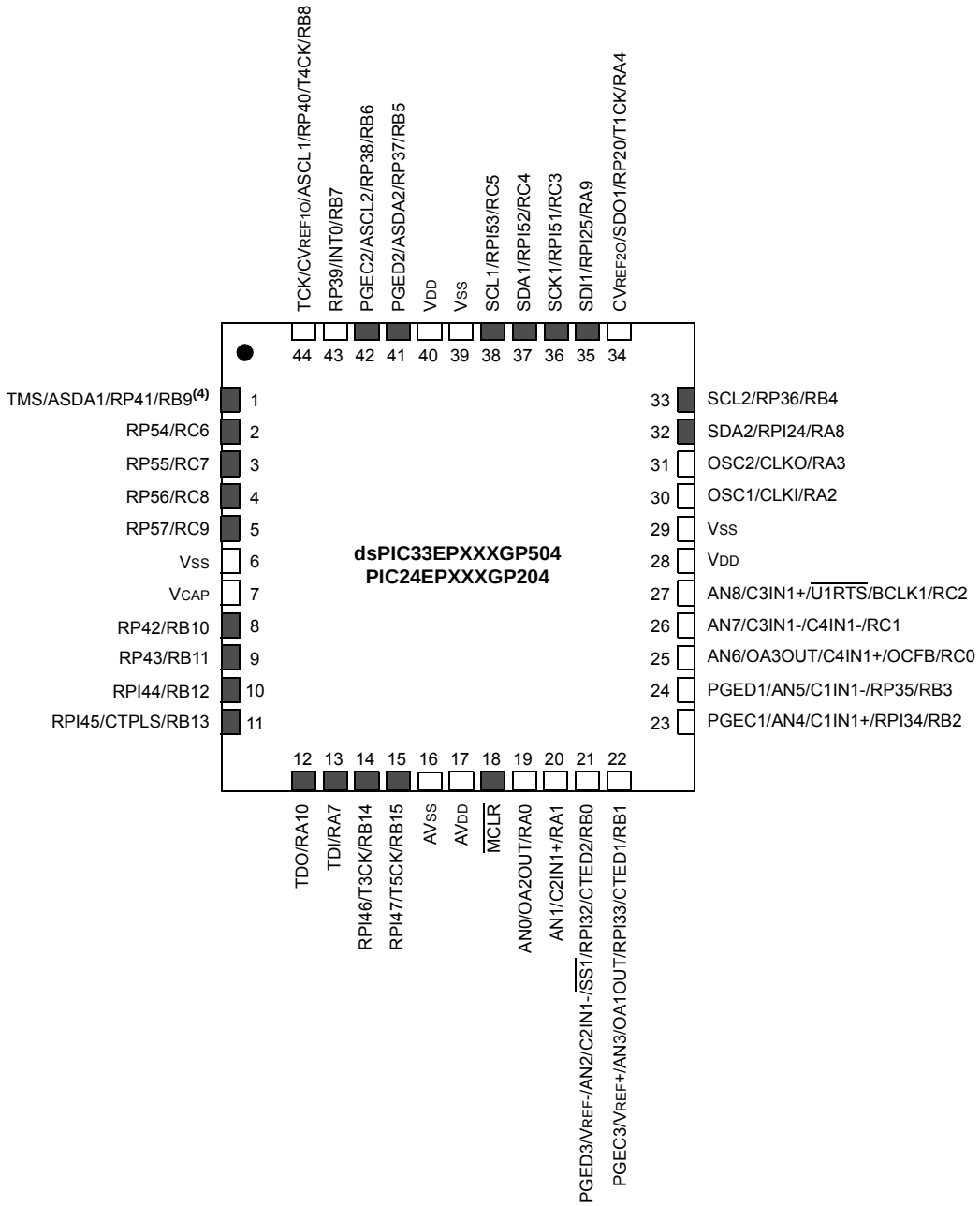
2: Every I/O port pin (RAx-RGx) can be used as a Change Notification pin (CNAx-CNGx). See **Section 11.0 "I/O Ports"** for more information.

3: There is an internal pull-up resistor connected to the TMS pin when the JTAG interface is active. See the JTAGEN bit field in Table 27-2.

Pin Diagrams (Continued)

44-Pin QFN(1,2,3)

■ = Pins are up to 5V tolerant



Note 1: The RPn/RPIn pins can be used by any remappable peripheral with some limitation. See **Section 11.4 "Peripheral Pin Select (PPS)"** for available peripherals and for information on limitations.

2: Every I/O port pin (RAx-RGx) can be used as a Change Notification pin (CNAx-CNGx). See **Section 11.0 "I/O Ports"** for more information.

3: The metal pad at the bottom of the device is not connected to any pins and is recommended to be connected to VSS externally.

4: There is an internal pull-up resistor connected to the TMS pin when the JTAG interface is active. See the JTAGEN bit field in Table 27-2.

4.0 MEMORY ORGANIZATION

Note: This data sheet summarizes the features of the dsPIC33EPXXXGP50X, dsPIC33EPXXXMC20X/50X and PIC24EPXXXGP/MC20X families of devices. It is not intended to be a comprehensive reference source. To complement the information in this data sheet, refer to **"Program Memory"** (DS70613) in the "*dsPIC33/PIC24 Family Reference Manual*", which is available from the Microchip web site (www.microchip.com).

The dsPIC33EPXXXGP50X, dsPIC33EPXXXMC20X/50X and PIC24EPXXXGP/MC20X architecture features separate program and data memory spaces, and buses. This architecture also allows the direct access of program memory from the Data Space (DS) during code execution.

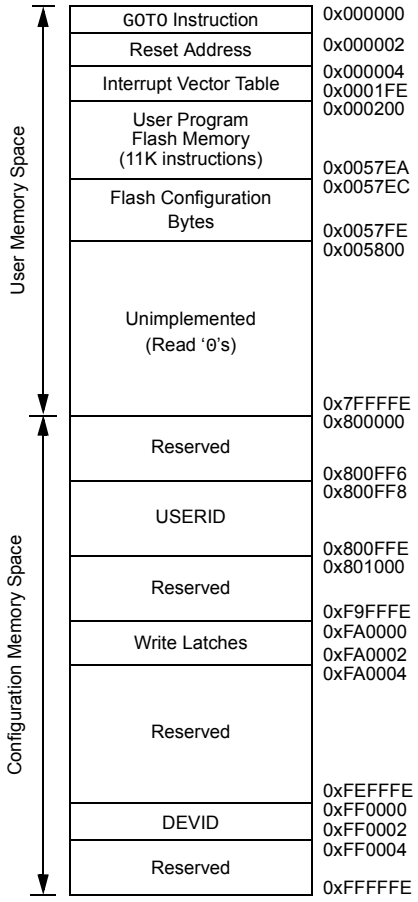
4.1 Program Address Space

The program address memory space of the dsPIC33EPXXXGP50X, dsPIC33EPXXXMC20X/50X and PIC24EPXXXGP/MC20X devices is 4M instructions. The space is addressable by a 24-bit value derived either from the 23-bit PC during program execution, or from table operation or Data Space remapping, as described in **Section 4.8 "Interfacing Program and Data Memory Spaces"**.

User application access to the program memory space is restricted to the lower half of the address range (0x000000 to 0x7FFFFF). The exception is the use of TBLRD operations, which use TBLPAG<7> to read Device ID sections of the configuration memory space.

The program memory maps, which are presented by device family and memory size, are shown in Figure 4-1 through Figure 4-5.

FIGURE 4-1: PROGRAM MEMORY MAP FOR dsPIC33EP32GP50X, dsPIC33EP32MC20X/50X AND PIC24EP32GP/MC20X DEVICES



Note: Memory areas are not shown to scale.

TABLE 4-8: TIMER1 THROUGH TIMER5 REGISTER MAP

SFR Name	Addr.	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	All Resets
TMR1	0100	Timer1 Register																xxxx
PR1	0102	Period Register 1																FFFF
T1CON	0104	TON	—	TSIDL	—	—	—	—	—	—	TGATE	TCKPS<1:0>		—	TSYNC	TCS	—	0000
TMR2	0106	Timer2 Register																xxxx
TMR3HLD	0108	Timer3 Holding Register (for 32-bit timer operations only)																xxxx
TMR3	010A	Timer3 Register																xxxx
PR2	010C	Period Register 2																FFFF
PR3	010E	Period Register 3																FFFF
T2CON	0110	TON	—	TSIDL	—	—	—	—	—	—	TGATE	TCKPS<1:0>		T32	—	TCS	—	0000
T3CON	0112	TON	—	TSIDL	—	—	—	—	—	—	TGATE	TCKPS<1:0>		—	—	TCS	—	0000
TMR4	0114	Timer4 Register																xxxx
TMR5HLD	0116	Timer5 Holding Register (for 32-bit operations only)																xxxx
TMR5	0118	Timer5 Register																xxxx
PR4	011A	Period Register 4																FFFF
PR5	011C	Period Register 5																FFFF
T4CON	011E	TON	—	TSIDL	—	—	—	—	—	—	TGATE	TCKPS<1:0>		T32	—	TCS	—	0000
T5CON	0120	TON	—	TSIDL	—	—	—	—	—	—	TGATE	TCKPS<1:0>		—	—	TCS	—	0000

Legend: x = unknown value on Reset, — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

TABLE 4-59: PORTA REGISTER MAP FOR PIC24EPXXXGP/MC202 AND dsPIC33EPXXXGP/MC202/502 DEVICES ONLY

File Name	Addr.	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	All Resets
TRISA	0E00	—	—	—	—	—	—	—	—	—	—	—	TRISA4	TRISA3	TRISA2	TRISA1	TRISA0	001F
PORTA	0E02	—	—	—	—	—	—	—	—	—	—	—	RA4	RA3	RA2	RA1	RA0	0000
LATA	0E04	—	—	—	—	—	—	—	—	—	—	—	LATA4	LATA3	LATA2	LA1TA1	LA0TA0	0000
ODCA	0E06	—	—	—	—	—	—	—	—	—	—	—	ODCA4	ODCA3	ODCA2	ODCA1	ODCA0	0000
CNENA	0E08	—	—	—	—	—	—	—	—	—	—	—	CNIEA4	CNIEA3	CNIEA2	CNIEA1	CNIEA0	0000
CNPUA	0E0A	—	—	—	—	—	—	—	—	—	—	—	CNPUA4	CNPUA3	CNPUA2	CNPUA1	CNPUA0	0000
CNPDA	0E0C	—	—	—	—	—	—	—	—	—	—	—	CNPDA4	CNPDA3	CNPDA2	CNPDA1	CNPDA0	0000
ANSELA	0E0E	—	—	—	—	—	—	—	—	—	—	—	ANSA4	—	—	ANSA1	ANSA0	0013

Legend: — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

TABLE 4-60: PORTB REGISTER MAP FOR PIC24EPXXXGP/MC202 AND dsPIC33EPXXXGP/MC202/502 DEVICES ONLY

File Name	Addr.	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	All Resets
TRISB	0E10	TRISB15	TRISB14	TRISB13	TRISB12	TRISB11	TRISB10	TRISB9	TRISB8	TRISB7	TRISB6	TRISB5	TRISB4	TRISB3	TRISB2	TRISB1	TRISB0	FFFF
PORTB	0E12	RB15	RB14	RB13	RB12	RB11	RB10	RB9	RB8	RB7	RB6	RB5	RB4	RB3	RB2	RB1	RB0	xxxx
LATB	0E14	LATB15	LATB14	LATB13	LATB12	LATB11	LATB10	LATB9	LATB8	LATB7	LATB6	LATB5	LATB4	LATB3	LATB2	LATB1	LATB0	xxxx
ODCB	0E16	ODCB15	ODCB14	ODCB13	ODCB12	ODCB11	ODCB10	ODCB9	ODCB8	ODCB7	ODCB6	ODCB5	ODCB4	ODCB3	ODCB2	ODCB1	ODCB0	0000
CNENB	0E18	CNIEB15	CNIEB14	CNIEB13	CNIEB12	CNIEB11	CNIEB10	CNIEB9	CNIEB8	CNIEB7	CNIEB6	CNIEB5	CNIEB4	CNIEB3	CNIEB2	CNIEB1	CNIEB0	0000
CNPUB	0E1A	CNPUB15	CNPUB14	CNPUB13	CNPUB12	CNPUB11	CNPUB10	CNPUB9	CNPUB8	CNPUB7	CNPUB6	CNPUB5	CNPUB4	CNPUB3	CNPUB2	CNPUB1	CNPUB0	0000
CNPDB	0E1C	CNPDB15	CNPDB14	CNPDB13	CNPDB12	CNPDB11	CNPDB10	CNPDB9	CNPDB8	CNPDB7	CNPDB6	CNPDB5	CNPDB4	CNPDB3	CNPDB2	CNPDB1	CNPDB0	0000
ANSELB	0E1E	—	—	—	—	—	—	—	ANSB8	—	—	—	—	ANSB3	ANSB2	ANSB1	ANSB0	010F

Legend: x = unknown value on Reset, — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

Allocating different Page registers for read and write access allows the architecture to support data movement between different pages in data memory. This is accomplished by setting the DSRPAG register value to the page from which you want to read, and configuring the DSWPAG register to the page to which it needs to be written. Data can also be moved from different PSV to EDS pages, by configuring the DSRPAG and DSWPAG registers to address PSV and EDS space, respectively. The data can be moved between pages by a single instruction.

When an EDS or PSV page overflow or underflow occurs, EA<15> is cleared as a result of the register indirect EA calculation. An overflow or underflow of the EA in the EDS or PSV pages can occur at the page boundaries when:

- The initial address prior to modification addresses an EDS or PSV page
- The EA calculation uses Pre-Modified or Post-Modified Register Indirect Addressing; however, this does not include Register Offset Addressing

In general, when an overflow is detected, the DSxPAG register is incremented and the EA<15> bit is set to keep the base address within the EDS or PSV window. When an underflow is detected, the DSxPAG register is decremented and the EA<15> bit is set to keep the base address within the EDS or PSV window. This creates a linear EDS and PSV address space, but only when using Register Indirect Addressing modes.

Exceptions to the operation described above arise when entering and exiting the boundaries of Page 0, EDS and PSV spaces. Table 4-61 lists the effects of overflow and underflow scenarios at different boundaries.

In the following cases, when overflow or underflow occurs, the EA<15> bit is set and the DSxPAG is not modified; therefore, the EA will wrap to the beginning of the current page:

- Register Indirect with Register Offset Addressing
- Modulo Addressing
- Bit-Reversed Addressing

TABLE 4-61: OVERFLOW AND UNDERFLOW SCENARIOS AT PAGE 0, EDS and PSV SPACE BOUNDARIES(2,3,4)

O/U, R/W	Operation	Before			After		
		DSxPAG	DS EA<15>	Page Description	DSxPAG	DS EA<15>	Page Description
O, Read	[++Wn] or [Wn++]	DSRPAG = 0x1FF	1	EDS: Last page	DSRPAG = 0x1FF	0	See **Note 1**
O, Read		DSRPAG = 0x2FF	1	PSV: Last lsw page	DSRPAG = 0x300	1	PSV: First MSB page
O, Read		DSRPAG = 0x3FF	1	PSV: Last MSB page	DSRPAG = 0x3FF	0	See **Note 1**
O, Write		DSWPAG = 0x1FF	1	EDS: Last page	DSWPAG = 0x1FF	0	See **Note 1**
U, Read	[--Wn] or [Wn--]	DSRPAG = 0x001	1	PSV page	DSRPAG = 0x001	0	See **Note 1**
U, Read		DSRPAG = 0x200	1	PSV: First lsw page	DSRPAG = 0x200	0	See **Note 1**
U, Read		DSRPAG = 0x300	1	PSV: First MSB page	DSRPAG = 0x2FF	1	PSV: Last lsw page

Legend: O = Overflow, U = Underflow, R = Read, W = Write

Note 1: The Register Indirect Addressing now addresses a location in the base Data Space (0x0000-0x8000).

2: An EDS access with DSxPAG = 0x000 will generate an address error trap.

3: Only reads from PS are supported using DSRPAG. An attempt to write to PS using DSWPAG will generate an address error trap.

4: Pseudo-Linear Addressing is not supported for large offsets.

REGISTER 8-1: DMAxCON: DMA CHANNEL x CONTROL REGISTER

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	U-0	U-0	U-0
CHEN	SIZE	DIR	HALF	NULLW	—	—	—
bit 15							bit 8

U-0	U-0	R/W-0	R/W-0	U-0	U-0	R/W-0	R/W-0
—	—	AMODE1	AMODE0	—	—	MODE1	MODE0
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15 **CHEN:** DMA Channel Enable bit
1 = Channel is enabled
0 = Channel is disabled

bit 14 **SIZE:** DMA Data Transfer Size bit
1 = Byte
0 = Word

bit 13 **DIR:** DMA Transfer Direction bit (source/destination bus select)
1 = Reads from RAM address, writes to peripheral address
0 = Reads from peripheral address, writes to RAM address

bit 12 **HALF:** DMA Block Transfer Interrupt Select bit
1 = Initiates interrupt when half of the data has been moved
0 = Initiates interrupt when all of the data has been moved

bit 11 **NULLW:** Null Data Peripheral Write Mode Select bit
1 = Null data write to peripheral in addition to RAM write (DIR bit must also be clear)
0 = Normal operation

bit 10-6 **Unimplemented:** Read as '0'

bit 5-4 **AMODE<1:0>:** DMA Channel Addressing Mode Select bits
11 = Reserved
10 = Peripheral Indirect Addressing mode
01 = Register Indirect without Post-Increment mode
00 = Register Indirect with Post-Increment mode

bit 3-2 **Unimplemented:** Read as '0'

bit 1-0 **MODE<1:0>:** DMA Channel Operating Mode Select bits
11 = One-Shot, Ping-Pong modes are enabled (one block transfer from/to each DMA buffer)
10 = Continuous, Ping-Pong modes are enabled
01 = One-Shot, Ping-Pong modes are disabled
00 = Continuous, Ping-Pong modes are disabled

10.3 Doze Mode

The preferred strategies for reducing power consumption are changing clock speed and invoking one of the power-saving modes. In some circumstances, this cannot be practical. For example, it may be necessary for an application to maintain uninterrupted synchronous communication, even while it is doing nothing else. Reducing system clock speed can introduce communication errors, while using a power-saving mode can stop communications completely.

Doze mode is a simple and effective alternative method to reduce power consumption while the device is still executing code. In this mode, the system clock continues to operate from the same source and at the same speed. Peripheral modules continue to be clocked at the same speed, while the CPU clock speed is reduced. Synchronization between the two clock domains is maintained, allowing the peripherals to access the SFRs while the CPU executes code at a slower rate.

Doze mode is enabled by setting the DOZEN bit (CLKDIV<11>). The ratio between peripheral and core clock speed is determined by the DOZE<2:0> bits (CLKDIV<14:12>). There are eight possible configurations, from 1:1 to 1:128, with 1:1 being the default setting.

Programs can use Doze mode to selectively reduce power consumption in event-driven applications. This allows clock-sensitive functions, such as synchronous communications, to continue without interruption while the CPU Idles, waiting for something to invoke an interrupt routine. An automatic return to full-speed CPU operation on interrupts can be enabled by setting the ROI bit (CLKDIV<15>). By default, interrupt events have no effect on Doze mode operation.

For example, suppose the device is operating at 20 MIPS and the ECAN™ module has been configured for 500 kbps, based on this device operating speed. If the device is placed in Doze mode with a clock frequency ratio of 1:4, the ECAN module continues to communicate at the required bit rate of 500 kbps, but the CPU now starts executing instructions at a frequency of 5 MIPS.

10.4 Peripheral Module Disable

The Peripheral Module Disable (PMD) registers provide a method to disable a peripheral module by stopping all clock sources supplied to that module. When a peripheral is disabled using the appropriate PMD control bit, the peripheral is in a minimum power consumption state. The control and status registers associated with the peripheral are also disabled, so writes to those registers do not have effect and read values are invalid.

A peripheral module is enabled only if both the associated bit in the PMD register is cleared and the peripheral is supported by the specific dsPIC® DSC variant. If the peripheral is present in the device, it is enabled in the PMD register by default.

Note:	If a PMD bit is set, the corresponding module is disabled after a delay of one instruction cycle. Similarly, if a PMD bit is cleared, the corresponding module is enabled after a delay of one instruction cycle (assuming the module control registers are already configured to enable module operation).

10.5 Power-Saving Resources

Many useful resources are provided on the main product page of the Microchip web site for the devices listed in this data sheet. This product page, which can be accessed using this link, contains the latest updates and additional information.

Note:	In the event you are not able to access the product page using the link above, enter this URL in your browser: http://www.microchip.com/wwwproducts/Devices.aspx?dDocName=en555464

10.5.1 KEY RESOURCES

- **"Watchdog Timer and Power-Saving Modes"** (DS70615) in the *"dsPIC33/PIC24 Family Reference Manual"*
- Code Samples
- Application Notes
- Software Libraries
- Webinars
- All Related *"dsPIC33/PIC24 Family Reference Manual"* Sections
- Development Tools

REGISTER 10-5: PMD6: PERIPHERAL MODULE DISABLE CONTROL REGISTER 6

U-0	U-0	U-0	U-0	U-0	R/W-0	R/W-0	R/W-0
—	—	—	—	—	PWM3MD(1)	PWM2MD(1)	PWM1MD(1)
bit 15							bit 8

U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
—	—	—	—	—	—	—	—
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15-11 **Unimplemented:** Read as '0'

bit 10 **PWM3MD:** PWM3 Module Disable bit(1)
1 = PWM3 module is disabled
0 = PWM3 module is enabled

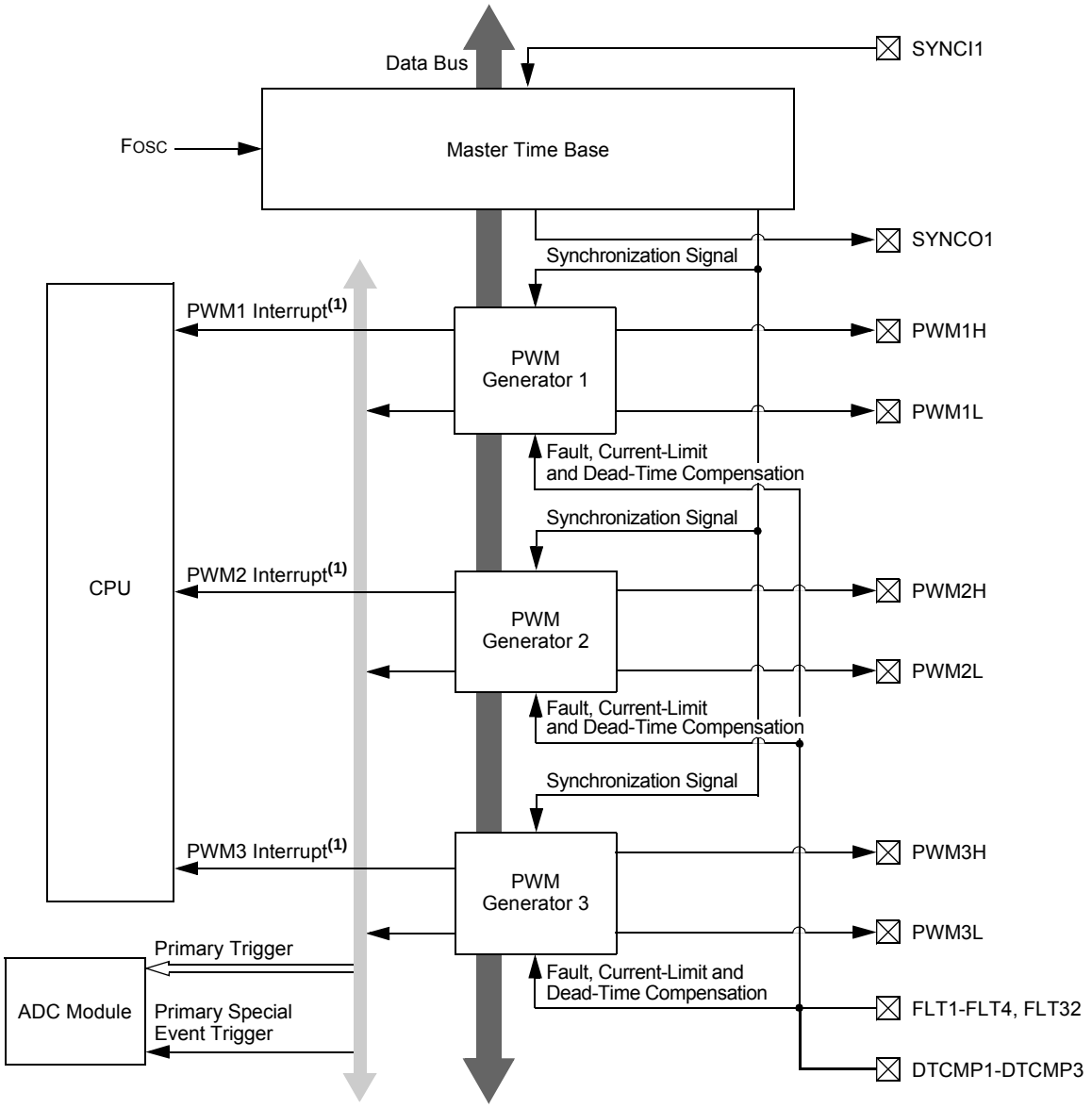
bit 9 **PWM2MD:** PWM2 Module Disable bit(1)
1 = PWM2 module is disabled
0 = PWM2 module is enabled

bit 8 **PWM1MD:** PWM1 Module Disable bit(1)
1 = PWM1 module is disabled
0 = PWM1 module is enabled

bit 7-0 **Unimplemented:** Read as '0'

Note 1: This bit is available on dsPIC33EPXXXMC50X/20X and PIC24EPXXXMC20X devices only.

FIGURE 16-1: HIGH-SPEED PWMx MODULE ARCHITECTURAL OVERVIEW



Note 1: The PWM interrupts are generated by logically ORing the FLTSTAT, CLSTAT and TRGSTAT status bits for the given PWM generator. Refer to the "*dsPIC33/PIC24 Family Reference Manual*", **"High-Speed PWM"** (DS70645) for more information.

REGISTER 19-1: I2CxCON: I2Cx CONTROL REGISTER (CONTINUED)

bit 6 **STREN:** SCLx Clock Stretch Enable bit (when operating as I^2C slave)
Used in conjunction with the SCLREL bit.
1 = Enables software or receives clock stretching
0 = Disables software or receives clock stretching

bit 5 **ACKDT:** Acknowledge Data bit (when operating as I^2C master, applicable during master receive)
Value that is transmitted when the software initiates an Acknowledge sequence.
1 = Sends NACK during Acknowledge
0 = Sends ACK during Acknowledge

bit 4 **ACKEN:** Acknowledge Sequence Enable bit
(when operating as I^2C master, applicable during master receive)
1 = Initiates Acknowledge sequence on SDAx and SCLx pins and transmits ACKDT data bit. Hardware is clear at the end of the master Acknowledge sequence.
0 = Acknowledge sequence is not in progress

bit 3 **RCEN:** Receive Enable bit (when operating as I^2C master)
1 = Enables Receive mode for I^2C. Hardware is clear at the end of the eighth bit of the master receive data byte.
0 = Receive sequence is not in progress

bit 2 **PEN:** Stop Condition Enable bit (when operating as I^2C master)
1 = Initiates Stop condition on SDAx and SCLx pins. Hardware is clear at the end of the master Stop sequence.
0 = Stop condition is not in progress

bit 1 **RSEN:** Repeated Start Condition Enable bit (when operating as I^2C master)
1 = Initiates Repeated Start condition on SDAx and SCLx pins. Hardware is clear at the end of the master Repeated Start sequence.
0 = Repeated Start condition is not in progress

bit 0 **SEN:** Start Condition Enable bit (when operating as I^2C master)
1 = Initiates Start condition on SDAx and SCLx pins. Hardware is clear at the end of the master Start sequence.
0 = Start condition is not in progress

Note 1: When performing master operations, ensure that the IPMIEN bit is set to '0'.

REGISTER 21-4: CxFCTRL: ECANx FIFO CONTROL REGISTER

R/W-0	R/W-0	R/W-0	U-0	U-0	U-0	U-0	U-0
DMABS2	DMABS1	DMABS0	—	—	—	—	—
bit 15							bit 8

U-0	U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
—	—	—	FSA4	FSA3	FSA2	FSA1	FSA0
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 15-13 **DMABS<2:0>:** DMA Buffer Size bits
111 = Reserved
110 = 32 buffers in RAM
101 = 24 buffers in RAM
100 = 16 buffers in RAM
011 = 12 buffers in RAM
010 = 8 buffers in RAM
001 = 6 buffers in RAM
000 = 4 buffers in RAM

bit 12-5 **Unimplemented:** Read as ‘0’

bit 4-0 **FSA<4:0>:** FIFO Area Starts with Buffer bits
11111 = Read Buffer RB31
11110 = Read Buffer RB30
•
•
•
00001 = TX/RX Buffer TRB1
00000 = TX/RX Buffer TRB0

REGISTER 21-11: CxFEN1: ECANx ACCEPTANCE FILTER ENABLE REGISTER 1

R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1
FLTEN15	FLTEN14	FLTEN13	FLTEN12	FLTEN11	FLTEN10	FLTEN9	FLTEN8
bit 15							bit 8

R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1
FLTEN7	FLTEN6	FLTEN5	FLTEN4	FLTEN3	FLTEN2	FLTEN1	FLTEN0
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 15-0 **FLTEN<15:0>:** Enable Filter n to Accept Messages bits
1 = Enables Filter n
0 = Disables Filter n

REGISTER 21-12: CxBUFPNT1: ECANx FILTER 0-3 BUFFER POINTER REGISTER 1

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
F3BP<3:0>				F2BP<3:0>			
bit 15							bit 8

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
F1BP<3:0>				F0BP<3:0>			
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 15-12 **F3BP<3:0>:** RX Buffer Mask for Filter 3 bits
1111 = Filter hits received in RX FIFO buffer
1110 = Filter hits received in RX Buffer 14
•
•
•
0001 = Filter hits received in RX Buffer 1
0000 = Filter hits received in RX Buffer 0

bit 11-8 **F2BP<3:0>:** RX Buffer Mask for Filter 2 bits (same values as bits<15:12>)

bit 7-4 **F1BP<3:0>:** RX Buffer Mask for Filter 1 bits (same values as bits<15:12>)

bit 3-0 **F0BP<3:0>:** RX Buffer Mask for Filter 0 bits (same values as bits<15:12>)

TABLE 24-1: PTG STEP COMMAND FORMAT (CONTINUED)

bit 3-0	Step Command	OPTION<3:0>	Option Description
	PTGCTRL(1)	0000	Reserved.
		0001	Reserved.
		0010	Disable Step Delay Timer (PTGSD).
		0011	Reserved.
		0100	Reserved.
		0101	Reserved.
		0110	Enable Step Delay Timer (PTGSD).
		0111	Reserved.
		1000	Start and wait for the PTG Timer0 to match the Timer0 Limit Register.
		1001	Start and wait for the PTG Timer1 to match the Timer1 Limit Register.
		1010	Reserved.
		1011	Wait for the software trigger bit transition from low-to-high before continuing (PTGSWT = 0 to 1).
		1100	Copy contents of the Counter 0 register to the AD1CHS0 register.
		1101	Copy contents of the Counter 1 register to the AD1CHS0 register.
		1110	Copy contents of the Literal 0 register to the AD1CHS0 register.
		1111	Generate triggers indicated in the Broadcast Trigger Enable register (PTGBTE).
	PTGADD(1)	0000	Add contents of the PTGADJ register to the Counter 0 Limit register (PTGC0LIM).
		0001	Add contents of the PTGADJ register to the Counter 1 Limit register (PTGC1LIM).
		0010	Add contents of the PTGADJ register to the Timer0 Limit register (PTGT0LIM).
		0011	Add contents of the PTGADJ register to the Timer1 Limit register (PTGT1LIM).
		0100	Add contents of the PTGADJ register to the Step Delay Limit register (PTGSDLIM).
		0101	Add contents of the PTGADJ register to the Literal 0 register (PTGL0).
		0110	Reserved.
		0111	Reserved.
	PTGCOPY(1)	1000	Copy contents of the PTGHOLD register to the Counter 0 Limit register (PTGC0LIM).
		1001	Copy contents of the PTGHOLD register to the Counter 1 Limit register (PTGC1LIM).
		1010	Copy contents of the PTGHOLD register to the Timer0 Limit register (PTGT0LIM).
		1011	Copy contents of the PTGHOLD register to the Timer1 Limit register (PTGT1LIM).
		1100	Copy contents of the PTGHOLD register to the Step Delay Limit register (PTGSDLIM).
		1101	Copy contents of the PTGHOLD register to the Literal 0 register (PTGL0).
		1110	Reserved.
		1111	Reserved.

Note 1: All reserved commands or options will execute but have no effect (i.e., execute as a NOP instruction).

2: Refer to Table 24-2 for the trigger output descriptions.

3: This feature is only available on dsPIC33EPXXXMC20X/50X and PIC24EPXXXMC20X devices.

REGISTER 25-3: CM4CON: COMPARATOR 4 CONTROL REGISTER

R/W-0	R/W-0	R/W-0	U-0	U-0	U-0	R/W-0	R/W-0
CON	COE	CPOL	—	—	—	CEVT	COUT
bit 15							bit 8

R/W-0	R/W-0	U-0	R/W-0	U-0	U-0	R/W-0	R/W-0
EVPOL1	EVPOL0	—	CREF(1)	—	—	CCH1(1)	CCH0(1)
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15 **CON:** Comparator Enable bit
1 = Comparator is enabled
0 = Comparator is disabled

bit 14 **COE:** Comparator Output Enable bit
1 = Comparator output is present on the CxOUT pin
0 = Comparator output is internal only

bit 13 **CPOL:** Comparator Output Polarity Select bit
1 = Comparator output is inverted
0 = Comparator output is not inverted

bit 12-10 **Unimplemented:** Read as '0'

bit 9 **CEVT:** Comparator Event bit
1 = Comparator event according to EVPOL<1:0> settings occurred; disables future triggers and interrupts until the bit is cleared
0 = Comparator event did not occur

bit 8 **COUT:** Comparator Output bit
When CPOL = 0 (non-inverted polarity):
1 = VIN+ > VIN-
0 = VIN+ < VIN-
When CPOL = 1 (inverted polarity):
1 = VIN+ < VIN-
0 = VIN+ > VIN-

bit 7-6 **EVPOL<1:0>:** Trigger/Event/Interrupt Polarity Select bits
11 = Trigger/event/interrupt generated on any change of the comparator output (while CEVT = 0)
10 = Trigger/event/interrupt generated only on high-to-low transition of the polarity selected comparator output (while CEVT = 0)
If CPOL = 1 (inverted polarity):
Low-to-high transition of the comparator output.
If CPOL = 0 (non-inverted polarity):
High-to-low transition of the comparator output.
01 = Trigger/event/interrupt generated only on low-to-high transition of the polarity selected comparator output (while CEVT = 0)
If CPOL = 1 (inverted polarity):
High-to-low transition of the comparator output.
If CPOL = 0 (non-inverted polarity):
Low-to-high transition of the comparator output.
00 = Trigger/event/interrupt generation is disabled

Note 1: Inputs that are selected and not available will be tied to VSS. See the **"Pin Diagrams"** section for available inputs for each package.

Most instructions are a single word. Certain double-word instructions are designed to provide all the required information in these 48 bits. In the second word, the 8 MSbs are '0's. If this second word is executed as an instruction (by itself), it executes as a NOP.

The double-word instructions execute in two instruction cycles.

Most single-word instructions are executed in a single instruction cycle, unless a conditional test is true, or the Program Counter is changed as a result of the instruction, or a PSV or Table Read is performed, or an SFR register is read. In these cases, the execution takes multiple instruction cycles with the additional instruction cycle(s) executed as a NOP. Certain instructions that involve skipping over the subsequent instruction require either two or three cycles if the skip is performed, depending on whether the instruction being skipped is a single-word or two-word instruction. Moreover, double-word moves require two cycles.

Note: For more details on the instruction set, refer to the *"16-bit MCU and DSC Programmer's Reference Manual"* (DS70157).

For more information on instructions that take more than one instruction cycle to execute, refer to **"CPU"** (DS70359) in the *"dsPIC33/PIC24 Family Reference Manual"*, particularly the **"Instruction Flow Types"** section.

TABLE 28-1: SYMBOLS USED IN OPCODE DESCRIPTIONS

Field	Description
#text	Means literal defined by "text"
(text)	Means "content of text"
[text]	Means "the location addressed by text"
{ }	Optional field or operation
a ∈ {b, c, d}	a is selected from the set of values b, c, d
<n:m>	Register bit field
.b	Byte mode selection
.d	Double-Word mode selection
.S	Shadow register select
.w	Word mode selection (default)
Acc	One of two accumulators {A, B}
AWB	Accumulator write back destination address register ∈ {W13, [W13]+ = 2}
bit4	4-bit bit selection field (used in word addressed instructions) ∈ {0...15}
C, DC, N, OV, Z	MCU Status bits: Carry, Digit Carry, Negative, Overflow, Sticky Zero
Expr	Absolute address, label or expression (resolved by the linker)
f	File register address ∈ {0x0000...0x1FFF}
lit1	1-bit unsigned literal ∈ {0,1}
lit4	4-bit unsigned literal ∈ {0...15}
lit5	5-bit unsigned literal ∈ {0...31}
lit8	8-bit unsigned literal ∈ {0...255}
lit10	10-bit unsigned literal ∈ {0...255} for Byte mode, {0:1023} for Word mode
lit14	14-bit unsigned literal ∈ {0...16384}
lit16	16-bit unsigned literal ∈ {0...65535}
lit23	23-bit unsigned literal ∈ {0...8388608}; LSb must be '0'
None	Field does not require an entry, can be blank
OA, OB, SA, SB	DSP Status bits: ACCA Overflow, ACCB Overflow, ACCA Saturate, ACCB Saturate
PC	Program Counter
Slit10	10-bit signed literal ∈ {-512...511}
Slit16	16-bit signed literal ∈ {-32768...32767}
Slit6	6-bit signed literal ∈ {-16...16}
Wb	Base W register ∈ {W0...W15}
Wd	Destination W register ∈ { Wd, [Wd], [Wd++], [Wd--], [++Wd], [--Wd] }
Wdo	Destination W register ∈ { Wnd, [Wnd], [Wnd++], [Wnd--], [++Wnd], [--Wnd], [Wnd+Wb] }

TABLE 28-2: INSTRUCTION SET OVERVIEW (CONTINUED)

Base Instr #	Assembly Mnemonic	Assembly Syntax		Description	# of Words	# of Cycles(2)	Status Flags Affected
25	DAW	DAW	Wn	Wn = decimal adjust Wn	1	1	C
26	DEC	DEC	f	f = f – 1	1	1	C,DC,N,OV,Z
		DEC	f,WREG	WREG = f – 1	1	1	C,DC,N,OV,Z
		DEC	Ws,Wd	Wd = Ws – 1	1	1	C,DC,N,OV,Z
27	DEC2	DEC2	f	f = f – 2	1	1	C,DC,N,OV,Z
		DEC2	f,WREG	WREG = f – 2	1	1	C,DC,N,OV,Z
		DEC2	Ws,Wd	Wd = Ws – 2	1	1	C,DC,N,OV,Z
28	DISI	DISI	#lit14	Disable Interrupts for k instruction cycles	1	1	None
29	DIV	DIV.S	Wm,Wn	Signed 16/16-bit Integer Divide	1	18	N,Z,C,OV
		DIV.SD	Wm,Wn	Signed 32/16-bit Integer Divide	1	18	N,Z,C,OV
		DIV.U	Wm,Wn	Unsigned 16/16-bit Integer Divide	1	18	N,Z,C,OV
		DIV.UD	Wm,Wn	Unsigned 32/16-bit Integer Divide	1	18	N,Z,C,OV
30	DIVF	DIVF	Wm,Wn(1)	Signed 16/16-bit Fractional Divide	1	18	N,Z,C,OV
31	DO	DO	#lit15,Expr(1)	Do code to PC + Expr, lit15 + 1 times	2	2	None
		DO	Wn,Expr(1)	Do code to PC + Expr, (Wn) + 1 times	2	2	None
32	ED	ED	Wm*Wm,Acc,Wx,Wy,Wxd(1)	Euclidean Distance (no accumulate)	1	1	OA,OB,OAB, SA,SB,SAB
33	EDAC	EDAC	Wm*Wm,Acc,Wx,Wy,Wxd(1)	Euclidean Distance	1	1	OA,OB,OAB, SA,SB,SAB
34	EXCH	EXCH	Wns,Wnd	Swap Wns with Wnd	1	1	None
35	FBCL	FBCL	Ws,Wnd	Find Bit Change from Left (MSb) Side	1	1	C
36	FF1L	FF1L	Ws,Wnd	Find First One from Left (MSb) Side	1	1	C
37	FF1R	FF1R	Ws,Wnd	Find First One from Right (LSb) Side	1	1	C
38	GOTO	GOTO	Expr	Go to address	2	4	None
		GOTO	Wn	Go to indirect	1	4	None
		GOTO.L	Wn	Go to indirect (long address)	1	4	None
39	INC	INC	f	f = f + 1	1	1	C,DC,N,OV,Z
		INC	f,WREG	WREG = f + 1	1	1	C,DC,N,OV,Z
		INC	Ws,Wd	Wd = Ws + 1	1	1	C,DC,N,OV,Z
40	INC2	INC2	f	f = f + 2	1	1	C,DC,N,OV,Z
		INC2	f,WREG	WREG = f + 2	1	1	C,DC,N,OV,Z
		INC2	Ws,Wd	Wd = Ws + 2	1	1	C,DC,N,OV,Z
41	IOR	IOR	f	f = f .IOR. WREG	1	1	N,Z
		IOR	f,WREG	WREG = f .IOR. WREG	1	1	N,Z
		IOR	#lit10,Wn	Wd = lit10 .IOR. Wd	1	1	N,Z
		IOR	Wb,Ws,Wd	Wd = Wb .IOR. Ws	1	1	N,Z
		IOR	Wb,#lit5,Wd	Wd = Wb .IOR. lit5	1	1	N,Z
42	LAC	LAC	Wso,#Slit4,Acc	Load Accumulator	1	1	OA,OB,OAB, SA,SB,SAB
43	LNK	LNK	#lit14	Link Frame Pointer	1	1	SFA
44	LSR	LSR	f	f = Logical Right Shift f	1	1	C,N,OV,Z
		LSR	f,WREG	WREG = Logical Right Shift f	1	1	C,N,OV,Z
		LSR	Ws,Wd	Wd = Logical Right Shift Ws	1	1	C,N,OV,Z
		LSR	Wb,Wns,Wnd	Wnd = Logical Right Shift Wb by Wns	1	1	N,Z
		LSR	Wb,#lit5,Wnd	Wnd = Logical Right Shift Wb by lit5	1	1	N,Z
45	MAC	MAC	Wm*Wn,Acc,Wx,Wxd,Wy,Wyd,AWB(1)	Multiply and Accumulate	1	1	OA,OB,OAB, SA,SB,SAB
		MAC	Wm*Wm,Acc,Wx,Wxd,Wy,Wyd(1)	Square and Accumulate	1	1	OA,OB,OAB, SA,SB,SAB

Note 1: These instructions are available in dsPIC33EPXXXMC20X/50X and PIC24EPXXXMC20X devices only.

2: Read and Read-Modify-Write (e.g., bit operations and logical operations) on non-CPU SFRs incur an additional instruction cycle.

TABLE 30-39: SPI2 SLAVE MODE (FULL-DUPLEX, CKE = 0, CKP = 1, SMP = 0) TIMING REQUIREMENTS

AC CHARACTERISTICS			Standard Operating Conditions: 3.0V to 3.6V (unless otherwise stated) Operating temperature -40°C ≤ TA ≤ +85°C for Industrial -40°C ≤ TA ≤ +125°C for Extended				
Param.	**Symbol**	**Characteristic(1)**	**Min.**	**Typ.(2)**	**Max.**	**Units**	**Conditions**
SP70	FscP	Maximum SCK2 Input Frequency	—	—	15	MHz	**(Note 3)**
SP72	TscF	SCK2 Input Fall Time	—	—	—	ns	See Parameter DO32 **(Note 4)**
SP73	TscR	SCK2 Input Rise Time	—	—	—	ns	See Parameter DO31 **(Note 4)**
SP30	TdoF	SDO2 Data Output Fall Time	—	—	—	ns	See Parameter DO32 **(Note 4)**
SP31	TdoR	SDO2 Data Output Rise Time	—	—	—	ns	See Parameter DO31 **(Note 4)**
SP35	TscH2doV, TscL2doV	SDO2 Data Output Valid after SCK2 Edge	—	6	20	ns	
SP36	TdoV2scH, TdoV2scL	SDO2 Data Output Setup to First SCK2 Edge	30	—	—	ns	
SP40	TdiV2scH, TdiV2scL	Setup Time of SDI2 Data Input to SCK2 Edge	30	—	—	ns	
SP41	TscH2diL, TscL2diL	Hold Time of SDI2 Data Input to SCK2 Edge	30	—	—	ns	
SP50	TssL2scH, TssL2scL	$\overline{SS2}$ ↓ to SCK2 ↑ or SCK2 ↓ Input	120	—	—	ns	
SP51	TssH2doZ	$\overline{SS2}$ ↑ to SDO2 Output High-Impedance	10	—	50	ns	**(Note 4)**
SP52	TscH2ssH TscL2ssH	$\overline{SS2}$ ↑ after SCK2 Edge	1.5 TCY + 40	—	—	ns	**(Note 4)**

Note 1: These parameters are characterized, but are not tested in manufacturing.

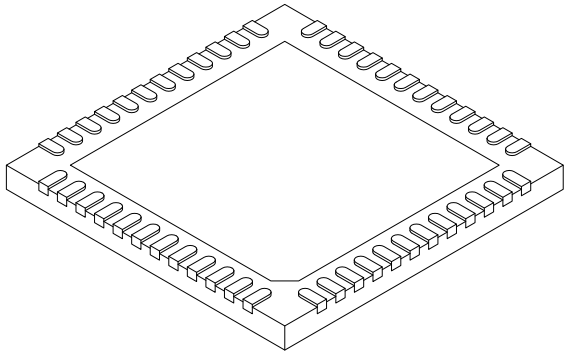
2: Data in "Typical" column is at 3.3V, +25°C unless otherwise stated.

3: The minimum clock period for SCK2 is 66.7 ns. Therefore, the SCK2 clock generated by the master must not violate this specification.

4: Assumes 50 pF load on all SPI2 pins.

48-Lead Plastic Ultra Thin Quad Flat, No Lead Package (MV) – 6x6x0.5 mm Body [UQFN]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Number of Pins	N		48	
Pitch	e		0.40 BSC	
Overall Height	A	0.45	0.50	0.55
Standoff	A1	0.00	0.02	0.05
Contact Thickness	A3		0.127 REF	
Overall Width	E		6.00 BSC	
Exposed Pad Width	E2	4.45	4.60	4.75
Overall Length	D		6.00 BSC	
Exposed Pad Length	D2	4.45	4.60	4.75
Contact Width	b	0.15	0.20	0.25
Contact Length	L	0.30	0.40	0.50
Contact-to-Exposed Pad	K	0.20	-	-

Notes:

1. Pin 1 visual index feature may vary, but must be located within the hatched area.
2. Package is saw singulated.
3. Dimensioning and tolerancing per ASME Y14.5M.

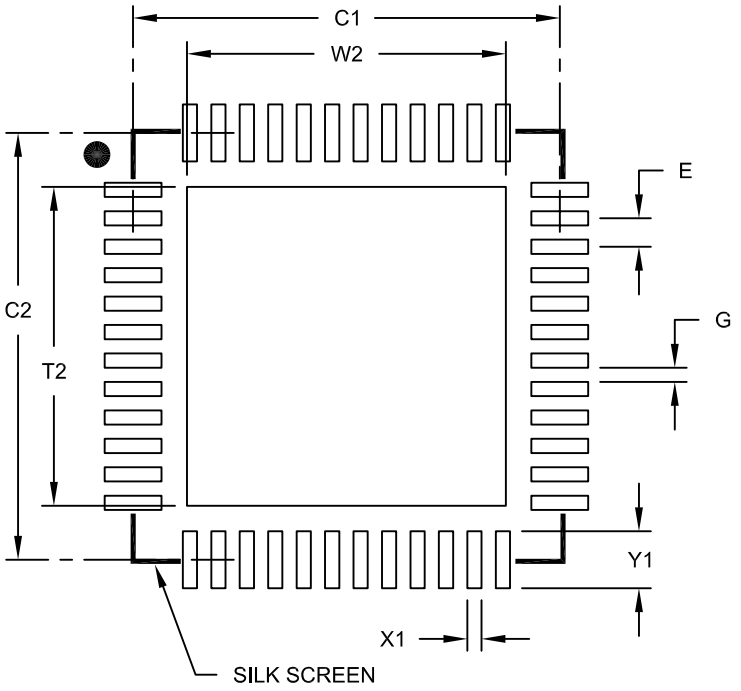
   BSC: Basic Dimension. Theoretically exact value shown without tolerances.

   REF: Reference Dimension, usually without tolerance, for information purposes only.

Microchip Technology Drawing C04-153A Sheet 2 of 2

48-Lead Ultra Thin Plastic Quad Flat, No Lead Package (MV) - 6x6 mm Body [UQFN]
With 0.40 mm Contact Length

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



RECOMMENDED LAND PATTERN

Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Contact Pitch	E		0.40 BSC	
Optional Center Pad Width	W2			4.45
Optional Center Pad Length	T2			4.45
Contact Pad Spacing	C1		6.00	
Contact Pad Spacing	C2		6.00	
Contact Pad Width (X28)	X1			0.20
Contact Pad Length (X28)	Y1			0.80
Distance Between Pads	G	0.20		

Notes:

1. Dimensioning and tolerancing per ASME Y14.5M

BSC: Basic Dimension. Theoretically exact value shown without tolerances.

Microchip Technology Drawing No. C04-2153A