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Details

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Product Status	Active
Core Processor	PIC
Core Size	16-Bit
Speed	70 MIPs
Connectivity	I ² C, IrDA, LINbus, QEI, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, DMA, Motor Control PWM, POR, PWM, WDT
Number of I/O	35
Program Memory Size	256КВ (85.5К х 24)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	16K x 16
Voltage - Supply (Vcc/Vdd)	3V ~ 3.6V
Data Converters	A/D 9x10b/12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	44-VQFN Exposed Pad
Supplier Device Package	44-QFN (8x8)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/pic24ep256mc204t-i-ml

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TABLE 4-3: INTERRUPT CONTROLLER REGISTER MAP FOR PIC24EPXXXGP20X DEVICES ONLY

File Name	Addr.	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	All Resets
IFS0	0800	—	DMA1IF	AD1IF	U1TXIF	U1RXIF	SPI1IF	SPI1EIF	T3IF	T2IF	OC2IF	IC2IF	DMA0IF	T1IF	OC1IF	IC1IF	INT0IF	0000
IFS1	0802	U2TXIF	U2RXIF	INT2IF	T5IF	T4IF	OC4IF	OC3IF	DMA2IF	-	—	_	INT1IF	CNIF	CMIF	MI2C1IF	SI2C1IF	0000
IFS2	0804	—	—	—		—	_	_	_		IC4IF	IC3IF	DMA3IF	_	—	SPI2IF	SPI2EIF	0000
IFS3	0806	—	—	—		—	—	_	_		—	—	_	—	MI2C2IF	SI2C2IF	—	0000
IFS4	0808	_	_	CTMUIF		_	_	_	_		_	_	—	CRCIF	U2EIF	U1EIF	_	0000
IFS8	0810	JTAGIF	ICDIF	—	_	—	—	—	—	_	—	—	—	—	—	—	—	0000
IFS9	0812	—	—	—	_	—	—	—	—	_	PTG3IF	PTG2IF	PTG1IF	PTG0IF	PTGWDTIF	PTGSTEPIF	—	0000
IEC0	0820	—	DMA1IE	AD1IE	U1TXIE	U1RXIE	SPI1IE	SPI1EIE	T3IE	T2IE	OC2IE	IC2IE	DMA0IE	T1IE	OC1IE	IC1IE	INT0IE	0000
IEC1	0822	U2TXIE	U2RXIE	INT2IE	T5IE	T4IE	OC4IE	OC3IE	DMA2IE	_	—	—	INT1IE	CNIE	CMIE	MI2C1IE	SI2C1IE	0000
IEC2	0824	—	—	—	_	—	—	—	—	_	IC4IE	IC3IE	DMA3IE	—	—	SPI2IE	SPI2EIE	0000
IEC3	0826	—	—	—	_	—	—	—	—		—	_	—	—	MI2C2IE	SI2C2IE	—	0000
IEC4	0828	—	—	CTMUIE	_	—	—	—	—	_	—	—	—	CRCIE	U2EIE	U1EIE	—	0000
IEC8	0830	JTAGIE	ICDIE	—	_	—	—	—	—		—	_	—	—	—	—	—	0000
IEC9	0832	—	—	—	_	—	—	—	_	_	PTG3IE	PTG2IE	PTG1IE	PTG0IE	PTGWDTIE	PTGSTEPIE	—	0000
IPC0	0840	—		T1IP<2:0>		—		OC1IP<2:0)>	_		IC1IP<2:0>		—		INT0IP<2:0>		4444
IPC1	0842	—		T2IP<2:0>		—		OC2IP<2:0)>			IC2IP<2:0>		—	0	0MA0IP<2:0>		4444
IPC2	0844	—	ι	J1RXIP<2:0	>	—	:	SPI1IP<2:0)>	_		SPI1EIP<2:0	>	—		T3IP<2:0>		4444
IPC3	0846	—	—	—	—	—	0)MA1IP<2:	0>			AD1IP<2:0>	•	—	ι	J1TXIP<2:0>		0444
IPC4	0848	—		CNIP<2:0>		—		CMIP<2:0	>	_		MI2C1IP<2:0	>	—	5	SI2C1IP<2:0>		4444
IPC5	084A	—	—	—	_	—	—	—	—	_	—	—	—	—		INT1IP<2:0>		0004
IPC6	084C	—		T4IP<2:0>		—		OC4IP<2:0)>	_		OC3IP<2:0>	•	—	0	0MA2IP<2:0>		4444
IPC7	084E	—	l	J2TXIP<2:0	>	—	ι	J2RXIP<2:	0>	_		INT2IP<2:0>	>	—		T5IP<2:0>		4444
IPC8	0850	—	—	—	_	—	—	—	—	_		SPI2IP<2:0>	>	—	S	SPI2EIP<2:0>		0044
IPC9	0852	—	—	—	_	—		IC4IP<2:0	>	_		IC3IP<2:0>		—	0	0MA3IP<2:0>		0444
IPC12	0858	—	—	—	_	—	N	112C2IP<2:	0>	_		SI2C2IP<2:0	>	—	—	—	—	0440
IPC16	0860	—		CRCIP<2:0	>	—		U2EIP<2:0	>	_		U1EIP<2:0>		—	—	—	—	4440
IPC19	0866	—	—	—	_	—	—	—	—	_		CTMUIP<2:0	>	—	—	—	—	0040
IPC35	0886	—		JTAGIP<2:0	>	—		ICDIP<2:0	>	_	—	—	—	—	—	—	—	4400
IPC36	0888	—	F	PTG0IP<2:0	>	—	PT	GWDTIP<	2:0>	_	P	TGSTEPIP<2	2:0>	—	—	—	—	4440
IPC37	088A	—	—	—		—	F	PTG3IP<2:	0>			PTG2IP<2:0	>	—	F	PTG1IP<2:0>		0444
INTCON1	08C0	NSTDIS	OVAERR	OVBERR	_	—	—	—	—	_	DIV0ERR	DMACERR	MATHERR	ADDRERR	STKERR	OSCFAIL	—	0000
INTCON2	08C2	GIE	DISI	SWTRAP	_	—	_	—	—	_	—	_	_	—	INT2EP	INT1EP	INT0EP	8000
INTCON3	08C4	_	—	—	_	—	_	—	—	_	—	DAE	DOOVR	—	_	—	—	0000
INTCON4	08C6	—	—	—	—	—	—	—	—	_	—	—	—	—	—	—	SGHT	0000
INTTREG	08C8	_	_	_	—		ILR<	3:0>			VECNU		JM<7:0>	:0>			0000	

- = unimplemented, read as '0'. Reset values are shown in hexadecimal. Legend:

TABLE 4-5: INTERRUPT CONTROLLER REGISTER MAP FOR dsPIC33EPXXXGP50X DEVICES ONLY (CONTINUED)

File Name	Addr.	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	All Resets
INTCON1	08C0	NSTDIS	OVAERR	OVBERR	COVAERR	COVBERR	OVATE	OVBTE	COVTE	SFTACERR	DIV0ERR	DMACERR	MATHERR	ADDRERR	STKERR	OSCFAIL		0000
INTCON2	08C2	GIE	DISI	SWTRAP	_	_		_	_	_	_	_	_	_	INT2EP	INT1EP	INT0EP	8000
INTCON3	08C4	_	_	_	_	_		_	_	_	_	DAE	DOOVR	_	_	_	_	0000
INTCON4	08C6					_	_			_				_	—		SGHT	0000
INTTREG	08C8						ILR<	3:0>					VECNU	M<7:0>				0000

Legend: — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

TABLE 4	4-31:	PER	IPHERA	L PIN S	ELECT	INPUT F	REGISTI	ER MAP	FOR ds	sPIC33E	PXXXG	P50X D	EVICES	3 ONLY	

File Name	Addr.	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	All Resets
RPINR0	06A0	—				INT1R<6:0>					—	—	—	—	_			0000
RPINR1	06A2		_			_	_		—					INT2R<6:0>				0000
RPINR3	06A6		_			_	_		—				-	T2CKR<6:0>	>			0000
RPINR7	06AE			IC2R<6:0>										IC1R<6:0>				0000
RPINR8	06B0	_		IC4R<6:0>						_	IC3R<6:0>							0000
RPINR11	06B6	_	_	_	_	_	-	_	_	_	OCFAR<6:0>							0000
RPINR18	06C4	_	_	_	_	_	-	_	_	_			l	J1RXR<6:0	>			0000
RPINR19	06C6	_	_	_	_	_	-	_	_	_			l	J2RXR<6:0	>			0000
RPINR22	06CC	_	SCK2INR<6:0>							_				SDI2R<6:0>				0000
RPINR23	06CE	_	_	_	_	_	-	_	_	_	– SS2R<6:0> 0					0000		
RPINR26	06D4	_	_	_		_	—		_		– C1RXR<6:0>					0000		

Legend: - = unimplemented, read as '0'. Reset values are shown in hexadecimal.

TABLE 4-32: PERIPHERAL PIN SELECT INPUT REGISTER MAP FOR dsPIC33EPXXXMC50X DEVICES ONLY

File Name	Addr.	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	All Resets
RPINR0	06A0	—				INT1R<6:0>	>			_	—	—	—			_	_	0000
RPINR1	06A2	_	_	_	_	_	_	_	_	_				INT2R<6:0>				0000
RPINR3	06A6	_	_	_	_	_	_	_	_	_			-	T2CKR<6:0>	>			0000
RPINR7	06AE	_				IC2R<6:0>				_				IC1R<6:0>				0000
RPINR8	06B0	_				IC4R<6:0>				_				IC3R<6:0>				0000
RPINR11	06B6	_	_	_	_	_	_	_	_	- OCFAR<6:0>						0000		
RPINR12	06B8	_				FLT2R<6:0>	>			_				FLT1R<6:0>	•			0000
RPINR14	06BC	_			(QEB1R<6:0	>			_			(QEA1R<6:0	>			0000
RPINR15	06BE	_			Н	OME1R<6:()>			_	INDX1R<6:0>						0000	
RPINR18	06C4	_	_	_	_	_	_	_	_	_	U1RXR<6:0>						0000	
RPINR19	06C6	_	_	_	_	_	_	_	_	_			ι	J2RXR<6:0	>			0000
RPINR22	06CC	_			S	CK2INR<6:	0>			_				SDI2R<6:0>				0000
RPINR23	06CE	_	_	_	_	_	-	_	_	_				SS2R<6:0>				0000
RPINR26	06D4	_	_	_	_	_	_	_	_	_			(C1RXR<6:0	>			0000
RPINR37	06EA	_	SYNCI1R<6:0>					_						0000				
RPINR38	06EC	—			D	CMP1R<6	:0>			—						0000		
RPINR39	06EE	_	DTCMP3R<6:0>						_	DTCMP2R<6:0>					0000			

Legend: - = unimplemented, read as '0'. Reset values are shown in hexadecimal.

dsPIC33EPXXXGP50X, dsPIC33EPXXXMC20X/50X AND PIC24EPXXXGP/MC20X

Allocating different Page registers for read and write access allows the architecture to support data movement between different pages in data memory. This is accomplished by setting the DSRPAG register value to the page from which you want to read, and configuring the DSWPAG register to the page to which it needs to be written. Data can also be moved from different PSV to EDS pages, by configuring the DSRPAG and DSWPAG registers to address PSV and EDS space, respectively. The data can be moved between pages by a single instruction.

When an EDS or PSV page overflow or underflow occurs, EA<15> is cleared as a result of the register indirect EA calculation. An overflow or underflow of the EA in the EDS or PSV pages can occur at the page boundaries when:

- The initial address prior to modification addresses an EDS or PSV page
- The EA calculation uses Pre-Modified or Post-Modified Register Indirect Addressing; however, this does not include Register Offset Addressing

In general, when an overflow is detected, the DSxPAG register is incremented and the EA<15> bit is set to keep the base address within the EDS or PSV window. When an underflow is detected, the DSxPAG register is decremented and the EA<15> bit is set to keep the base address within the EDS or PSV window. This creates a linear EDS and PSV address space, but only when using Register Indirect Addressing modes.

Exceptions to the operation described above arise when entering and exiting the boundaries of Page 0, EDS and PSV spaces. Table 4-61 lists the effects of overflow and underflow scenarios at different boundaries.

In the following cases, when overflow or underflow occurs, the EA<15> bit is set and the DSxPAG is not modified; therefore, the EA will wrap to the beginning of the current page:

- · Register Indirect with Register Offset Addressing
- Modulo Addressing
- · Bit-Reversed Addressing

			Before			After	
0/U, R/W	Operation	DSxPAG	DS EA<15>	Page Description	DSxPAG	DS EA<15>	Page Description
O, Read		DSRPAG = 0x1FF	1	EDS: Last page	DSRPAG = 0x1FF	0	See Note 1
O, Read	[++\Wn]	DSRPAG = 0x2FF	1	PSV: Last lsw page	DSRPAG = 0x300	1	PSV: First MSB page
O, Read	[Wn++]	DSRPAG = 0x3FF	1	PSV: Last MSB page	DSRPAG = 0x3FF	0	See Note 1
O, Write		DSWPAG = 0x1FF	1	EDS: Last page	DSWPAG = 0x1FF	0	See Note 1
U, Read		DSRPAG = 0x001	1	PSV page	DSRPAG = 0x001	0	See Note 1
U, Read	[Wn] Or	DSRPAG = 0x200 1 PS\ pag		PSV: First Isw page	DSRPAG = 0x200	0	See Note 1
U, Read	[WII —]	DSRPAG = 0x300	1	PSV: First MSB page	DSRPAG = 0x2FF	1	PSV: Last Isw page

TABLE 4-61: OVERFLOW AND UNDERFLOW SCENARIOS AT PAGE 0, EDS and PSV SPACE BOUNDARIES^(2,3,4)

Legend: O = Overflow, U = Underflow, R = Read, W = Write

Note 1: The Register Indirect Addressing now addresses a location in the base Data Space (0x0000-0x8000).

2: An EDS access with DSxPAG = 0x000 will generate an address error trap.

- **3:** Only reads from PS are supported using DSRPAG. An attempt to write to PS using DSWPAG will generate an address error trap.
- 4: Pseudo-Linear Addressing is not supported for large offsets.

dsPIC33EPXXXGP50X, dsPIC33EPXXXMC20X/50X AND PIC24EPXXXGP/MC20X

U-0	U-0	U-0	U-0	U-0	U-0	U-0	R/W-0
	—	_	_	_	_	_	PLLDIV8
bit 15		·					bit 8
R/W-0	R/W-0	R/W-1	R/W-1	R/W-0	R/W-0	R/W-0	R/W-0
PLLDIV7	PLLDIV6	PLLDIV5	PLLDIV4	PLLDIV3	PLLDIV2	PLLDIV1	PLLDIV0
bit 7		·					bit 0
Legend:							
R = Readable	bit	W = Writable	bit	U = Unimpler	mented bit, read	l as '0'	
-n = Value at F	POR	'1' = Bit is set		'0' = Bit is cle	ared	x = Bit is unki	nown
bit 15-9	Unimplemen	ted: Read as '	0'				
bit 8-0	PLLDIV<8:0	>: PLL Feedba	ck Divisor bits	(also denoted	as 'M', PLL mu	ltiplier)	
	111111111	= 513					
	•						
	•						
	•						
	000110000:	= 50 (default)					
	•						
	•						
	•						
	00000010:	= 4					
	000000001	= 3 = 2					
	0000000000000	-					

REGISTER 9-3: PLLFBD: PLL FEEDBACK DIVISOR REGISTER

NOTES:

16.0 HIGH-SPEED PWM MODULE (dsPIC33EPXXXMC20X/50X AND PIC24EPXXXMC20X DEVICES ONLY)

- Note 1: This data sheet summarizes the features of the dsPIC33EPXXXGP50X, dsPIC33EPXXXMC20X/50X and PIC24EPXXXGP/MC20X families of devices. It is not intended to be a comprehensive reference source. To complement the information in this data sheet, refer to "High-Speed PWM" (DS70645) in the "dsPIC33/PIC24 Family Reference Manual", which is available from the Microchip web site (www.microchip.com).
 - Some registers and associated bits described in this section may not be available on all devices. Refer to Section 4.0 "Memory Organization" in this data sheet for device-specific register and bit information.

The dsPIC33EPXXXMC20X/50X and PIC24EPXXXMC20X devices support a dedicated Pulse-Width Modulation (PWM) module with up to 6 outputs.

The high-speed PWMx module consists of the following major features:

- Three PWM generators
- Two PWM outputs per PWM generator
- Individual period and duty cycle for each PWM pair
- Duty cycle, dead time, phase shift and frequency resolution of Tcy/2 (7.14 ns at Fcy = 70MHz)
- Independent Fault and current-limit inputs for six PWM outputs
- · Redundant output
- Center-Aligned PWM mode
- Output override control
- Chop mode (also known as Gated mode)
- Special Event Trigger
- Prescaler for input clock
- PWMxL and PWMxH output pin swapping
- Independent PWM frequency, duty cycle and phase-shift changes for each PWM generator
- Dead-time compensation
- Enhanced Leading-Edge Blanking (LEB) functionality
- Frequency resolution enhancement
- PWM capture functionality

Note: In Edge-Aligned PWM mode, the duty cycle, dead time, phase shift and frequency resolution are 8.32 ns.

The high-speed PWMx module contains up to three PWM generators. Each PWM generator provides two PWM outputs: PWMxH and PWMxL. The master time base generator provides a synchronous signal as a common time base to synchronize the various PWM outputs. The individual PWM outputs are available on the output pins of the device. The input Fault signals and current-limit signals, when enabled, can monitor and protect the system by placing the PWM outputs into a known "safe" state.

Each PWMx can generate a trigger to the ADC module to sample the analog signal at a specific instance during the PWM period. In addition, the high-speed PWMx module also generates a Special Event Trigger to the ADC module based on either of the two master time bases.

The high-speed PWMx module can synchronize itself with an external signal or can act as a synchronizing source to any external device. The SYNCI1 input pin that utilizes PPS, can synchronize the high-speed PWMx module with an external signal. The SYNC01 pin is an output pin that provides a synchronous signal to an external device.

Figure 16-1 illustrates an architectural overview of the high-speed PWMx module and its interconnection with the CPU and other peripherals.

16.1 PWM Faults

The PWMx module incorporates multiple external Fault inputs to include FLT1 and FLT2 which are remappable using the PPS feature, FLT3 and FLT4 which are available only on the larger 44-pin and 64-pin packages, and FLT32 which has been implemented with Class B safety features, and is available on a fixed pin on all dsPIC33EPXXXMC20X/50X and PIC24EPXXXMC20X devices.

These Faults provide a safe and reliable way to safely shut down the PWM outputs when the Fault input is asserted.

16.1.1 PWM FAULTS AT RESET

During any Reset event, the PWMx module maintains ownership of the Class B Fault, FLT32. At Reset, this Fault is enabled in Latched mode to ensure the fail-safe power-up of the application. The application software must clear the PWM Fault before enabling the highspeed motor control PWMx module. To clear the Fault condition, the FLT32 pin must first be pulled low externally or the internal pull-down resistor in the CNPDx register can be enabled.

Note: The Fault mode may be changed using the FLTMOD<1:0> bits (FCLCON<1:0>), regardless of the state of FLT32.

REGISTER 16-1: PTCON: PWMx TIME BASE CONTROL REGISTER (CONTINUED)

bit 6-4	SYNCSRC<2:0>: Synchronous Source Selection bits ⁽¹⁾ 111 = Reserved
	•
	• 100 = Reserved 011 = PTGO17 ⁽²⁾ 010 = PTGO16 ⁽²⁾ 001 = Reserved 000 = SYNCI1 input from PPS
bit 3-0	<pre>SEVTPS<3:0>: PWMx Special Event Trigger Output Postscaler Select bits⁽¹⁾ 1111 = 1:16 Postscaler generates Special Event Trigger on every sixteenth compare match event</pre>
	0001 = 1:2 Postscaler generates Special Event Trigger on every second compare match event 0000 = 1:1 Postscaler generates Special Event Trigger on every compare match event

- **Note 1:** These bits should be changed only when PTEN = 0. In addition, when using the SYNCI1 feature, the user application must program the period register with a value that is slightly larger than the expected period of the external synchronization input signal.
 - 2: See Section 24.0 "Peripheral Trigger Generator (PTG) Module" for information on this selection.

dsPIC33EPXXXGP50X, dsPIC33EPXXXMC20X/50X AND PIC24EPXXXGP/MC20X

R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1
			PTPE	R<15:8>			
bit 15							bit 8
R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-0	R/W-0	R/W-0
			PTPE	:R<7:0>			
bit 7							bit 0
Legend:							
R = Readable I	bit	W = Writable bi	t	U = Unimpler	mented bit, read	d as '0'	

'0' = Bit is cleared

x = Bit is unknown

REGISTER 16-3: PTPER: PWMx PRIMARY MASTER TIME BASE PERIOD REGISTER

bit 15-0 **PTPER<15:0>:** Primary Master Time Base (PMTMR) Period Value bits

'1' = Bit is set

REGISTER 16-4: SEVTCMP: PWMx PRIMARY SPECIAL EVENT COMPARE REGISTER

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
			SEVTO	CMP<15:8>			
bit 15							bit 8
R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
			SEVT	CMP<7:0>			
bit 7							bit 0
Legend:							
R = Readable	bit	W = Writable b	it	U = Unimpler	mented bit, rea	ad as '0'	
-n = Value at F	POR	'1' = Bit is set		'0' = Bit is cle	ared	x = Bit is unkı	nown

bit 15-0 SEVTCMP<15:0>: Special Event Compare Count Value bits

-n = Value at POR

HS/HC-	0 HS/HC-0	HS/HC-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
FLTSTAT	-(1) CLSTAT ⁽¹⁾	TRGSTAT	FLTIEN	CLIEN	TRGIEN	ITB ⁽²⁾	MDCS ⁽²⁾
bit 15							bit 8
R/W-0	R/W-0	R/W-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0
DTC1	DTC0	DTCP ⁽³⁾	<u> </u>	MTBS	CAM ^(2,4)	XPRES ⁽⁵⁾	IUE ⁽²⁾
bit 7							bit 0
Legend:		HC = Hardware	Clearable bit	HS = Hardwa	are Settable bit		
R = Reada	able bit	W = Writable bi	t	U = Unimplei	mented bit, rea	d as '0'	
-n = Value	at POR	'1' = Bit is set		'0' = Bit is cle	eared	x = Bit is unk	nown
bit 15	FLTSTAT: Fai 1 = Fault inter 0 = No Fault i This bit is clea	ult Interrupt Statu rrupt is pending interrupt is pendi	us bit ⁽¹⁾ ng LTIEN = 0				
hit 14	CI STAT. Cur	rent-l imit Interru	nt Status hit(1)				
	1 = Current-lin 0 = No curren This bit is clea	mit interrupt is pentitienter interrupt is pentitienter interrupt is ared by setting C	ending s pending CLIEN = 0.				
bit 13	TRGSTAT: Tr	igger Interrupt S	tatus bit				
	1 = Trigger in 0 = No trigger This bit is clea	terrupt is pending r interrupt is pend ared by setting T	g ding RGIEN = 0.				
bit 12	FLTIEN: Faul	t Interrupt Enabl	e bit				
	1 = Fault inter 0 = Fault inter	rrupt is enabled rrupt is disabled	and the FLTST	AT bit is cleare	ed		
bit 11	CLIEN: Curre	ent-Limit Interrup	t Enable bit				
	1 = Current-lii 0 = Current-lii	mit interrupt is er mit interrupt is di	nabled sabled and the	CLSTAT bit is	cleared		
bit 10	TRGIEN: Trig	ger Interrupt Ena	able bit				
	1 = A trigger e 0 = Trigger ev	event generates /ent interrupts ar	an interrupt rec	quest the TRGSTAT	bit is cleared		
bit 9	ITB: Independ	dent Time Base	Mode bit ⁽²⁾				
	1 = PHASEx (0 = PTPER re	register provides egister provides f	time base peri timing for this F	iod for this PW WM generato	/M generator r		
bit 8	MDCS: Maste	er Duty Cycle Re	gister Select bi	it(2)			
	1 = MDC regi 0 = PDCx reg	ster provides du ister provides du	ty cycle informa ity cycle inform	ation for this P ation for this F	WM generator WM generator		
Note 1:	Software must clea	ar the interrupt st	atus here and	in the correspo	onding IFSx bit	in the interrup	ot controller.
2:	These bits should	not be changed	after the PWM	, is enabled (P	PTEN = 1).	•	
3:	DTC<1:0> = 11 for	r DTCP to be effe	ective; otherwis	se, DTCP is ig	nored.		
4:	The Independent T CAM bit is ignored	Time Base (ITB =	1) mode must	be enabled to	use Center-Ali	igned mode. If	TTB = 0, the
-	T		· · · · · · · · · · · · · · · · · · ·				

REGISTER 16-7: PWMCONx: PWMx CONTROL REGISTER

5: To operate in External Period Reset mode, the ITB bit must be '1' and the CLMOD bit in the FCLCONx register must be '0'.

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REGISTER 16-8: PDCx: PWMx GENERATOR DUTY CYCLE REGISTER

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
			PDC	x<15:8>			
bit 15							bit 8
R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
			PDC	x<7:0>			
bit 7							bit 0
Legend:							
R = Readable bit W = Writable bit			bit	U = Unimplemented bit, read as '0'			
-n = Value at POR '1' = Bit is		'1' = Bit is set		'0' = Bit is cle	ared	x = Bit is unkr	nown

bit 15-0 **PDCx<15:0>:** PWMx Generator # Duty Cycle Value bits

REGISTER 16-9: PHASEx: PWMx PRIMARY PHASE-SHIFT REGISTER

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	
			PHAS	Ex<15:8>				
bit 15							bit 8	
R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	
			PHAS	SEx<7:0>				
bit 7							bit 0	
Legend:								
R = Readable bit W = Writable bit			it	U = Unimplemented bit, read as '0'				
-n = Value at POR '1' = Bit is set				'0' = Bit is cle	ared	x = Bit is unkr	nown	

bit 15-0 PHASEx<15:0>: PWMx Phase-Shift Value or Independent Time Base Period for the PWM Generator bits

Note 1: If ITB (PWMCONx<9>) = 0, the following applies based on the mode of operation: Complementary, Redundant and Push-Pull Output mode (PMOD<1:0> (IOCON<11:10>) = 00, 01 or 10), PHASEx<15:0> = Phase-shift value for PWMxH and PWMxL outputs

 If ITB (PWMCONx<9>) = 1, the following applies based on the mode of operation: Complementary, Redundant and Push-Pull Output mode (PMOD<1:0> (IOCONx<11:10>) = 00, 01 or 10), PHASEx<15:0> = Independent time base period value for PWMxH and PWMxL





REGISTER 23-6: AD1CHS0: ADC1 INPUT CHANNEL 0 SELECT REGISTER (CONTINUED)

bit 4-0	CH0SA<4:0>: Channel 0 Positive Input Select for Sample MUXA bits ⁽¹⁾									
	11111 = Open; use this selection with CTMU capacitive and time measurement									
	11110 = Channel 0 positive input is connected to the CTMU temperature measurement diode (CTMU TEMP)									
	11101 - Reserved									
	11011 = Reserved									
	11010 = Channel 0 positive input is the output of OA3/AN6 ^(2,3)									
	11001 = Channel 0 positive input is the output of OA2/AN0 ⁽²⁾									
	11000 = Channel U positive input is the output of OA1/AN3 ⁽²⁾									
	•									
	•									
	•									
	10000 = Reserved									
	01111 = Channel 0 positive input is AN15 ^(1,3)									
	01110 = Channel 0 positive input is AN14 ^(1,3)									
	01101 = Channel 0 positive input is AN13 ^(1,3)									
	•									
	•									
	• (1 2)									
	00010 = Channel 0 positive input is AN2 ^(1,3)									
	00001 = Channel 0 positive input is AN1(1,3)									
	00000 = Channel 0 positive input is AN0(',3)									

- **Note 1:** AN0 through AN7 are repurposed when comparator and op amp functionality is enabled. See Figure 23-1 to determine how enabling a particular op amp or comparator affects selection choices for Channels 1, 2 and 3.
 - 2: The OAx input is used if the corresponding op amp is selected (OPMODE (CMxCON<10>) = 1); otherwise, the ANx input is used.
 - 3: See the "Pin Diagrams" section for the available analog channels for each device.

24.4 Step Commands and Format

TABLE 24-1: PTG STEP COMMAND FORMAT

Step Command Byte:						
STE	Px<7:0>					
CMD<3:0>	OPTION<3:0>					
bit 7 bit	4 bit 3 bit 0					

bit 7-4	CMD<3:0>	Step Command	Command Description
	0000	PTGCTRL	Execute control command as described by OPTION<3:0>.
	0001	PTGADD	Add contents of PTGADJ register to target register as described by OPTION<3:0>.
		PTGCOPY	Copy contents of PTGHOLD register to target register as described by OPTION<3:0>.
	001x	PTGSTRB	Copy the value contained in CMD<0>:OPTION<3:0> to the CH0SA<4:0> bits (AD1CHS0<4:0>).
	0100	PTGWHI	Wait for a low-to-high edge input from the selected PTG trigger input as described by OPTION<3:0>.
	0101	PTGWLO	Wait for a high-to-low edge input from the selected PTG trigger input as described by OPTION<3:0>.
	0110	Reserved	Reserved.
	0111	PTGIRQ	Generate individual interrupt request as described by OPTION3<:0>.
	100x	PTGTRIG	Generate individual trigger output as described by < <cmd<0>:OPTION<3:0>>.</cmd<0>
	101x	PTGJMP	Copy the value indicated in < <cmd<0>:OPTION<3:0>> to the Queue Pointer (PTGQPTR) and jump to that Step queue.</cmd<0>
	110x	PTGJMPC0	PTGC0 = PTGC0LIM: Increment the Queue Pointer (PTGQPTR).
			$PTGC0 \neq PTGC0LIM$: Increment Counter 0 (PTGC0) and copy the value indicated in < <cmd<0>:OPTION<3:0>> to the Queue Pointer (PTGQPTR), and jump to that Step queue</cmd<0>
	111x	PTGJMPC1	PTGC1 = PTGC1LIM: Increment the Queue Pointer (PTGQPTR).
			$PTGC1 \neq PTGC1LIM$: Increment Counter 1 (PTGC1) and copy the value indicated in < <cmd<0>:OPTION<3:0>> to the Queue Pointer (PTGQPTR), and jump to that Step queue.</cmd<0>

Note 1: All reserved commands or options will execute but have no effect (i.e., execute as a NOP instruction).

2: Refer to Table 24-2 for the trigger output descriptions.

3: This feature is only available on dsPIC33EPXXXMC20X/50X and PIC24EPXXXMC20X devices.

30.1 DC Characteristics

|--|

			Maximum MIPS			
Characteristic	VDD Range (in Volts)	Temp Range (in °C)	dsPIC33EPXXXGP50X, dsPIC33EPXXXMC20X/50X and PIC24EPXXXGP/MC20X			
	3.0V to 3.6V ⁽¹⁾	-40°C to +85°C	70			
—	3.0V to 3.6V ⁽¹⁾	-40°C to +125°C	60			

Note 1: Device is functional at VBORMIN < VDD < VDDMIN. Analog modules (ADC, op amp/comparator and comparator voltage reference) may have degraded performance. Device functionality is tested but not characterized. Refer to Parameter BO10 in Table 30-13 for the minimum and maximum BOR values.

TABLE 30-2: THERMAL OPERATING CONDITIONS

Rating	Symbol	Min.	Тур.	Max.	Unit
Industrial Temperature Devices					
Operating Junction Temperature Range	TJ	-40		+125	°C
Operating Ambient Temperature Range	TA	-40		+85	°C
Extended Temperature Devices					
Operating Junction Temperature Range	TJ	-40		+140	°C
Operating Ambient Temperature Range	TA	-40		+125	°C
Power Dissipation: Internal chip power dissipation: $PINT = VDD \times (IDD - \Sigma IOH)$ I/O Pin Power Dissipation:	PD		Pint + Pi/c	D	W
$I/O = \Sigma (\{VDD - VOH\} \times IOH) + \Sigma (VOL \times IOL)$					
Maximum Allowed Power Dissipation	PDMAX	(TJ — TA)/θJ	IA	W

TABLE 30-3: THERMAL PACKAGING CHARACTERISTICS

Characteristic	Symbol	Тур.	Max.	Unit	Notes
Package Thermal Resistance, 64-Pin QFN	θJA	28.0	_	°C/W	1
Package Thermal Resistance, 64-Pin TQFP 10x10 mm	θја	48.3		°C/W	1
Package Thermal Resistance, 48-Pin UQFN 6x6 mm	θја	41	-	°C/W	1
Package Thermal Resistance, 44-Pin QFN	θJA	29.0		°C/W	1
Package Thermal Resistance, 44-Pin TQFP 10x10 mm	θја	49.8		°C/W	1
Package Thermal Resistance, 44-Pin VTLA 6x6 mm	θја	25.2	_	°C/W	1
Package Thermal Resistance, 36-Pin VTLA 5x5 mm	θJA	28.5		°C/W	1
Package Thermal Resistance, 28-Pin QFN-S	θја	30.0		°C/W	1
Package Thermal Resistance, 28-Pin SSOP	θја	71.0	_	°C/W	1
Package Thermal Resistance, 28-Pin SOIC	θJA	69.7	_	°C/W	1
Package Thermal Resistance, 28-Pin SPDIP	θJA	60.0	_	°C/W	1

Note 1: Junction to ambient thermal resistance, Theta-JA (θ JA) numbers are achieved by package simulations.

DC CHARACTI	ERISTICS	$\begin{tabular}{lllllllllllllllllllllllllllllllllll$				ustrial ktended		
Parameter No.	Тур.	Max.	Units	Conditions				
Idle Current (II	dle) ⁽¹⁾							
DC40d	3	8	mA	-40°C				
DC40a	3	8	mA	+25°C	2 21/			
DC40b	3	8	mA	+85°C	5.5V	10 1011-5		
DC40c	3	8	mA	+125°C				
DC42d	6	12	mA	-40°C				
DC42a	6	12	mA	+25°C	3 3\/	20 MIPS		
DC42b	6	12	mA	+85°C	5.5 V	20 1011 3		
DC42c	6	12	mA	+125°C				
DC44d	11	18	mA	-40°C				
DC44a	11	18	mA	+25°C	3 3\/			
DC44b	11	18	mA	+85°C	5.5 V	40 1011 3		
DC44c	11	18	mA	+125°C				
DC45d	17	27	mA	-40°C				
DC45a	17	27	mA	+25°C	3 3\/	60 MIPS		
DC45b	17	27	mA	+85°C	5.5 V	00 1011-3		
DC45c	17	27	mA	+125°C				
DC46d	20	35	mA	-40°C				
DC46a	20	35	mA	+25°C	3.3V	70 MIPS		
DC46b	20	35	mA	+85°C				

TABLE 30-7: DC CHARACTERISTICS: IDLE CURRENT (lidle)

Note 1: Base Idle current (IIDLE) is measured as follows:

• CPU core is off, oscillator is configured in EC mode and external clock is active; OSC1 is driven with external square wave from rail-to-rail (EC clock overshoot/undershoot < 250 mV required)

- · CLKO is configured as an I/O input pin in the Configuration Word
- All I/O pins are configured as inputs and pulled to Vss
- $\overline{\text{MCLR}}$ = VDD, WDT and FSCM are disabled
- No peripheral modules are operating; however, every peripheral is being clocked (all PMDx bits are zeroed)
- The NVMSIDL bit (NVMCON<12>) = 1 (i.e., Flash regulator is set to standby while the device is in Idle mode)
- The VREGSF bit (RCON<11>) = 0 (i.e., Flash regulator is set to standby while the device is in Sleep mode)
- JTAG is disabled

AC CHARACTERISTICS				Standard Operating Conditions: 3.0V to 3.6V(unless otherwise stated)Operating temperature $-40^{\circ}C \le TA \le +85^{\circ}C$ for Industrial $-40^{\circ}C \le TA \le +125^{\circ}C$ for Extended					
Param No.	Symbol	Characteristic ⁽¹⁾	Min.	Typ. ⁽²⁾	Max.	Units	Conditions		
SY00	Τρυ	Power-up Period	—	400	600	μS			
SY10	Tost	Oscillator Start-up Time	_	1024 Tosc			Tosc = OSC1 period		
SY12	Twdt	Watchdog Timer Time-out Period	0.81	0.98	1.22	ms	WDTPRE = 0, WDTPOST<3:0> = 0000, using LPRC tolerances indicated in F21 (see Table 30-20) at +85°C		
			3.26	3.91	4.88	ms	WDTPRE = 1, WDTPOST<3:0> = 0000, using LPRC tolerances indicated in F21 (see Table 30-20) at +85°C		
SY13	Tioz	I/O High-Impedance from MCLR Low or Watchdog Timer Reset	0.68	0.72	1.2	μS			
SY20	TMCLR	MCLR Pulse Width (low)	2	_	_	μS			
SY30	TBOR	BOR Pulse Width (low)	1	—		μS			
SY35	TFSCM	Fail-Safe Clock Monitor Delay	—	500	900	μS	-40°C to +85°C		
SY36	TVREG	Voltage Regulator Standby-to-Active mode Transition Time		_	30	μS			
SY37	Toscdfrc	FRC Oscillator Start-up Delay	46	48	54	μS			
SY38	TOSCDLPRC	LPRC Oscillator Start-up Delay	_	_	70	μS			

TABLE 30-22:RESET, WATCHDOG TIMER, OSCILLATOR START-UP TIMER, POWER-UP TIMERTIMING REQUIREMENTS

Note 1: These parameters are characterized but not tested in manufacturing.

2: Data in "Typical" column is at 3.3V, +25°C unless otherwise stated.









FIGURE 30-38: ADC CONVERSION (10-BIT MODE) TIMING CHARACTERISTICS (CHPS<1:0> = 01, SIMSAM = 0, ASAM = 1, SSRC<2:0> = 111, SSRCG = 0, SAMC<4:0> = 00010)



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Temperature (Celsius)

70 80 90 100 110 120

TYPICAL FRC FREQUENCY @ VDD = 3.3V



-40 -30 -20 -10

0 10 20 30 40 50 60

FIGURE 32-9: