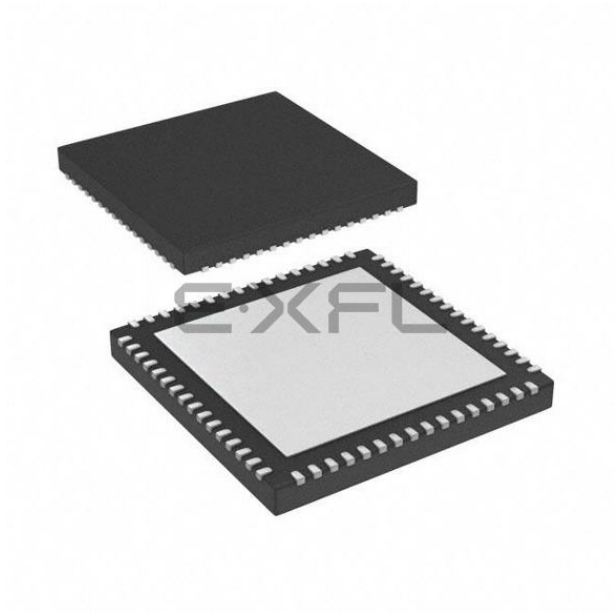

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## What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

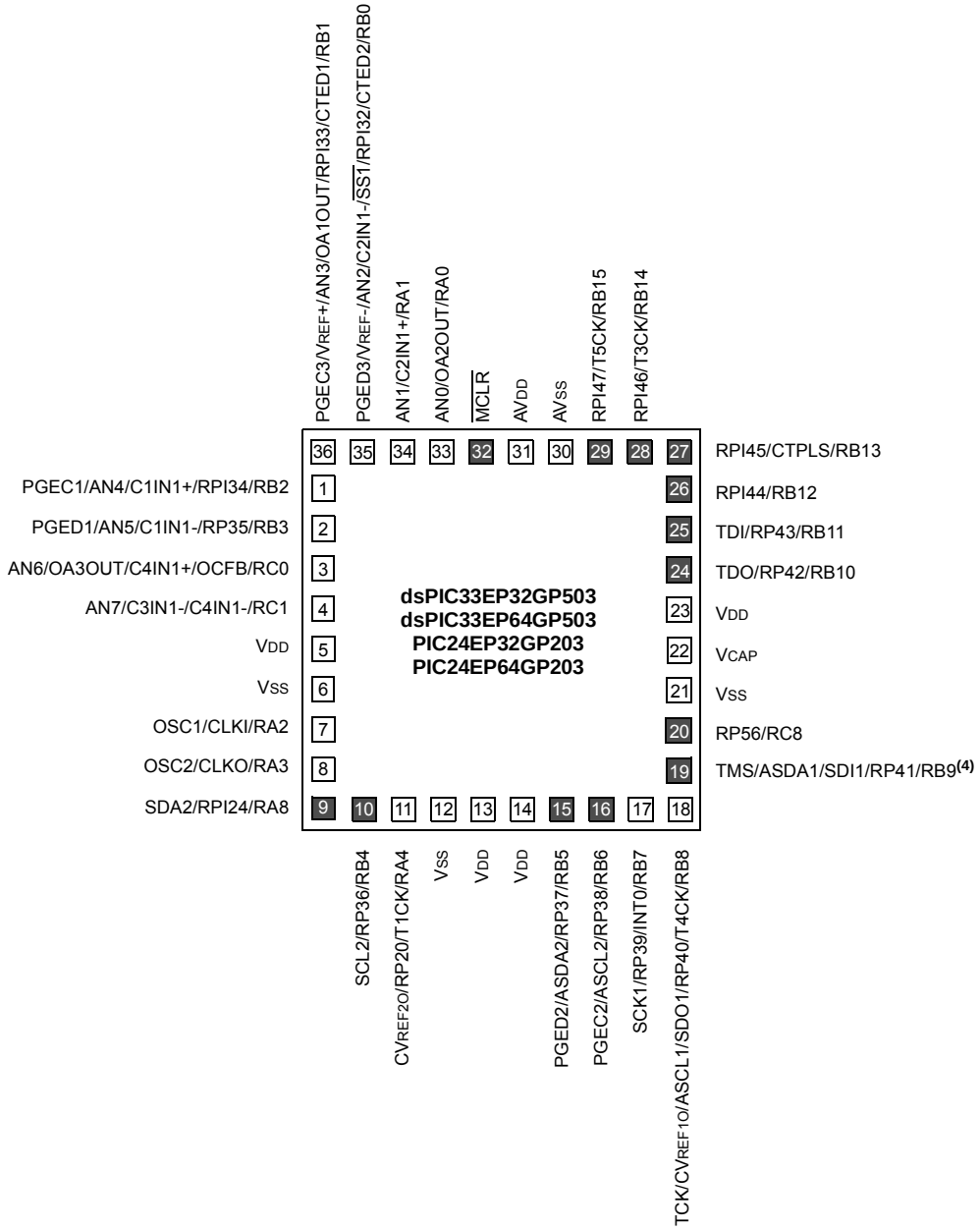
## Applications of "Embedded - Microcontrollers"

| Details | |
|---|---|
| Product Status | Obsolete |
| Core Processor | PIC |
| Core Size | 16-Bit |
| Speed | 60 MIPs |
| Connectivity | I²C, IrDA, LINbus, QEI, SPI, UART/USART |
| Peripherals | Brown-out Detect/Reset, DMA, Motor Control PWM, POR, PWM, WDT |
| Number of I/O | 53 |
| Program Memory Size | 256KB (85.5K x 24) |
| Program Memory Type | FLASH |
| EEPROM Size | - |
| RAM Size | 16K x 16 |
| Voltage - Supply (Vcc/Vdd) | 3V ~ 3.6V |
| Data Converters | A/D 16x10b/12b |
| Oscillator Type | Internal |
| Operating Temperature | -40°C ~ 125°C (TA) |
| Mounting Type | Surface Mount |
| Package / Case | 64-VFQFN Exposed Pad |
| Supplier Device Package | 64-QFN (9x9) |
| Purchase URL | https://www.e-xfl.com/product-detail/microchip-technology/pic24ep256mc206t-e-mr |

## Pin Diagrams (Continued)

**36-Pin VTLA(1,2,3)**

■ = Pins are up to 5V tolerant




**Note 1:** The RPn/RPIn pins can be used by any remappable peripheral with some limitation. See **Section 11.4 "Peripheral Pin Select (PPS)"** for available peripherals and for information on limitations.

**2:** Every I/O port pin (RAx-RGx) can be used as a Change Notification pin (CNAx-CNGx). See **Section 11.0 "I/O Ports"** for more information.

**3:** The metal pad at the bottom of the device is not connected to any pins and is recommended to be connected to VSS externally.

**4:** There is an internal pull-up resistor connected to the TMS pin when the JTAG interface is active. See the JTAGEN bit field in Table 27-2.

# 4.0 MEMORY ORGANIZATION

**Note:** This data sheet summarizes the features of the dsPIC33EPXXXGP50X, dsPIC33EPXXXMC20X/50X and PIC24EPXXXGP/MC20X families of devices. It is not intended to be a comprehensive reference source. To complement the information in this data sheet, refer to **"Program Memory"** (DS70613) in the "*dsPIC33/PIC24 Family Reference Manual*", which is available from the Microchip web site (www.microchip.com).

The dsPIC33EPXXXGP50X, dsPIC33EPXXXMC20X/50X and PIC24EPXXXGP/MC20X architecture features separate program and data memory spaces, and buses. This architecture also allows the direct access of program memory from the Data Space (DS) during code execution.

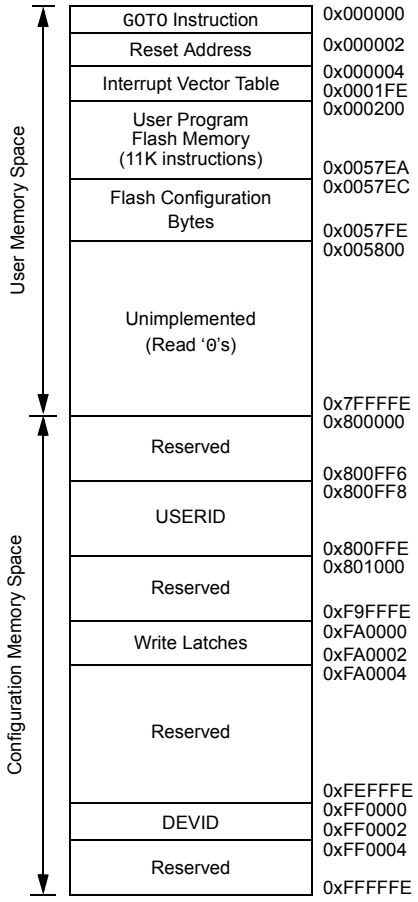
## 4.1 Program Address Space

The program address memory space of the dsPIC33EPXXXGP50X, dsPIC33EPXXXMC20X/50X and PIC24EPXXXGP/MC20X devices is 4M instructions. The space is addressable by a 24-bit value derived either from the 23-bit PC during program execution, or from table operation or Data Space remapping, as described in **Section 4.8 "Interfacing Program and Data Memory Spaces"**.

User application access to the program memory space is restricted to the lower half of the address range (0x000000 to 0x7FFFFF). The exception is the use of TBLRD operations, which use TBLPAG<7> to read Device ID sections of the configuration memory space.

The program memory maps, which are presented by device family and memory size, are shown in Figure 4-1 through Figure 4-5.

**FIGURE 4-1: PROGRAM MEMORY MAP FOR dsPIC33EP32GP50X, dsPIC33EP32MC20X/50X AND PIC24EP32GP/MC20X DEVICES**




**Note:** Memory areas are not shown to scale.

**TABLE 4-2: CPU CORE REGISTER MAP FOR PIC24EPXXXGP/MC20X DEVICES ONLY**

| File Name | Addr. | Bit 15 | Bit 14 | Bit 13 | Bit 12 | Bit 11 | Bit 10 | Bit 9 | Bit 8 | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 | All Resets |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| W0 | 0000 | W0 (WREG) | | | | | | | | | | | | | | | | xxxx |
| W1 | 0002 | W1 | | | | | | | | | | | | | | | | xxxx |
| W2 | 0004 | W2 | | | | | | | | | | | | | | | | xxxx |
| W3 | 0006 | W3 | | | | | | | | | | | | | | | | xxxx |
| W4 | 0008 | W4 | | | | | | | | | | | | | | | | xxxx |
| W5 | 000A | W5 | | | | | | | | | | | | | | | | xxxx |
| W6 | 000C | W6 | | | | | | | | | | | | | | | | xxxx |
| W7 | 000E | W7 | | | | | | | | | | | | | | | | xxxx |
| W8 | 0010 | W8 | | | | | | | | | | | | | | | | xxxx |
| W9 | 0012 | W9 | | | | | | | | | | | | | | | | xxxx |
| W10 | 0014 | W10 | | | | | | | | | | | | | | | | xxxx |
| W11 | 0016 | W11 | | | | | | | | | | | | | | | | xxxx |
| W12 | 0018 | W12 | | | | | | | | | | | | | | | | xxxx |
| W13 | 001A | W13 | | | | | | | | | | | | | | | | xxxx |
| W14 | 001C | W14 | | | | | | | | | | | | | | | | xxxx |
| W15 | 001E | W15 | | | | | | | | | | | | | | | | xxxx |
| SPLIM | 0020 | SPLIM<15:0> | | | | | | | | | | | | | | | | 0000 |
| PCL | 002E | PCL<15:1> | | | | | | | | | | | | | | | — | 0000 |
| PCH | 0030 | — | — | — | — | — | — | — | — | — | PCH<6:0> | | | | | | | 0000 |
| DSRPAG | 0032 | — | — | — | — | — | — | DSRPAG<9:0> | | | | | | | | | | 0001 |
| DSWPAG | 0034 | — | — | — | — | — | — | — | DSWPAG<8:0> | | | | | | | | | 0001 |
| RCOUNT | 0036 | RCOUNT<15:0> | | | | | | | | | | | | | | | | 0000 |
| SR | 0042 | — | — | — | — | — | — | — | DC | IPL2 | IPL1 | IPL0 | RA | N | OV | Z | C | 0000 |
| CORCON | 0044 | VAR | — | — | — | — | — | — | — | — | — | — | — | IPL3 | SFA | — | — | 0020 |
| DISICNT | 0052 | — | — | DISICNT<13:0> | | | | | | | | | | | | | | 0000 |
| TBLPAG | 0054 | — | — | — | — | — | — | — | — | TBLPAG<7:0> | | | | | | | | 0000 |
| MSTRPR | 0058 | MSTRPR<15:0> | | | | | | | | | | | | | | | | 0000 |

**Legend:** x = unknown value on Reset, — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

**TABLE 4-29: PERIPHERAL PIN SELECT INPUT REGISTER MAP FOR PIC24EPXXXMC20X DEVICES ONLY**

| File Name | Addr. | Bit 15 | Bit 14 | Bit 13 | Bit 12 | Bit 11 | Bit 10 | Bit 9 | Bit 8 | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 | All Resets |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| RPINR0 | 06A0 | — | INT1R<6:0> | | | | | | | — | — | — | — | — | — | — | — | 0000 |
| RPINR1 | 06A2 | — | — | — | — | — | — | — | — | — | INT2R<6:0> | | | | | | | 0000 |
| RPINR3 | 06A6 | — | — | — | — | — | — | — | — | — | T2CKR<6:0> | | | | | | | 0000 |
| RPINR7 | 06AE | — | IC2R<6:0> | | | | | | | — | IC1R<6:0> | | | | | | | 0000 |
| RPINR8 | 06B0 | — | IC4R<6:0> | | | | | | | — | IC3R<6:0> | | | | | | | 0000 |
| RPINR11 | 06B6 | — | — | — | — | — | — | — | — | — | OCFAR<6:0> | | | | | | | 0000 |
| RPINR12 | 06B8 | — | FLT2R<6:0> | | | | | | | — | FLT1R<6:0> | | | | | | | 0000 |
| RPINR14 | 06BC | — | QEB1R<6:0> | | | | | | | — | QEA1R<6:0> | | | | | | | 0000 |
| RPINR15 | 06BE | — | HOME1R<6:0> | | | | | | | — | INDX1R<6:0> | | | | | | | 0000 |
| RPINR18 | 06C4 | — | — | — | — | — | — | — | — | — | U1RXR<6:0> | | | | | | | 0000 |
| RPINR19 | 06C6 | — | — | — | — | — | — | — | — | — | U2RXR<6:0> | | | | | | | 0000 |
| RPINR22 | 06CC | — | SCK2INR<6:0> | | | | | | | — | SDI2R<6:0> | | | | | | | 0000 |
| RPINR23 | 06CE | — | — | — | — | — | — | — | — | — | SS2R<6:0> | | | | | | | 0000 |
| RPINR26 | 06D4 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | 0000 |
| RPINR37 | 06EA | — | SYNCI1R<6:0> | | | | | | | — | — | — | — | — | — | — | — | 0000 |
| RPINR38 | 06EC | — | DTCMP1R<6:0> | | | | | | | — | — | — | — | — | — | — | — | 0000 |
| RPINR39 | 06EE | — | DTCMP3R<6:0> | | | | | | | — | DTCMP2R<6:0> | | | | | | | 0000 |

**Legend:** — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

**TABLE 4-30: PERIPHERAL PIN SELECT INPUT REGISTER MAP FOR PIC24EPXXXGP20X DEVICES ONLY**

| File Name | Addr. | Bit 15 | Bit 14 | Bit 13 | Bit 12 | Bit 11 | Bit 10 | Bit 9 | Bit 8 | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 | All Resets |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| RPINR0 | 06A0 | — | INT1R<6:0> | | | | | | | — | — | — | — | — | — | — | — | 0000 |
| RPINR1 | 06A2 | — | — | — | — | — | — | — | — | — | INT2R<6:0> | | | | | | | 0000 |
| RPINR3 | 06A6 | — | — | — | — | — | — | — | — | — | T2CKR<6:0> | | | | | | | 0000 |
| RPINR7 | 06AE | — | IC2R<6:0> | | | | | | | — | IC1R<6:0> | | | | | | | 0000 |
| RPINR8 | 06B0 | — | IC4R<6:0> | | | | | | | — | IC3R<6:0> | | | | | | | 0000 |
| RPINR11 | 06B6 | — | — | — | — | — | — | — | — | — | OCFAR<6:0> | | | | | | | 0000 |
| RPINR18 | 06C4 | — | — | — | — | — | — | — | — | — | U1RXR<6:0> | | | | | | | 0000 |
| RPINR19 | 06C6 | — | — | — | — | — | — | — | — | — | U2RXR<6:0> | | | | | | | 0000 |
| RPINR22 | 06CC | — | SCK2INR<6:0> | | | | | | | — | SDI2R<6:0> | | | | | | | 0000 |
| RPINR23 | 06CE | — | — | — | — | — | — | — | — | — | SS2R<6:0> | | | | | | | 0000 |

**Legend:** — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

## 5.2 RTSP Operation

RTSP allows the user application to erase a single page of memory and to program two instruction words at a time. See the General Purpose and Motor Control Family tables (Table 1 and Table 2, respectively) for the page sizes of each device.

For more information on erasing and programming Flash memory, refer to **"Flash Programming"** (DS70609) in the *"dsPIC33/PIC24 Family Reference Manual"*.

## 5.3 Programming Operations

A complete programming sequence is necessary for programming or erasing the internal Flash in RTSP mode. The processor stalls (waits) until the programming operation is finished.

For erase and program times, refer to Parameters D137a and D137b (Page Erase Time), and D138a and D138b (Word Write Cycle Time) in Table 30-14 in **Section 30.0 "Electrical Characteristics"**.

Setting the WR bit (NVMCON<15>) starts the operation and the WR bit is automatically cleared when the operation is finished.

### 5.3.1 PROGRAMMING ALGORITHM FOR FLASH PROGRAM MEMORY

Programmers can program two adjacent words (24 bits x 2) of program Flash memory at a time on every other word address boundary (0x000002, 0x000006, 0x00000A, etc.). To do this, it is necessary to erase the page that contains the desired address of the location the user wants to change.

For protection against accidental operations, the write initiate sequence for NVMKEY must be used to allow any erase or program operation to proceed. After the programming command has been executed, the user application must wait for the programming time until programming is complete. The two instructions following the start of the programming sequence should be NOPs.

Refer to **Flash Programming"** (DS70609) in the "*dsPIC33/PIC24 Family Reference Manual*" for details and codes examples on programming using RTSP.

## 5.4 Flash Memory Resources

Many useful resources are provided on the main product page of the Microchip web site for the devices listed in this data sheet. This product page, which can be accessed using this link, contains the latest updates and additional information.

| | |
|---|---|
| **Note:** | In the event you are not able to access the product page using the link above, enter this URL in your browser: http://www.microchip.com/wwwproducts/Devices.aspx?dDocName=en555464 |

### 5.4.1 KEY RESOURCES

- **"Flash Programming"** (DS70609) in the *"dsPIC33/PIC24 Family Reference Manual"*
- Code Samples
- Application Notes
- Software Libraries
- Webinars
- All Related *"dsPIC33/PIC24 Family Reference Manual"* Sections
- Development Tools

## 5.5 Control Registers

Four SFRs are used to erase and write the program Flash memory: NVMCON, NVMKEY, NVMADRH and NVMADRL.

The NVMCON register (Register 5-1) enables and initiates Flash memory erase and write operations.

NVMKEY (Register 5-4) is a write-only register that is used for write protection. To start a programming or erase sequence, the user application must consecutively write 0x55 and 0xAA to the NVMKEY register.

There are two NVM Address registers: NVMADRH and NVMADRL. These two registers, when concatenated, form the 24-bit Effective Address (EA) of the selected word for programming operations or the selected page for erase operations.

The NVMADRH register is used to hold the upper 8 bits of the EA, while the NVMADRL register is used to hold the lower 16 bits of the EA.

**FIGURE 7-1: dsPIC33EPXXXGP50X, dsPIC33EPXXXMC20X/50X AND PIC24EPXXXGP/MC20X INTERRUPT VECTOR TABLE**

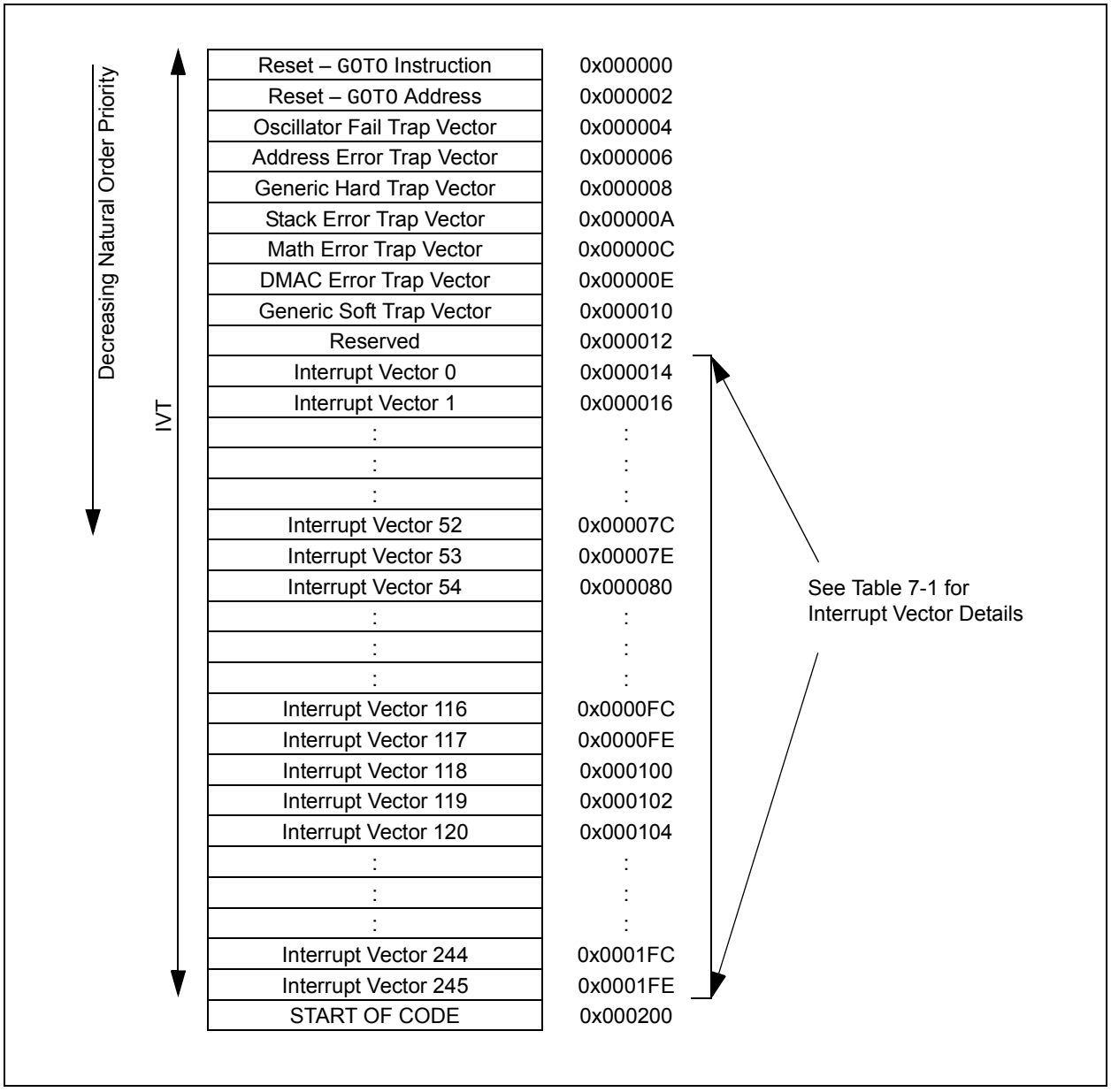


**TABLE 11-2: INPUT PIN SELECTION FOR SELECTABLE INPUT SOURCES**

| Peripheral Pin Select Input Register Value | Input/ Output | Pin Assignment | Peripheral Pin Select Input Register Value | Input/ Output | Pin Assignment |
|---|---|---|---|---|---|
| 000 0000 | I | Vss | 010 1101 | I | RPI45 |
| 000 0001 | I | C1OUT(1) | 010 1110 | I | RPI46 |
| 000 0010 | I | C2OUT(1) | 010 1111 | I | RPI47 |
| 000 0011 | I | C3OUT(1) | 011 0000 | — | — |
| 000 0100 | I | C4OUT(1) | 011 0001 | — | — |
| 000 0101 | — | — | 011 0010 | — | — |
| 000 0110 | I | PTGO30(1) | 011 0011 | I | RPI51 |
| 000 0111 | I | PTGO31(1) | 011 0100 | I | RPI52 |
| 000 1000 | I | FINDX1(1,2) | 011 0101 | I | RPI53 |
| 000 1001 | I | FHOME1(1,2) | 011 0110 | I/O | RP54 |
| 000 1010 | — | — | 011 0111 | I/O | RP55 |
| 000 1011 | — | — | 011 1000 | I/O | RP56 |
| 000 1100 | — | — | 011 1001 | I/O | RP57 |
| 000 1101 | — | — | 011 1010 | I | RPI58 |
| 000 1110 | — | — | 011 1011 | — | — |
| 000 1111 | — | — | 011 1100 | — | — |
| 001 0000 | — | — | 011 1101 | — | — |
| 001 0001 | — | — | 011 1110 | — | — |
| 001 0010 | — | — | 011 1111 | — | — |
| 001 0011 | — | — | 100 0000 | — | — |
| 001 0100 | I/O | RP20 | 100 0001 | — | — |
| 001 0101 | — | — | 100 0010 | — | — |
| 001 0110 | — | — | 100 0011 | — | — |
| 001 0111 | — | — | 100 0100 | — | — |
| 001 1000 | I | RPI24 | 100 0101 | — | — |
| 001 1001 | I | RPI25 | 100 0110 | — | — |
| 001 1010 | — | — | 100 0111 | — | — |
| 001 1011 | I | RPI27 | 100 1000 | — | — |
| 001 1100 | I | RPI28 | 100 1001 | — | — |
| 001 1101 | — | — | 100 1010 | — | — |
| 001 1110 | — | — | 100 1011 | — | — |
| 001 1111 | — | — | 100 1100 | — | — |
| 010 0000 | I | RPI32 | 100 1101 | — | — |
| 010 0001 | I | RPI33 | 100 1110 | — | — |
| 010 0010 | I | RPI34 | 100 1111 | — | — |
| 010 0011 | I/O | RP35 | 101 0000 | — | — |
| 010 0100 | I/O | RP36 | 101 0001 | — | — |
| 010 0101 | I/O | RP37 | 101 0010 | — | — |
| 010 0110 | I/O | RP38 | 101 0011 | — | — |
| 010 0111 | I/O | RP39 | 101 0100 | — | — |

**Legend:** Shaded rows indicate PPS Input register values that are unimplemented.

**Note 1:** See **Section 11.4.4.1 “Virtual Connections”** for more information on selecting this pin assignment.

**2:** These inputs are available on dsPIC33EPXXXGP/MC50X devices only.

**REGISTER 11-22: RPOR4: PERIPHERAL PIN SELECT OUTPUT REGISTER 4**

| U-0 | U-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
|---|---|---|---|---|---|---|---|
| — | — | RP43R<5:0> | | | | | |
| bit 15 | | | | | | | bit 8 |

| U-0 | U-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
|---|---|---|---|---|---|---|---|
| — | — | RP42R<5:0> | | | | | |
| bit 7 | | | | | | | bit 0 |

| **Legend:** | | | |
|---|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as ‘0’ | |
| -n = Value at POR | ‘1’ = Bit is set | ‘0’ = Bit is cleared | x = Bit is unknown |

bit 15-14 **Unimplemented:** Read as ‘0’

bit 13-8 **RP43R<5:0>:** Peripheral Output Function is Assigned to RP43 Output Pin bits (see Table 11-3 for peripheral function numbers)

bit 7-6 **Unimplemented:** Read as ‘0’

bit 5-0 **RP42R<5:0>:** Peripheral Output Function is Assigned to RP42 Output Pin bits (see Table 11-3 for peripheral function numbers)

**REGISTER 11-23: RPOR5: PERIPHERAL PIN SELECT OUTPUT REGISTER 5**

| U-0 | U-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
|---|---|---|---|---|---|---|---|
| — | — | RP55R<5:0> | | | | | |
| bit 15 | | | | | | | bit 8 |

| U-0 | U-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
|---|---|---|---|---|---|---|---|
| — | — | RP54R<5:0> | | | | | |
| bit 7 | | | | | | | bit 0 |

| **Legend:** | | | |
|---|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as ‘0’ | |
| -n = Value at POR | ‘1’ = Bit is set | ‘0’ = Bit is cleared | x = Bit is unknown |

bit 15-14 **Unimplemented:** Read as ‘0’

bit 13-8 **RP55R<5:0>:** Peripheral Output Function is Assigned to RP55 Output Pin bits (see Table 11-3 for peripheral function numbers)

bit 7-6 **Unimplemented:** Read as ‘0’

bit 5-0 **RP54R<5:0>:** Peripheral Output Function is Assigned to RP54 Output Pin bits (see Table 11-3 for peripheral function numbers)

**NOTES:**

**REGISTER 15-2: OCxCON2: OUTPUT COMPARE x CONTROL REGISTER 2**

| R/W-0 | R/W-0 | R/W-0 | R/W-0 | U-0 | U-0 | U-0 | R/W-0 |
|---|---|---|---|---|---|---|---|
| FLTMD | FLTOUT | FLTTRIEN | OCINV | — | — | — | OC32 |
| bit 15 | | | | | | | bit 8 |

| R/W-0 | R/W-0, HS | R/W-0 | R/W-0 | R/W-1 | R/W-1 | R/W-0 | R/W-0 |
|---|---|---|---|---|---|---|---|
| OCTRIG | TRIGSTAT | OCTRIS | SYNCSEL4 | SYNCSEL3 | SYNCSEL2 | SYNCSEL1 | SYNCSEL0 |
| bit 7 | | | | | | | bit 0 |

| **Legend:** | HS = Hardware Settable bit | | |
|---|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as '0' | |
| -n = Value at POR | '1' = Bit is set | '0' = Bit is cleared | x = Bit is unknown |

bit 15 **FLTMD:** Fault Mode Select bit
1 = Fault mode is maintained until the Fault source is removed; the corresponding OCFLTx bit is cleared in software and a new PWM period starts
0 = Fault mode is maintained until the Fault source is removed and a new PWM period starts

bit 14 **FLTOUT:** Fault Out bit
1 = PWM output is driven high on a Fault
0 = PWM output is driven low on a Fault

bit 13 **FLTTRIEN:** Fault Output State Select bit
1 = OCx pin is tri-stated on a Fault condition
0 = OCx pin I/O state is defined by the FLTOUT bit on a Fault condition

bit 12 **OCINV:** Output Compare x Invert bit
1 = OCx output is inverted
0 = OCx output is not inverted

bit 11-9 **Unimplemented:** Read as '0'

bit 8 **OC32:** Cascade Two OCx Modules Enable bit (32-bit operation)
1 = Cascade module operation is enabled
0 = Cascade module operation is disabled

bit 7 **OCTRIG:** Output Compare x Trigger/Sync Select bit
1 = Triggers OCx from the source designated by the SYNCSELx bits
0 = Synchronizes OCx with the source designated by the SYNCSELx bits

bit 6 **TRIGSTAT:** Timer Trigger Status bit
1 = Timer source has been triggered and is running
0 = Timer source has not been triggered and is being held clear

bit 5 **OCTRIS:** Output Compare x Output Pin Direction Select bit
1 = OCx is tri-stated
0 = Output Compare x module drives the OCx pin

**Note 1:** Do not use the OCx module as its own Synchronization or Trigger source.

**2:** When the OCy module is turned OFF, it sends a trigger out signal. If the OCx module uses the OCy module as a Trigger source, the OCy module must be unselected as a Trigger source prior to disabling it.

**3:** Each Output Compare x module (OCx) has one PTG Trigger/Synchronization source. See **Section 24.0 "Peripheral Trigger Generator (PTG) Module"** for more information.
PTGO0 = OC1
PTGO1 = OC2
PTGO2 = OC3
PTGO3 = OC4

**REGISTER 18-3: SPIxCON2: SPIx CONTROL REGISTER 2**

| R/W-0 | R/W-0 | R/W-0 | U-0 | U-0 | U-0 | U-0 | U-0 |
|---|---|---|---|---|---|---|---|
| FRMEN | SPIFSD | FRMPOL | — | — | — | — | — |
| bit 15 | | | | | | | bit 8 |

| U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | R/W-0 | R/W-0 |
|---|---|---|---|---|---|---|---|
| — | — | — | — | — | — | FRMDLY | SPIBEN |
| bit 7 | | | | | | | bit 0 |

| **Legend:** | | | |
|---|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as '0' | |
| -n = Value at POR | '1' = Bit is set | '0' = Bit is cleared | x = Bit is unknown |

bit 15 **FRMEN:** Framed SPIx Support bit
1 = Framed SPIx support is enabled ($\overline{SS}$x pin is used as Frame Sync pulse input/output)
0 = Framed SPIx support is disabled

bit 14 **SPIFSD:** Frame Sync Pulse Direction Control bit
1 = Frame Sync pulse input (slave)
0 = Frame Sync pulse output (master)

bit 13 **FRMPOL:** Frame Sync Pulse Polarity bit
1 = Frame Sync pulse is active-high
0 = Frame Sync pulse is active-low

bit 12-2 **Unimplemented:** Read as '0'

bit 1 **FRMDLY:** Frame Sync Pulse Edge Select bit
1 = Frame Sync pulse coincides with first bit clock
0 = Frame Sync pulse precedes first bit clock

bit 0 **SPIBEN:** Enhanced Buffer Enable bit
1 = Enhanced buffer is enabled
0 = Enhanced buffer is disabled (Standard mode)

**REGISTER 21-2: CxCTRL2: ECANx CONTROL REGISTER 2**

| U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 |
|---|---|---|---|---|---|---|---|
| — | — | — | — | — | — | — | — |
| bit 15 | | | | | | | bit 8 |

| U-0 | U-0 | U-0 | R-0 | R-0 | R-0 | R-0 | R-0 |
|---|---|---|---|---|---|---|---|
| — | — | — | DNCNT4 | DNCNT3 | DNCNT2 | DNCNT1 | DNCNT0 |
| bit 7 | | | | | | | bit 0 |

| **Legend:** | | | |
|---|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as ‘0’ | |
| -n = Value at POR | ‘1’ = Bit is set | ‘0’ = Bit is cleared | x = Bit is unknown |

bit 15-5 **Unimplemented:** Read as ‘0’

bit 4-0 **DNCNT<4:0>:** DeviceNet™ Filter Bit Number bits

10010-11111 = Invalid selection
10001 = Compares up to Data Byte 3, bit 6 with EID<17>
•
•
•
00001 = Compares up to Data Byte 1, bit 7 with EID<0>
00000 = Does not compare data bytes

**REGISTER 26-3: CRCXORH: CRC XOR POLYNOMIAL HIGH REGISTER**

| R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
|---|---|---|---|---|---|---|---|
| X<31:24> | | | | | | | |
| bit 15 | | | | | | | bit 8 |

| R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
|---|---|---|---|---|---|---|---|
| X<23:16> | | | | | | | |
| bit 7 | | | | | | | bit 0 |

| **Legend:** | | | |
|---|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as ‘0’ | |
| -n = Value at POR | ‘1’ = Bit is set | ‘0’ = Bit is cleared | x = Bit is unknown |

bit 15-0 **X<31:16>:** XOR of Polynomial Term $X^n$ Enable bits

**REGISTER 26-4: CRCXORL: CRC XOR POLYNOMIAL LOW REGISTER**

| R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
|---|---|---|---|---|---|---|---|
| X<15:8> | | | | | | | |
| bit 15 | | | | | | | bit 8 |

| R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | U-0 |
|---|---|---|---|---|---|---|---|
| X<7:1> | | | | | | | — |
| bit 7 | | | | | | | bit 0 |

| **Legend:** | | | |
|---|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as ‘0’ | |
| -n = Value at POR | ‘1’ = Bit is set | ‘0’ = Bit is cleared | x = Bit is unknown |

bit 15-1 **X<15:1>:** XOR of Polynomial Term $X^n$ Enable bits

bit 0 **Unimplemented:** Read as ‘0’

## 27.2 User ID Words

dsPIC33EPXXXGP50X, dsPIC33EPXXXMC20X/50X and PIC24EPXXXGP/MC20X devices contain four User ID Words, located at addresses, 0x800FF8 through 0x800FFE. The User ID Words can be used for storing product information such as serial numbers, system manufacturing dates, manufacturing lot numbers and other application-specific information.

The User ID Words register map is shown in Table 27-3.

**TABLE 27-3: USER ID WORDS REGISTER MAP**

| File Name | Address | Bits 23-16 | Bits 15-0 |
|---|---|---|---|
| FUID0 | 0x800FF8 | — | UID0 |
| FUID1 | 0x800FFA | — | UID1 |
| FUID2 | 0x800FFC | — | UID2 |
| FUID3 | 0x800FFE | — | UID3 |

**Legend:** — = unimplemented, read as '1'.

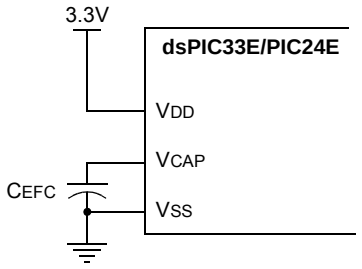
## 27.3 On-Chip Voltage Regulator

All of the dsPIC33EPXXXGP50X, dsPIC33EPXXXMC20X/50X and PIC24EPXXXGP/MC20X devices power their core digital logic at a nominal 1.8V. This can create a conflict for designs that are required to operate at a higher typical voltage, such as 3.3V. To simplify system design, all devices in the dsPIC33EPXXXGP50X, dsPIC33EPXXXMC20X/50X and PIC24EPXXXGP/MC20X family incorporate an on-chip regulator that allows the device to run its core logic from VDD.

The regulator provides power to the core from the other VDD pins. A low-ESR (less than 1 Ohm) capacitor (such as tantalum or ceramic) must be connected to the VCAP pin (Figure 27-1). This helps to maintain the stability of the regulator. The recommended value for the filter capacitor is provided in Table 30-5 located in **Section 30.0 "Electrical Characteristics"**.

| | |
|---|---|
| **Note:** | It is important for the low-ESR capacitor to be placed as close as possible to the VCAP pin. |

**FIGURE 27-1: CONNECTIONS FOR THE ON-CHIP VOLTAGE REGULATOR(1,2,3)**




**Note 1:** These are typical operating voltages. Refer to Table 30-5 located in **Section 30.1 "DC Characteristics"** for the full operating ranges of VDD and VCAP.

**2:** It is important for the low-ESR capacitor to be placed as close as possible to the VCAP pin.

**3:** Typical VCAP pin voltage = 1.8V when VDD ≥ VDDMIN.

## 27.4 Brown-out Reset (BOR)

The Brown-out Reset (BOR) module is based on an internal voltage reference circuit that monitors the regulated supply voltage, VCAP. The main purpose of the BOR module is to generate a device Reset when a brown-out condition occurs. Brown-out conditions are generally caused by glitches on the AC mains (for example, missing portions of the AC cycle waveform due to bad power transmission lines or voltage sags due to excessive current draw when a large inductive load is turned on).

A BOR generates a Reset pulse, which resets the device. The BOR selects the clock source, based on the device Configuration bit values (FNOSC<2:0> and POSCMD<1:0>).

If an oscillator mode is selected, the BOR activates the Oscillator Start-up Timer (OST). The system clock is held until OST expires. If the PLL is used, the clock is held until the LOCK bit (OSCCON<5>) is '1'.

Concurrently, the PWRT Time-out (TPWRT) is applied before the internal Reset is released. If TPWRT = 0 and a crystal oscillator is being used, then a nominal delay of TFSCM is applied. The total delay in this case is TFSCM. Refer to Parameter SY35 in Table 30-22 of **Section 30.0 "Electrical Characteristics"** for specific TFSCM values.

The BOR status bit (RCON<1>) is set to indicate that a BOR has occurred. The BOR circuit continues to operate while in Sleep or Idle modes and resets the device should VDD fall below the BOR threshold voltage.

**TABLE 28-2: INSTRUCTION SET OVERVIEW (CONTINUED)**

| Base Instr # | Assembly Mnemonic | Assembly Syntax | | Description | # of Words | # of Cycles(2) | Status Flags Affected |
|---|---|---|---|---|---|---|---|
| 53 | NEG | NEG | Acc(1) | Negate Accumulator | 1 | 1 | OA,OB,OAB, SA,SB,SAB |
| | | NEG | f | f = $\bar{f}$ + 1 | 1 | 1 | C,DC,N,OV,Z |
| | | NEG | f,WREG | WREG = $\bar{f}$ + 1 | 1 | 1 | C,DC,N,OV,Z |
| | | NEG | Ws,Wd | Wd = $\overline{Ws}$ + 1 | 1 | 1 | C,DC,N,OV,Z |
| 54 | NOP | NOP | | No Operation | 1 | 1 | None |
| | | NOPR | | No Operation | 1 | 1 | None |
| 55 | POP | POP | f | Pop f from Top-of-Stack (TOS) | 1 | 1 | None |
| | | POP | Wdo | Pop from Top-of-Stack (TOS) to Wdo | 1 | 1 | None |
| | | POP.D | Wnd | Pop from Top-of-Stack (TOS) to W(nd):W(nd + 1) | 1 | 2 | None |
| | | POP.S | | Pop Shadow Registers | 1 | 1 | All |
| 56 | PUSH | PUSH | f | Push f to Top-of-Stack (TOS) | 1 | 1 | None |
| | | PUSH | Wso | Push Wso to Top-of-Stack (TOS) | 1 | 1 | None |
| | | PUSH.D | Wns | Push W(ns):W(ns + 1) to Top-of-Stack (TOS) | 1 | 2 | None |
| | | PUSH.S | | Push Shadow Registers | 1 | 1 | None |
| 57 | PWRSAV | PWRSAV | #lit1 | Go into Sleep or Idle mode | 1 | 1 | WDTO,Sleep |
| 58 | RCALL | RCALL | Expr | Relative Call | 1 | 4 | SFA |
| | | RCALL | Wn | Computed Call | 1 | 4 | SFA |
| 59 | REPEAT | REPEAT | #lit15 | Repeat Next Instruction lit15 + 1 times | 1 | 1 | None |
| | | REPEAT | Wn | Repeat Next Instruction (Wn) + 1 times | 1 | 1 | None |
| 60 | RESET | RESET | | Software device Reset | 1 | 1 | None |
| 61 | RETFIE | RETFIE | | Return from interrupt | 1 | 6 (5) | SFA |
| 62 | RETLW | RETLW | #lit10,Wn | Return with literal in Wn | 1 | 6 (5) | SFA |
| 63 | RETURN | RETURN | | Return from Subroutine | 1 | 6 (5) | SFA |
| 64 | RLC | RLC | f | f = Rotate Left through Carry f | 1 | 1 | C,N,Z |
| | | RLC | f,WREG | WREG = Rotate Left through Carry f | 1 | 1 | C,N,Z |
| | | RLC | Ws,Wd | Wd = Rotate Left through Carry Ws | 1 | 1 | C,N,Z |
| 65 | RLNC | RLNC | f | f = Rotate Left (No Carry) f | 1 | 1 | N,Z |
| | | RLNC | f,WREG | WREG = Rotate Left (No Carry) f | 1 | 1 | N,Z |
| | | RLNC | Ws,Wd | Wd = Rotate Left (No Carry) Ws | 1 | 1 | N,Z |
| 66 | RRC | RRC | f | f = Rotate Right through Carry f | 1 | 1 | C,N,Z |
| | | RRC | f,WREG | WREG = Rotate Right through Carry f | 1 | 1 | C,N,Z |
| | | RRC | Ws,Wd | Wd = Rotate Right through Carry Ws | 1 | 1 | C,N,Z |
| 67 | RRNC | RRNC | f | f = Rotate Right (No Carry) f | 1 | 1 | N,Z |
| | | RRNC | f,WREG | WREG = Rotate Right (No Carry) f | 1 | 1 | N,Z |
| | | RRNC | Ws,Wd | Wd = Rotate Right (No Carry) Ws | 1 | 1 | N,Z |
| 68 | SAC | SAC | Acc,#Slit4,Wdo(1) | Store Accumulator | 1 | 1 | None |
| | | SAC.R | Acc,#Slit4,Wdo(1) | Store Rounded Accumulator | 1 | 1 | None |
| 69 | SE | SE | Ws,Wnd | Wnd = sign-extended Ws | 1 | 1 | C,N,Z |
| 70 | SETM | SETM | f | f = 0xFFFF | 1 | 1 | None |
| | | SETM | WREG | WREG = 0xFFFF | 1 | 1 | None |
| | | SETM | Ws | Ws = 0xFFFF | 1 | 1 | None |
| 71 | SFTAC | SFTAC | Acc,Wn(1) | Arithmetic Shift Accumulator by (Wn) | 1 | 1 | OA,OB,OAB, SA,SB,SAB |
| | | SFTAC | Acc,#Slit6(1) | Arithmetic Shift Accumulator by Slit6 | 1 | 1 | OA,OB,OAB, SA,SB,SAB |

**Note 1:** These instructions are available in dsPIC33EPXXXMC20X/50X and PIC24EPXXXMC20X devices only.

**2:** Read and Read-Modify-Write (e.g., bit operations and logical operations) on non-CPU SFRs incur an additional instruction cycle.

## 30.1 DC Characteristics

**TABLE 30-1: OPERATING MIPS VS. VOLTAGE**

| Characteristic | VDD Range (in Volts) | Temp Range (in °C) | Maximum MIPS |
|---|---|---|---|
| | | | dsPIC33EPXXXGP50X, dsPIC33EPXXXMC20X/50X and PIC24EPXXXGP/MC20X |
| — | 3.0V to 3.6V(1) | -40°C to +85°C | 70 |
| — | 3.0V to 3.6V(1) | -40°C to +125°C | 60 |

**Note 1:** Device is functional at VBORMIN < VDD < VDDMIN. Analog modules (ADC, op amp/comparator and comparator voltage reference) may have degraded performance. Device functionality is tested but not characterized. Refer to Parameter BO10 in Table 30-13 for the minimum and maximum BOR values.

**TABLE 30-2: THERMAL OPERATING CONDITIONS**

| Rating | Symbol | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|
| Industrial Temperature Devices | | | | | |
| Operating Junction Temperature Range | TJ | -40 | — | +125 | °C |
| Operating Ambient Temperature Range | TA | -40 | — | +85 | °C |
| Extended Temperature Devices | | | | | |
| Operating Junction Temperature Range | TJ | -40 | — | +140 | °C |
| Operating Ambient Temperature Range | TA | -40 | — | +125 | °C |
| Power Dissipation:<br>Internal chip power dissipation:<br>PINT = VDD x (IDD – Σ IOH)<br>I/O Pin Power Dissipation:<br>I/O = Σ ({VDD – VOH} x IOH) + Σ (VOL x IOL) | PD | PINT + PI/O | | | W |
| Maximum Allowed Power Dissipation | PDMAX | (TJ – TA)/θJA | | | W |

**TABLE 30-3: THERMAL PACKAGING CHARACTERISTICS**

| Characteristic | Symbol | Typ. | Max. | Unit | Notes |
|---|---|---|---|---|---|
| Package Thermal Resistance, 64-Pin QFN | θJA | 28.0 | — | °C/W | 1 |
| Package Thermal Resistance, 64-Pin TQFP 10x10 mm | θJA | 48.3 | — | °C/W | 1 |
| Package Thermal Resistance, 48-Pin UQFN 6x6 mm | θJA | 41 | — | °C/W | 1 |
| Package Thermal Resistance, 44-Pin QFN | θJA | 29.0 | — | °C/W | 1 |
| Package Thermal Resistance, 44-Pin TQFP 10x10 mm | θJA | 49.8 | — | °C/W | 1 |
| Package Thermal Resistance, 44-Pin VTLA 6x6 mm | θJA | 25.2 | — | °C/W | 1 |
| Package Thermal Resistance, 36-Pin VTLA 5x5 mm | θJA | 28.5 | — | °C/W | 1 |
| Package Thermal Resistance, 28-Pin QFN-S | θJA | 30.0 | — | °C/W | 1 |
| Package Thermal Resistance, 28-Pin SSOP | θJA | 71.0 | — | °C/W | 1 |
| Package Thermal Resistance, 28-Pin SOIC | θJA | 69.7 | — | °C/W | 1 |
| Package Thermal Resistance, 28-Pin SPDIP | θJA | 60.0 | — | °C/W | 1 |

**Note 1:** Junction to ambient thermal resistance, Theta-JA (θJA) numbers are achieved by package simulations.

**FIGURE 30-11: TIMERQ (QEI MODULE) EXTERNAL CLOCK TIMING CHARACTERISTICS (dsPIC33EPXXXMC20X/50X AND PIC24EPXXXMC20X DEVICES ONLY)**

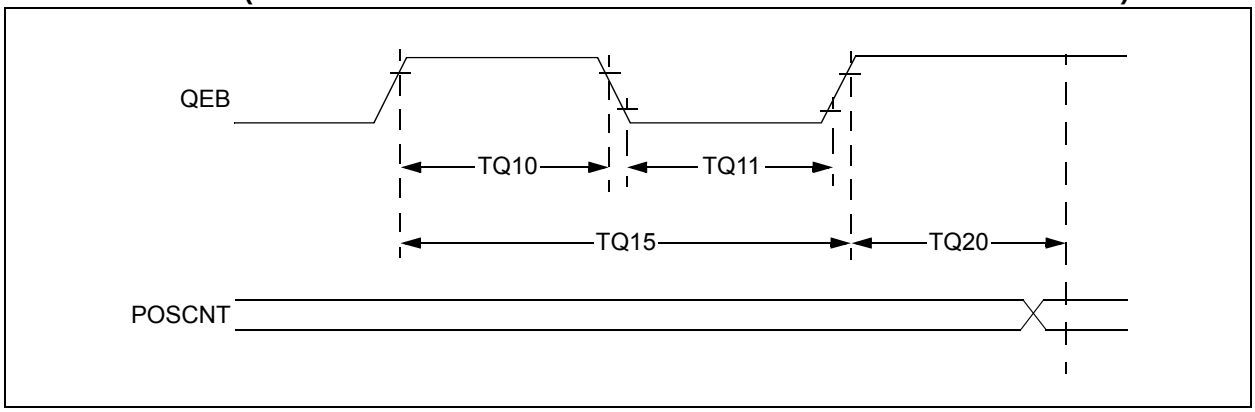



**TABLE 30-30: QEI MODULE EXTERNAL CLOCK TIMING REQUIREMENTS (dsPIC33EPXXXMC20X/50X AND PIC24EPXXXMC20X DEVICES ONLY)**

| AC CHARACTERISTICS | | | | Standard Operating Conditions: 3.0V to 3.6V (unless otherwise stated)<br>Operating temperature -40°C ≤ TA ≤ +85°C for Industrial<br>-40°C ≤ TA ≤ +125°C for Extended | | | | |
|---|---|---|---|---|---|---|---|---|
| **Param No.** | **Symbol** | **Characteristic(1)** | | **Min.** | **Typ.** | **Max.** | **Units** | **Conditions** |
| TQ10 | TtQH | TQCK High Time | Synchronous, with prescaler | Greater of 12.5 + 25 or (0.5 TCY/N) + 25 | — | — | ns | Must also meet Parameter TQ15 |
| TQ11 | TtQL | TQCK Low Time | Synchronous, with prescaler | Greater of 12.5 + 25 or (0.5 TCY/N) + 25 | — | — | ns | Must also meet Parameter TQ15 |
| TQ15 | TtQP | TQCP Input Period | Synchronous, with prescaler | Greater of 25 + 50 or (1 TCY/N) + 50 | — | — | ns | |
| TQ20 | TCKEXTMRL | Delay from External TQCK Clock Edge to Timer Increment | | — | 1 | TCY | — | |

**Note 1:** These parameters are characterized but not tested in manufacturing.

**TABLE 30-38: SPI2 SLAVE MODE (FULL-DUPLEX, CKE = 1, CKP = 1, SMP = 0) TIMING REQUIREMENTS**

| AC CHARACTERISTICS | | | Standard Operating Conditions: 3.0V to 3.6V (unless otherwise stated)<br>Operating temperature -40°C ≤ TA ≤ +85°C for Industrial<br>-40°C ≤ TA ≤ +125°C for Extended | | | | |
|---|---|---|---|---|---|---|---|
| **Param.** | **Symbol** | **Characteristic(1)** | **Min.** | **Typ.(2)** | **Max.** | **Units** | **Conditions** |
| SP70 | FscP | Maximum SCK2 Input Frequency | — | — | Lesser of FP or 11 | MHz | **(Note 3)** |
| SP72 | TscF | SCK2 Input Fall Time | — | — | — | ns | See Parameter DO32 **(Note 4)** |
| SP73 | TscR | SCK2 Input Rise Time | — | — | — | ns | See Parameter DO31 **(Note 4)** |
| SP30 | TdoF | SDO2 Data Output Fall Time | — | — | — | ns | See Parameter DO32 **(Note 4)** |
| SP31 | TdoR | SDO2 Data Output Rise Time | — | — | — | ns | See Parameter DO31 **(Note 4)** |
| SP35 | TscH2doV, TscL2doV | SDO2 Data Output Valid after SCK2 Edge | — | 6 | 20 | ns | |
| SP36 | TdoV2scH, TdoV2scL | SDO2 Data Output Setup to First SCK2 Edge | 30 | — | — | ns | |
| SP40 | TdiV2scH, TdiV2scL | Setup Time of SDI2 Data Input to SCK2 Edge | 30 | — | — | ns | |
| SP41 | TscH2diL, TscL2diL | Hold Time of SDI2 Data Input to SCK2 Edge | 30 | — | — | ns | |
| SP50 | TssL2scH, TssL2scL | $\overline{SS2}$ ↓ to SCK2 ↑ or SCK2 ↓ Input | 120 | — | — | ns | |
| SP51 | TssH2doZ | $\overline{SS2}$ ↑ to SDO2 Output High-Impedance | 10 | — | 50 | ns | **(Note 4)** |
| SP52 | TscH2ssH TscL2ssH | $\overline{SS2}$ ↑ after SCK2 Edge | 1.5 TCY + 40 | — | — | ns | **(Note 4)** |
| SP60 | TssL2doV | SDO2 Data Output Valid after $\overline{SS2}$ Edge | — | — | 50 | ns | |

**Note 1:** These parameters are characterized, but are not tested in manufacturing.

**2:** Data in "Typical" column is at 3.3V, +25°C unless otherwise stated.

**3:** The minimum clock period for SCK2 is 91 ns. Therefore, the SCK2 clock generated by the master must not violate this specification.

**4:** Assumes 50 pF load on all SPI2 pins.

**TABLE 30-59: ADC MODULE SPECIFICATIONS (10-BIT MODE)**

| AC CHARACTERISTICS | | | Standard Operating Conditions: 3.0V to 3.6V (unless otherwise stated)(1)<br>Operating temperature -40°C ≤ TA ≤ +85°C for Industrial<br>-40°C ≤ TA ≤ +125°C for Extended | | | | |
|---|---|---|---|---|---|---|---|
| **Param No.** | **Symbol** | **Characteristic** | **Min.** | **Typ.** | **Max.** | **Units** | **Conditions** |
| **ADC Accuracy (10-Bit Mode)** | | | | | | | |
| AD20b | Nr | Resolution | 10 Data Bits | | | bits | |
| AD21b | INL | Integral Nonlinearity | -0.625 | — | 0.625 | LSb | -40°C ≤ TA ≤ +85°C **(Note 2)** |
| | | | -1.5 | — | 1.5 | LSb | +85°C < TA ≤ +125°C **(Note 2)** |
| AD22b | DNL | Differential Nonlinearity | -0.25 | — | 0.25 | LSb | -40°C ≤ TA ≤ +85°C **(Note 2)** |
| | | | -0.25 | — | 0.25 | LSb | +85°C < TA ≤ +125°C **(Note 2)** |
| AD23b | GERR | Gain Error | -2.5 | — | 2.5 | LSb | -40°C ≤ TA ≤ +85°C **(Note 2)** |
| | | | -2.5 | — | 2.5 | LSb | +85°C < TA ≤ +125°C **(Note 2)** |
| AD24b | EOFF | Offset Error | -1.25 | — | 1.25 | LSb | -40°C ≤ TA ≤ +85°C **(Note 2)** |
| | | | -1.25 | — | 1.25 | LSb | +85°C < TA ≤ +125°C **(Note 2)** |
| AD25b | — | Monotonicity | — | — | — | — | Guaranteed |
| **Dynamic Performance (10-Bit Mode)** | | | | | | | |
| AD30b | THD | Total Harmonic Distortion(3) | — | 64 | — | dB | |
| AD31b | SINAD | Signal to Noise and Distortion(3) | — | 57 | — | dB | |
| AD32b | SFDR | Spurious Free Dynamic Range(3) | — | 72 | — | dB | |
| AD33b | FNYQ | Input Signal Bandwidth(3) | — | 550 | — | kHz | |
| AD34b | ENOB | Effective Number of Bits(3) | — | 9.4 | — | bits | |

**Note 1:** Device is functional at VBORMIN < VDD < VDDMIN, but will have degraded performance. Device functionality is tested, but not characterized. Analog modules (ADC, op amp/comparator and comparator voltage reference) may have degraded performance. Refer to Parameter BO10 in Table 30-13 for the minimum and maximum BOR values.

**2:** For all accuracy specifications, VINL = AVSS = VREFL = 0V and AVDD = VREFH = 3.6V.

**3:** Parameters are characterized but not tested in manufacturing.

**TABLE 30-61: ADC CONVERSION (10-BIT MODE) TIMING REQUIREMENTS**

| AC CHARACTERISTICS | | | Standard Operating Conditions: 3.0V to 3.6V (unless otherwise stated)[1]<br>Operating temperature -40°C ≤ TA ≤ +85°C for Industrial<br>-40°C ≤ TA ≤ +125°C for Extended | | | | |
|---|---|---|---|---|---|---|---|
| **Param No.** | **Symbol** | **Characteristic** | **Min.** | **Typ.** | **Max.** | **Units** | **Conditions** |
| **Clock Parameters** | | | | | | | |
| AD50 | TAD | ADC Clock Period | 76 | — | — | ns | |
| AD51 | tRC | ADC Internal RC Oscillator Period[2] | — | 250 | — | ns | |
| **Conversion Rate** | | | | | | | |
| AD55 | tCONV | Conversion Time | — | 12 TAD | — | — | |
| AD56 | FCNV | Throughput Rate | — | — | 1.1 | Msps | Using simultaneous sampling |
| AD57a | TSAMP | Sample Time when Sampling any ANx Input | 2 TAD | — | — | — | |
| AD57b | TSAMP | Sample Time when Sampling the Op Amp Outputs (Configuration A and Configuration B)[4,5] | 4 TAD | — | — | — | |
| **Timing Parameters** | | | | | | | |
| AD60 | tPCS | Conversion Start from Sample Trigger[2,3] | 2 TAD | — | 3 TAD | — | Auto-convert trigger is not selected |
| AD61 | tPSS | Sample Start from Setting Sample (SAMP) bit[2,3)] | 2 TAD | — | 3 TAD | — | |
| AD62 | tCSS | Conversion Completion to Sample Start (ASAM = 1)[2,3] | — | 0.5 TAD | — | — | |
| AD63 | tDPU | Time to Stabilize Analog Stage from ADC Off to ADC On[2,3] | — | — | 20 | μs | **(Note 6)** |

**Note 1:** Device is functional at VBORMIN < VDD < VDDMIN, but will have degraded performance. Device functionality is tested, but not characterized. Analog modules (ADC, op amp/comparator and comparator voltage reference) may have degraded performance. Refer to Parameter BO10 in Table 30-13 for the minimum and maximum BOR values.

**2:** Parameters are characterized but not tested in manufacturing.

**3:** Because the sample caps will eventually lose charge, clock rates below 10 kHz may affect linearity performance, especially at elevated temperatures.

**4:** See Figure 25-6 for configuration information.

**5:** See Figure 25-7 for configuration information.

**6:** The parameter, tDPU, is the time required for the ADC module to stabilize at the appropriate level when the module is turned on (ADON (AD1CON1<15>) = 1). During this time, the ADC result is indeterminate.

**TABLE 30-62: DMA MODULE TIMING REQUIREMENTS**

| AC CHARACTERISTICS | | Standard Operating Conditions: 3.0V to 3.6V (unless otherwise stated)<br>Operating temperature -40°C ≤ TA ≤ +85°C for Industrial<br>-40°C ≤ TA ≤ +125°C for Extended | | | | |
|---|---|---|---|---|---|---|
| **Param No.** | **Characteristic** | **Min.** | **Typ.[1]** | **Max.** | **Units** | **Conditions** |
| DM1 | DMA Byte/Word Transfer Latency | 1 TCY[2] | — | — | ns | |

**Note 1:** These parameters are characterized, but not tested in manufacturing.

**2:** Because DMA transfers use the CPU data bus, this time is dependent on other functions on the bus.