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Applications of "<u>Embedded -</u> <u>Microcontrollers</u>"

Details

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Product Status	Obsolete
Core Processor	PIC
Core Size	16-Bit
Speed	60 MIPs
Connectivity	I ² C, IrDA, LINbus, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, DMA, POR, PWM, WDT
Number of I/O	21
Program Memory Size	32KB (10.7K x 24)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	2K x 16
Voltage - Supply (Vcc/Vdd)	3V ~ 3.6V
Data Converters	A/D 6x10b/12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 150°C (TA)
Mounting Type	Surface Mount
Package / Case	28-VQFN Exposed Pad
Supplier Device Package	28-QFN-S (6x6)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/pic24ep32gp202-h-mm

Email: info@E-XFL.COM

Address: Room A, 16/F, Full Win Commercial Centre, 573 Nathan Road, Mongkok, Hong Kong



FIGURE 4-10: DATA MEMORY MAP FOR dsPIC33EP256MC20X/50X AND dsPIC33EP256GP50X DEVICES

4.4 Special Function Register Maps

TABLE 4-1: CPU CORE REGISTER MAP FOR dsPIC33EPXXXMC20X/50X AND dsPIC33EPXXXGP50X DEVICES ONLY

File Name	Addr.	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	All Resets
W0	0000								W0 (WR	EG)								xxxx
W1	0002								W1									xxxx
W2	0004								W2									xxxx
W3	0006								W3									xxxx
W4	8000								W4									xxxx
W5	000A								W5									xxxx
W6	000C								W6									xxxx
W7	000E								W7									xxxx
W8	0010								W8									xxxx
W9	0012								W9									xxxx
W10	0014								W10									xxxx
W11	0016								W11									xxxx
W12	0018								W12									xxxx
W13	001A								W13									xxxx
W14	001C								W14									xxxx
W15	001E								W15									xxxx
SPLIM	0020								SPLI	Л								0000
ACCAL	0022								ACCA	L								0000
ACCAH	0024								ACCA	н								0000
ACCAU	0026			Się	gn Extensio	n of ACCA<	39>						AC	CAU				0000
ACCBL	0028								ACCB	L								0000
ACCBH	002A								ACCB	н								0000
ACCBU	002C			Się	gn Extensio	n of ACCB<	39>						AC	CBU				0000
PCL	002E							P	CL<15:0>								—	0000
PCH	0030	_	—	—	—	_	-	—	—	—				PCH<6:0>				0000
DSRPAG	0032	_	—	—	—	_	-					DSRPAC	G<9:0>					0001
DSWPAG	0034	_	—	—	—	_	-	—				DS	WPAG<8:	0>				0001
RCOUNT	0036								RCOUNT<	:15:0>								0000
DCOUNT	0038	DCOUNT<15:0> 01							0000									
DOSTARTL	003A	DOSTARTL<15:1>0							0000									
DOSTARTH	003C	_	_	_	_	—	_	_	_	_	_			DOSTAF	RTH<5:0>			0000
DOENDL	003E							DO	ENDL<15:1>	>							_	0000
DOENDH	0040	_	_	—	—	_	_	_	—	_	_			DOEND)H<5:0>			0000

Legend: x = unknown value on Reset, — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

TABLE 4-59: PORTA REGISTER MAP FOR PIC24EPXXXGP/MC202 AND dsPIC33EPXXXGP/MC202/502 DEVICES ONLY

File Name	Addr.	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	All Resets
TRISA	0E00		—	—				—			—		TRISA4	TRISA3	TRISA2	TRISA1	TRISA0	001F
PORTA	0E02		—	_		_		—			—		RA4	RA3	RA2	RA1	RA0	0000
LATA	0E04		—	—				—			—		LATA4	LATA3	LATA2	LA1TA1	LA0TA0	0000
ODCA	0E06		—	—				—			—		ODCA4	ODCA3	ODCA2	ODCA1	ODCA0	0000
CNENA	0E08		—	—				—			—		CNIEA4	CNIEA3	CNIEA2	CNIEA1	CNIEA0	0000
CNPUA	0E0A		—	—				—			—		CNPUA4	CNPUA3	CNPUA2	CNPUA1	CNPUA0	0000
CNPDA	0E0C		—	—				—			—		CNPDA4	CNPDA3	CNPDA2	CNPDA1	CNPDA0	0000
ANSELA	0E0E	-	—	—			-	—		_	_		ANSA4	_	—	ANSA1	ANSA0	0013

Legend: — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

TABLE 4-60: PORTB REGISTER MAP FOR PIC24EPXXXGP/MC202 AND dsPIC33EPXXXGP/MC202/502 DEVICES ONLY

File Name	Addr.	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	All Resets
TRISB	0E10	TRISB15	TRISB14	TRISB13	TRISB12	TRISB11	TRISB10	TRISB9	TRISB8	TRISB7	TRISB6	TRISB5	TRISB4	TRISB3	TRISB2	TRISB1	TRISB0	FFFF
PORTB	0E12	RB15	RB14	RB13	RB12	RB11	RB10	RB9	RB8	RB7	RB6	RB5	RB4	RB3	RB2	RB1	RB0	xxxx
LATB	0E14	LATB15	LATB14	LATB13	LATB12	LATB11	LATB10	LATB9	LATB8	LATB7	LATB6	LATB5	LATB4	LATB3	LATB2	LATB1	LATB0	xxxx
ODCB	0E16	ODCB15	ODCB14	ODCB13	ODCB12	ODCB11	ODCB10	ODCB9	ODCB8	ODCB7	ODCB6	ODCB5	ODCB4	ODCB3	ODCB2	ODCB1	ODCB0	0000
CNENB	0E18	CNIEB15	CNIEB14	CNIEB13	CNIEB12	CNIEB11	CNIEB10	CNIEB9	CNIEB8	CNIEB7	CNIEB6	CNIEB5	CNIEB4	CNIEB3	CNIEB2	CNIEB1	CNIEB0	0000
CNPUB	0E1A	CNPUB15	CNPUB14	CNPUB13	CNPUB12	CNPUB11	CNPUB10	CNPUB9	CNPUB8	CNPUB7	CNPUB6	CNPUB5	CNPUB4	CNPUB3	CNPUB2	CNPUB1	CNPUB0	0000
CNPDB	0E1C	CNPDB15	CNPDB14	CNPDB13	CNPDB12	CNPDB11	CNPDB10	CNPDB9	CNPDB8	CNPDB7	CNPDB6	CNPDB5	CNPDB4	CNPDB3	CNPDB2	CNPDB1	CNPDB0	0000
ANSELB	0E1E			_	-	—	—	—	ANSB8		_	—		ANSB3	ANSB2	ANSB1	ANSB0	010F

Legend: x = unknown value on Reset, — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

4.4.1 PAGED MEMORY SCHEME

The dsPIC33EPXXXGP50X, dsPIC33EPXXXMC20X/ 50X and PIC24EPXXXGP/MC20X architecture extends the available Data Space through a paging scheme, which allows the available Data Space to be accessed using MOV instructions in a linear fashion for pre-modified and post-modified Effective Addresses (EA). The upper half of the base Data Space address is used in conjunction with the Data Space Page registers, the 10-bit Read Page register (DSRPAG) or the 9-bit Write Page register (DSWPAG), to form an Extended Data Space (EDS) address or Program Space Visibility (PSV) address. The Data Space Page registers are located in the SFR space.

Construction of the EDS address is shown in Example 4-1. When DSRPAG<9> = 0 and the base address bit, EA<15> = 1, the DSRPAG<8:0> bits are concatenated onto EA<14:0> to form the 24-bit EDS read address. Similarly, when base address bit, EA<15> = 1, DSWPAG<8:0> are concatenated onto EA<14:0> to form the 24-bit EDS write address.





REGISTER 8-7: DMAXPAD: DMA CHANNEL X PERIPHERAL ADDRESS REGISTER⁽¹⁾

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
			PAD	<15:8>			
bit 15							bit 8
R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
			PAD)<7:0>			
bit 7							bit 0
Legend:							
R = Readable	bit	W = Writable b	oit	U = Unimpler	nented bit, rea	d as '0'	
-n = Value at P	OR	'1' = Bit is set		'0' = Bit is cle	ared	x = Bit is unkr	nown

bit 15-0 PAD<15:0>: Peripheral Address Register bits

Note 1: If the channel is enabled (i.e., active), writes to this register may result in unpredictable behavior of the DMA channel and should be avoided.

REGISTER 8-8: DMAXCNT: DMA CHANNEL X TRANSFER COUNT REGISTER⁽¹⁾

U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	_			CNT<	13:8> (2)		
bit 15							bit 8
R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
			CNT≪	<7:0> (2)			
bit 7							bit 0
Legend:							
R = Readable b	oit	W = Writable b	oit	U = Unimpler	nented bit, read	d as '0'	
-n = Value at P	OR	'1' = Bit is set		'0' = Bit is cle	ared	x = Bit is unkr	nown

bit 15-14 Unimplemented: Read as '0'

bit 13-0 CNT<13:0>: DMA Transfer Count Register bits⁽²⁾

Note 1: If the channel is enabled (i.e., active), writes to this register may result in unpredictable behavior of the DMA channel and should be avoided.

2: The number of DMA transfers = CNT<13:0> + 1.

10.3 Doze Mode

The preferred strategies for reducing power consumption are changing clock speed and invoking one of the powersaving modes. In some circumstances, this cannot be practical. For example, it may be necessary for an application to maintain uninterrupted synchronous communication, even while it is doing nothing else. Reducing system clock speed can introduce communication errors, while using a power-saving mode can stop communications completely.

Doze mode is a simple and effective alternative method to reduce power consumption while the device is still executing code. In this mode, the system clock continues to operate from the same source and at the same speed. Peripheral modules continue to be clocked at the same speed, while the CPU clock speed is reduced. Synchronization between the two clock domains is maintained, allowing the peripherals to access the SFRs while the CPU executes code at a slower rate.

Doze mode is enabled by setting the DOZEN bit (CLKDIV<11>). The ratio between peripheral and core clock speed is determined by the DOZE<2:0> bits (CLKDIV<14:12>). There are eight possible configurations, from 1:1 to 1:128, with 1:1 being the default setting.

Programs can use Doze mode to selectively reduce power consumption in event-driven applications. This allows clock-sensitive functions, such as synchronous communications, to continue without interruption while the CPU Idles, waiting for something to invoke an interrupt routine. An automatic return to full-speed CPU operation on interrupts can be enabled by setting the ROI bit (CLKDIV<15>). By default, interrupt events have no effect on Doze mode operation.

For example, suppose the device is operating at 20 MIPS and the ECAN[™] module has been configured for 500 kbps, based on this device operating speed. If the device is placed in Doze mode with a clock frequency ratio of 1:4, the ECAN module continues to communicate at the required bit rate of 500 kbps, but the CPU now starts executing instructions at a frequency of 5 MIPS.

10.4 Peripheral Module Disable

The Peripheral Module Disable (PMD) registers provide a method to disable a peripheral module by stopping all clock sources supplied to that module. When a peripheral is disabled using the appropriate PMD control bit, the peripheral is in a minimum power consumption state. The control and status registers associated with the peripheral are also disabled, so writes to those registers do not have effect and read values are invalid.

A peripheral module is enabled only if both the associated bit in the PMD register is cleared and the peripheral is supported by the specific dsPIC[®] DSC variant. If the peripheral is present in the device, it is enabled in the PMD register by default.

Note:	If a PMD bit is set, the corresponding
	module is disabled after a delay of one
	instruction cycle. Similarly, if a PMD bit is
	cleared, the corresponding module is
	enabled after a delay of one instruction
	cycle (assuming the module control regis-
	ters are already configured to enable
	module operation).

10.5 Power-Saving Resources

Many useful resources are provided on the main product page of the Microchip web site for the devices listed in this data sheet. This product page, which can be accessed using this link, contains the latest updates and additional information.



10.5.1 KEY RESOURCES

- "Watchdog Timer and Power-Saving Modes" (DS70615) in the "dsPIC33/PIC24 Family Reference Manual"
- Code Samples
- Application Notes
- Software Libraries
- Webinars
- All Related "dsPIC33/PIC24 Family Reference Manual" Sections
- Development Tools

REGISTER 10-1: PMD1: PERIPHERAL MODULE DISABLE CONTROL REGISTER 1 (CONTINUED)

- bit 3 SPI1MD: SPI1 Module Disable bit 1 = SPI1 module is disabled
 - 0 = SPI1 module is enabled
- bit 2 Unimplemented: Read as '0'
- bit 1 C1MD: ECAN1 Module Disable bit⁽²⁾ 1 = ECAN1 module is disabled 0 = ECAN1 module is enabled
- bit 0 AD1MD: ADC1 Module Disable bit 1 = ADC1 module is disabled 0 = ADC1 module is enabled
- Note 1: This bit is available on dsPIC33EPXXXMC20X/50X and PIC24EPXXXMC20X devices only.
 - 2: This bit is available on dsPIC33EPXXXGP50X and dsPIC33EPXXXMC50X devices only.

U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
—	—	—	_	—	—	—	—
bit 15				·	-		bit 8
U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
				SS2R<6:0>			
bit 7	<u>.</u>						bit 0
Logondi							

REGISTER 11-13: RPINR23: PERIPHERAL PIN SELECT INPUT REGISTER 23

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read	l as '0'
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15-7	Unimplemented: Read as '0'
bit 6-0	SS2R<6:0>: Assign SPI2 Slave Select (SS2) to the Corresponding RPn Pin bits (see Table 11-2 for input pin selection numbers)
	1111001 = Input tied to RPI121
	•
	0000001 = Input tied to CMP1 0000000 = Input tied to Vss

REGISTER 11-14: RPINR26: PERIPHERAL PIN SELECT INPUT REGISTER 26 (dsPIC33EPXXXGP/MC50X DEVICES ONLY)

U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
—	—	—	—	—	_	—	—
bit 15							bit 8
U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
—				C1RXR<6:0>	>		
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read	as '0'
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15-7	Unimplemented: Read as '0'
bit 6-0	C1RXR<6:0>: Assign CAN1 RX Input (CRX1) to the Corresponding RPn Pin bits (see Table 11-2 for input pin selection numbers)
	1111001 = Input tied to RPI121
	•
	0000001 = Input tied to CMP1 0000000 = Input tied to Vss

13.0 TIMER2/3 AND TIMER4/5

- Note 1: This data sheet summarizes the features of the dsPIC33EPXXXGP50X, dsPIC33EPXXXMC20X/50X and PIC24EPXXXGP/MC20X family of devices. It is not intended to be a comprehensive reference source. To complement the information in this data sheet, refer to "Timers" (DS70362) of the "dsPIC33/PIC24 Family Reference Manual", which is available from the Microchip web site (www.microchip.com).
 - 2: Some registers and associated bits described in this section may not be available on all devices. Refer to **Section 4.0 "Memory Organization"** in this data sheet for device-specific register and bit information.

The Timer2/3 and Timer4/5 modules are 32-bit timers, which can also be configured as four independent 16-bit timers with selectable operating modes.

As 32-bit timers, Timer2/3 and Timer4/5 operate in three modes:

- Two Independent 16-Bit Timers (e.g., Timer2 and Timer3) with all 16-Bit Operating modes (except Asynchronous Counter mode)
- Single 32-Bit Timer
- Single 32-Bit Synchronous Counter
- They also support these features:
- Timer Gate Operation
- Selectable Prescaler Settings
- Timer Operation during Idle and Sleep modes
- Interrupt on a 32-Bit Period Register Match
- Time Base for Input Capture and Output Compare Modules (Timer2 and Timer3 only)
- ADC1 Event Trigger (32-bit timer pairs, and Timer3 and Timer5 only)

Individually, all four of the 16-bit timers can function as synchronous timers or counters. They also offer the features listed previously, except for the event trigger; this is implemented only with Timer2/3. The operating modes and enabled features are determined by setting the appropriate bit(s) in the T2CON, T3CON, and T4CON, T5CON registers. T2CON and T4CON are shown in generic form in Register 13-1. T3CON and T5CON are shown in Register 13-2.

For 32-bit timer/counter operation, Timer2 and Timer4 are the least significant word (lsw); Timer3 and Timer5 are the most significant word (msw) of the 32-bit timers.

Note: For 32-bit operation, T3CON and T5CON control bits are ignored. Only T2CON and T4CON control bits are used for setup and control. Timer2 and Timer4 clock and gate inputs are utilized for the 32-bit timer modules, but an interrupt is generated with the Timer3 and Timer5 interrupt flags.

A block diagram for an example 32-bit timer pair (Timer2/3 and Timer4/5) is shown in Figure 13-3.

Note: Only Timer2, 3, 4 and 5 can trigger a DMA data transfer.

REGISTER 16-13: IOCONX: PWMx I/O CONTROL REGISTER⁽²⁾ (CONTINUED)

- bit 1 SWAP: SWAP PWMxH and PWMxL Pins bit
 1 = PWMxH output signal is connected to PWMxL pins; PWMxL output signal is connected to PWMxH pins
 0 = PWMxH and PWMxL pins are mapped to their respective pins
 bit 0 OSYNC: Output Override Synchronization bit
 1 = Output overrides via the OVRDAT<1:0> bits are synchronized to the PWMx period boundary
 - 0 = Output overrides via the OVDDAT<1:0> bits occur on the next CPU clock boundary
- Note 1: These bits should not be changed after the PWMx module is enabled (PTEN = 1).
 - 2: If the PWMLOCK Configuration bit (FOSCSEL<6>) is a '1', the IOCONx register can only be written after the unlock sequence has been executed.

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	U-0	U-0
PHR	PHF	PLR	PLF	FLTLEBEN	CLLEBEN	_	_
bit 15	1		1		1		bit 8
U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
—	—	BCH(")	BCL	BPHH	BPHL	BPLH	BPLL
bit 7							bit 0
Legend:							
R = Readable	bit	W = Writable	bit	U = Unimpler	mented bit, read	as '0'	
-n = Value at F	POR	'1' = Bit is set		'0' = Bit is cle	ared	x = Bit is unkr	nown
bit 15	PHR: PWMxH	Rising Edge	Trigger Enabl	e bit			
	\perp = Rising edg 0 = Leading-E	ge of PyvivixH v Edge Blanking i	anores risina	edge of PWM	anking counter kH		
bit 14	PHF: PWMxH	Falling Edge	Trigger Enabl	e bit			
	1 = Falling ed	ge of PWMxH	will trigger Le	ading-Edge Bla	anking counter		
	0 = Leading-E	Edge Blanking i	gnores falling	g edge of PWM	хH		
bit 13	PLR: PWMxL	. Rising Edge T	rigger Enable	e bit oding Edgo Blo	nking countor		
	0 = Leading-E	Edge Blanking i	gnores rising	edge of PWM	kL		
bit 12	PLF: PWMxL	Falling Edge T	rigger Enable	e bit			
	1 = Falling ed	ge of PWMxL	will trigger Le	ading-Edge Bla	anking counter		
	0 = Leading-E	Edge Blanking i	gnores falling	g edge of PWM	xL		
bit 11	1 = Leading-F	-ault Input Lea Edge Blanking i	ding-Edge Bla	anking Enable	bit		
	0 = Leading-E	Edge Blanking i	s not applied	to selected Fa	ult input		
bit 10	CLLEBEN: C	urrent-Limit Le	ading-Edge E	Blanking Enable	e bit		
	1 = Leading-E	Edge Blanking i	s applied to s	selected curren	t-limit input		
hit 0.6	0 = Leading-E	tode Blanking I	s not applied	to selected cul	rrent-limit input		
bit 5	BCH Blankin	a in Selected F	J Blanking Sign	al High Enable	hit(1)		
bit 5	1 = State blan	kina (of curren	t-limit and/or	Fault input sigr	nals) when seled	ted blanking s	ianal is hiah
	0 = No blankii	ng when select	ed blanking s	signal is high	,	5	0 0
bit 4	BCL: Blanking	g in Selected B	lanking Signa	al Low Enable I	bit ⁽¹⁾		
	1 = State blan	iking (of curren	t-limit and/or	Fault input sigr	nals) when seled	cted blanking s	ignal is low
bit 3	BPHH: Blanki	ing in PWMxH	High Enable	hit			
bit o	1 = State blan	iking (of curren	t-limit and/or	Fault input sigr	nals) when PWN	/IxH output is h	igh
	0 = No blanki	ng when PWM	xH output is h	nigh			-
bit 2	BPHL: Blanki	ng in PWMxH	Low Enable b	pit			
	1 = State blan 0 = No blankii	nking (of curren ng when PWM	t-limit and/or xH output is le	Fault input sigr ow	nals) when PWN	IxH output is lo	W
bit 1	BPLH: Blanki	ng in PWMxL I	High Enable b	oit			
	1 = State blan 0 = No blankii	nking (of curren ng when PWM	t-limit and/or xL output is h	Fault input sigr igh	nals) when PWN	/IxL output is hi	igh
bit 0	BPLL: Blanki	ng in PWMxL L	ow Enable b	it			
	1 = State blan	king (of curren	t-limit and/or	Fault input sigr	nals) when PWN	IxL output is lo	W
	v = i N o diankii		x∟ output is io	JW			

REGISTER 16-16: LEBCONX: PWMx LEADING-EDGE BLANKING CONTROL REGISTER

Note 1: The blanking signal is selected via the BLANKSELx bits in the AUXCONx register.

REGISTER 17-7: VEL1CNT: VELOCITY COUNTER 1 REGISTER

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
			VELC	NT<15:8>			
bit 15							bit 8
R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
			VELC	NT<7:0>			
bit 7							bit 0
Legend:							
R = Readable bit W = Writable bit U = Unimplemented bit, read as '0'							
-n = Value at POR (1' = Bit is set (0' = Bit is cleared x = Bit is unknown					nown		

bit 15-0 VELCNT<15:0>: Velocity Counter bits

REGISTER 17-8: INDX1CNTH: INDEX COUNTER 1 HIGH WORD REGISTER

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
			INDXCN	T<31:24>			
bit 15							bit 8
R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
			INDXCN	T<23:16>			
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit	, read as '0'
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15-0 INDXCNT<31:16>: High Word Used to Form 32-Bit Index Counter Register (INDX1CNT) bits

REGISTER 17-9: INDX1CNTL: INDEX COUNTER 1 LOW WORD REGISTER

'1' = Bit is set

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
			INDXC	NT<15:8>			
bit 15							bit 8
R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
			INDXC	NT<7:0>			
bit 7							bit 0
Legend:							
R = Readable b	it	W = Writable bit		U = Unimpler	mented bit, read	l as '0'	

'0' = Bit is cleared

bit 15-0 INDXCNT<15:0>: Low Word Used to Form 32-Bit Index Counter Register (INDX1CNT) bits

-n = Value at POR

x = Bit is unknown

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
			QEIGE	EC<31:24>			
bit 15							bit 8
R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
			QEIGE	EC<23:16>			
bit 7							bit 0
Legend:							
R = Readable	bit	W = Writable	bit	U = Unimplen	nented bit, read	d as '0'	
-n = Value at POR '1' = Bit is set			'0' = Bit is clea	ared	x = Bit is unkr	nown	

REGISTER 17-15: QEI1GECH: QEI1 GREATER THAN OR EQUAL COMPARE HIGH WORD REGISTER

bit 15-0 QEIGEC<31:16>: High Word Used to Form 32-Bit Greater Than or Equal Compare Register (QEI1GEC) bits

REGISTER 17-16: QEI1GECL: QEI1 GREATER THAN OR EQUAL COMPARE LOW WORD REGISTER

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
			QEIGE	C<15:8>			
bit 15							bit 8
R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
			QEIG	EC<7:0>			
bit 7							bit 0
Legend:							
R = Readable bit W = Writable bit		bit	U = Unimplei	mented bit, rea	id as '0'		
-n = Value at POR '1' = Bit is set		'0' = Bit is cle	eared	x = Bit is unkr	nown		

bit 15-0 QEIGEC<15:0>: Low Word Used to Form 32-Bit Greater Than or Equal Compare Register (QEI1GEC) bits

REGISTER 17-17: INT1TMRH: INTERVAL 1 TIMER HIGH WORD REGISTER

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
			INTTM	R<31:24>			
bit 15							bit 8
R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
			INTTM	R<23:16>			
bit 7							bit 0
Legend:							
R = Readable bit W = Writable bit U = Unimplemented bit, read as '0'							
-n = Value at POR '1' = Bit is set '0' = Bit is cleared x = Bit is unknown					nown		

bit 15-0 INTTMR<31:16>: High Word Used to Form 32-Bit Interval Timer Register (INT1TMR) bits

REGISTER 17-18: INT1TMRL: INTERVAL 1 TIMER LOW WORD REGISTER

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
			INTTM	1R<15:8>			
bit 15							bit 8
R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
			INTT	/IR<7:0>			
bit 7							bit 0
Legend:							
R = Readable bit W = Writable bit U = Unimplemented bit, read as '0'							
-n = Value at POR '1' = Bit is set '0' = Bit is cleared x = Bit is unknown				nown			

bit 15-0 INTTMR<15:0>: Low Word Used to Form 32-Bit Interval Timer Register (INT1TMR) bits

20.1 UART Helpful Tips

- 1. In multi-node, direct-connect UART networks, receive inputs UART react to the complementary logic level defined by the URXINV bit (UxMODE<4>), which defines the Idle state, the default of which is logic high (i.e., URXINV = 0). Because remote devices do not initialize at the same time, it is likely that one of the devices, because the RX line is floating, will trigger a Start bit detection and will cause the first byte received, after the device has been initialized, to be invalid. To avoid this situation, the user should use a pull-up or pull-down resistor on the RX pin depending on the value of the URXINV bit.
 - a) If URXINV = 0, use a pull-up resistor on the RX pin.
 - b) If URXINV = 1, use a pull-down resistor on the RX pin.
- 2. The first character received on a wake-up from Sleep mode caused by activity on the UxRX pin of the UARTx module will be invalid. In Sleep mode, peripheral clocks are disabled. By the time the oscillator system has restarted and stabilized from Sleep mode, the baud rate bit sampling clock, relative to the incoming UxRX bit timing, is no longer synchronized, resulting in the first character being invalid; this is to be expected.

20.2 UART Resources

Many useful resources are provided on the main product page of the Microchip web site for the devices listed in this data sheet. This product page, which can be accessed using this link, contains the latest updates and additional information.

Note:	In the event you are not able to access the
	product page using the link above, enter
	this URL in your browser:
	http://www.microchip.com/wwwproducts/
	Devices.aspx?dDocName=en555464

20.2.1 KEY RESOURCES

- "UART" (DS70582) in the "dsPIC33/PIC24 Family Reference Manual"
- Code Samples
- Application Notes
- Software Libraries
- Webinars
- All Related "dsPIC33/PIC24 Family Reference Manual" Sections
- Development Tools

21.2 Modes of Operation

The ECAN module can operate in one of several operation modes selected by the user. These modes include:

- · Initialization mode
- Disable mode
- Normal Operation mode
- · Listen Only mode
- Listen All Messages mode
- Loopback mode

Modes are requested by setting the REQOP<2:0> bits (CxCTRL1<10:8>). Entry into a mode is Acknowledged by monitoring the OPMODE<2:0> bits (CxCTRL1<7:5>). The module does not change the mode and the OPMODEx bits until a change in mode is acceptable, generally during bus Idle time, which is defined as at least 11 consecutive recessive bits.

21.3 ECAN Resources

Many useful resources are provided on the main product page of the Microchip web site for the devices listed in this data sheet. This product page, which can be accessed using this link, contains the latest updates and additional information.

Note:	In the event you are not able to access the
	product page using the link above, enter
	this URL in your browser:
	http://www.microchip.com/wwwproducts/
	Devices.aspx?dDocName=en555464

21.3.1 KEY RESOURCES

- "Enhanced Controller Area Network (ECAN™)" (DS70353) in the "dsPIC33/PIC24 Family Reference Manual"
- · Code Samples
- Application Notes
- Software Libraries
- Webinars
- All Related *"dsPIC33/PIC24 Family Reference Manual"* Sections
- · Development Tools

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0		
F15BP<3:0>			F14BP<3:0>						
bit 15						bit 8			
R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0		
F13BP<3:0> F12			F12B	P<3:0>					
bit 7							bit 0		
Legend:									
R = Readab	le bit	W = Writable	W = Writable bit		U = Unimplemented bit, read as '0'				
-n = Value a	t POR	'1' = Bit is set		'0' = Bit is cleared		x = Bit is unknown			
L									
bit 15-12	F15BP<3:0	>: RX Buffer Ma	sk for Filter 1	5 bits					
	1111 = Filte	er hits received in	n RX FIFO bu	uffer					
	1110 = Filte	r hits received in	n RX Buffer 1	4					
	•								
	•								
	•	n hito no ocivio d iv							
	0001 = Filte	r hits received ii							
h:+ 44 0				4 h:ta (a a ma a ma)					
DIT 11-8	F14BP<3:0	F14BP<3:0>: RX Butter Mask for Filter 14 bits (same values as bits<15:12>)							
bit 7-4	F13BP<3:0>: RX Buffer Mask for Filter 13 bits (same values as bits<15:12>)								
bit 3-0 F12BP<3:0>: RX Buffer Mask for Filter 12 bits (same values as bits<15:12>)									

REGISTER 21-15: CxBUFPNT4: ECANx FILTER 12-15 BUFFER POINTER REGISTER 4

REGISTER 25-4: CMxMSKSRC: COMPARATOR x MASK SOURCE SELECT CONTROL REGISTER

U-0	U-0	U-0	U-0	R/W-0	R/W-0	R/W-0	RW-0
—	—	—	—	SELSRCC3	SELSRCC2	SELSRCC1	SELSRCC0
bit 15							bit 8

| R/W-0 |
|----------|----------|----------|----------|----------|----------|----------|----------|
| SELSRCB3 | SELSRCB2 | SELSRCB1 | SELSRCB0 | SELSRCA3 | SELSRCA2 | SELSRCA1 | SELSRCA0 |
| bit 7 | | | | | | | bit 0 |

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read	as '0'
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15-12 Unimplemented: Read as '0'

bit 11-8	SELSRCC<3:0>: Mask C Input Select bits
	1111 = FLT4
	1110 = FLT2
	1101 = PTGO19
	1100 = PTGO18
	1011 = Reserved
	1010 = Reserved
	1001 = Reserved
	1000 = Reserved
	0111 = Reserved
	0110 = Reserved
	0101 = PWM3H
	0100 = PWM3L
	0011 = PWM2H
	0010 = PWM2L
	0001 = PWM1H
	0000 = PWM1L
bit 7-4	SELSRCB<3:0>: Mask B Input Select bits
bit 7-4	SELSRCB<3:0>: Mask B Input Select bits 1111 = FLT4
bit 7-4	SELSRCB<3:0>: Mask B Input Select bits 1111 = FLT4 1110 = FLT2
bit 7-4	SELSRCB<3:0>: Mask B Input Select bits 1111 = FLT4 1110 = FLT2 1101 = PTGO19
bit 7-4	SELSRCB<3:0>: Mask B Input Select bits 1111 = FLT4 1110 = FLT2 1101 = PTGO19 1100 = PTGO18
bit 7-4	SELSRCB<3:0>: Mask B Input Select bits 1111 = FLT4 1110 = FLT2 1101 = PTGO19 1100 = PTGO18 1011 = Reserved
bit 7-4	SELSRCB<3:0>: Mask B Input Select bits 1111 = FLT4 1110 = FLT2 1101 = PTGO19 1100 = PTGO18 1011 = Reserved 1010 = Reserved
bit 7-4	SELSRCB<3:0>: Mask B Input Select bits 1111 = FLT4 1110 = FLT2 1101 = PTGO19 1100 = PTGO18 1011 = Reserved 1010 = Reserved 1001 = Reserved
bit 7-4	SELSRCB<3:0>: Mask B Input Select bits 1111 = FLT4 1110 = FLT2 1101 = PTGO19 1100 = PTGO18 1011 = Reserved 1010 = Reserved 1001 = Reserved 1000 = Reserved
bit 7-4	SELSRCB<3:0>: Mask B Input Select bits 1111 = FLT4 1110 = FLT2 1101 = PTGO19 1100 = PTGO18 1011 = Reserved 1001 = Reserved 1000 = Reserved 0011 = Reserved 0111 = Reserved
bit 7-4	SELSRCB<3:0>: Mask B Input Select bits 1111 = FLT4 1110 = FLT2 1101 = PTGO19 1100 = PTGO18 1011 = Reserved 1010 = Reserved 1001 = Reserved 1000 = Reserved 0111 = Reserved 0110 = Reserved 0110 = Reserved
bit 7-4	SELSRCB<3:0>: Mask B Input Select bits 1111 = FLT4 1110 = FLT2 1101 = PTGO19 1100 = PTGO18 1011 = Reserved 1010 = Reserved 1000 = Reserved 1000 = Reserved 0111 = Reserved 0110 = Reserved 0110 = Reserved 0110 = PWM3H 0100 = PWM3I
bit 7-4	SELSRCB<3:0>: Mask B Input Select bits 1111 = FLT4 1110 = FLT2 1101 = PTGO19 1100 = PTGO18 1011 = Reserved 1010 = Reserved 1000 = Reserved 0111 = Reserved 0111 = Reserved 0110 = Reserved 0110 = PWM3H 0100 = PWM3L 0011 = PWM2H
bit 7-4	SELSRCB<3:0>: Mask B Input Select bits 1111 = FLT4 1110 = FLT2 1101 = PTGO19 1100 = PTGO18 1011 = Reserved 1010 = Reserved 1001 = Reserved 0101 = Reserved 0111 = Reserved 0110 = Reserved 0110 = PWM3H 0100 = PWM3L 0011 = PWM2H 0010 = PWM2I
bit 7-4	SELSRCB<3:0>: Mask B Input Select bits 1111 = FLT4 1110 = FLT2 1101 = PTGO19 1100 = PTGO18 1011 = Reserved 1010 = Reserved 1001 = Reserved 0101 = Reserved 0111 = Reserved 0110 = Reserved 0110 = PWM3H 0100 = PWM3L 0011 = PWM2H 0010 = PWM2L 0001 = PWM1H
bit 7-4	SELSRCB<3:0>: Mask B Input Select bits 1111 = FLT4 1110 = FLT2 1101 = PTGO19 1100 = PTGO18 1011 = Reserved 1010 = Reserved 1001 = Reserved 0101 = Reserved 0111 = Reserved 0110 = Reserved 0110 = PWM3H 0100 = PWM3L 0011 = PWM2H 0010 = PWM2L 0001 = PWM1H 0000 = PWM1I



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28-Lead Plastic Small Outline (SO) - Wide, 7.50 mm Body [SOIC]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging





	MILLIMETERS					
Dimension	MIN	NOM	MAX			
Number of Pins	N		28			
Pitch	е	1.27 BSC				
Overall Height	Α	-	-	2.65		
Molded Package Thickness	A2	2.05	-	-		
Standoff §	A1	0.10	-	0.30		
Overall Width	E	10.30 BSC				
Molded Package Width	E1	7.50 BSC				
Overall Length	D	17.90 BSC				
Chamfer (Optional)	h	0.25	-	0.75		
Foot Length	L	0.40	-	1.27		
Footprint	L1	1.40 REF				
Lead Angle	Θ	0°	-	-		
Foot Angle	φ	0°	-	8°		
Lead Thickness	С	0.18	-	0.33		
Lead Width	b	0.31	-	0.51		
Mold Draft Angle Top	α	5°	-	15°		
Mold Draft Angle Bottom	β	5°	-	15°		

Notes:

- 1. Pin 1 visual index feature may vary, but must be located within the hatched area.
- 2. § Significant Characteristic
- 3. Dimension D does not include mold flash, protrusions or gate burrs, which shall not exceed 0.15 mm per end. Dimension E1 does not include interlead flash or protrusion, which shall not exceed 0.25 mm per side.
- 4. Dimensioning and tolerancing per ASME Y14.5M
 - BSC: Basic Dimension. Theoretically exact value shown without tolerances. REF: Reference Dimension, usually without tolerance, for information purposes only.
- 5. Datums A & B to be determined at Datum H.

Microchip Technology Drawing C04-052C Sheet 2 of 2