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#### What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

### Applications of "<u>Embedded -</u> <u>Microcontrollers</u>"

#### Details

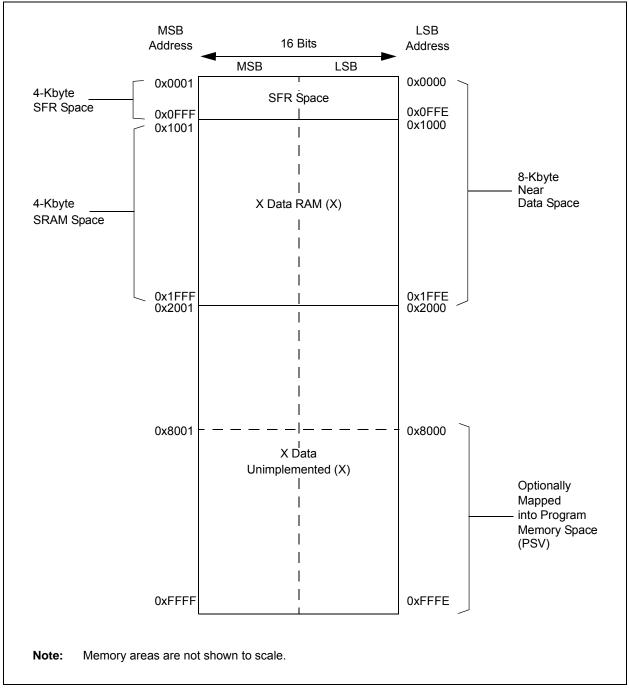
Details	
Product Status	Obsolete
Core Processor	PIC
Core Size	16-Bit
Speed	60 MIPs
Connectivity	I <sup>2</sup> C, IrDA, LINbus, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, DMA, POR, PWM, WDT
Number of I/O	25
Program Memory Size	32KB (10.7K x 24)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	2K x 16
Voltage - Supply (Vcc/Vdd)	3V ~ 3.6V
Data Converters	A/D 8x10b/12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 150°C (TA)
Mounting Type	Surface Mount
Package / Case	36-VFTLA Exposed Pad
Supplier Device Package	36-VTLA (5x5)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/pic24ep32gp203-h-tl

Email: info@E-XFL.COM

Address: Room A, 16/F, Full Win Commercial Centre, 573 Nathan Road, Mongkok, Hong Kong



### FIGURE 4-5: PROGRAM MEMORY MAP FOR dsPIC33EP512GP50X, dsPIC33EP512MC20X/50X AND PIC24EP512GP/MC20X DEVICES





### TABLE 4-5: INTERRUPT CONTROLLER REGISTER MAP FOR dsPIC33EPXXXGP50X DEVICES ONLY (CONTINUED)

File Name	Addr.	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	All Resets
INTCON1	08C0	NSTDIS	OVAERR	OVBERR	COVAERR	COVBERR	OVATE	OVBTE	COVTE	SFTACERR	DIV0ERR	DMACERR	MATHERR	ADDRERR	STKERR	OSCFAIL		0000
INTCON2	08C2	GIE	DISI	SWTRAP	_	_	_	_	_	_	—	_	_	—	INT2EP	INT1EP	INT0EP	8000
INTCON3	08C4		_	_	—	_	_		_	_	—	DAE	DOOVR	—	_	_		0000
INTCON4	08C6		_				Ι	_			—	_		—			SGHT	0000
INTTREG	08C8	_	_	_	_		ILR<	3:0>					VECNU	M<7:0>				0000

**Legend:** — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

R/W-0	R/W-0	R/W-0	R/W-0	R/C-0	R/C-0	R-0	R/W-0
OA	OB	SA	SB	OAB	SAB	DA	DC
bit 15							bit 8
R/W-0 <sup>(3)</sup>	R/W-0 <sup>(3)</sup>	R/W-0 <sup>(3)</sup>	R-0	R/W-0	R/W-0	R/W-0	R/W-0
	IPL<2:0> <sup>(2)</sup>		RA	Ν	OV	Z	С
bit 7							bit 0

## REGISTER 7-1: SR: CPU STATUS REGISTER<sup>(1)</sup>

Legend:	gend: C = Clearable bit					
R = Readable bit	W = Writable bit	U = Unimplemented bit	t, read as '0'			
-n = Value at POR	'1'= Bit is set	'0' = Bit is cleared	x = Bit is unknown			

bit 7-5	IPL<2:0>: CPU Interrupt Priority Level Status bits <sup>(2,3)</sup>
	111 = CPU Interrupt Priority Level is 7 (15); user interrupts are disabled
	110 = CPU Interrupt Priority Level is 6 (14)
	101 = CPU Interrupt Priority Level is 5 (13)
	100 = CPU Interrupt Priority Level is 4 (12)
	011 = CPU Interrupt Priority Level is 3 (11)
	010 = CPU Interrupt Priority Level is 2 (10)
	001 = CPU Interrupt Priority Level is 1 (9)
	000 = CPU Interrupt Priority Level is 0 (8)

- **Note 1:** For complete register details, see Register 3-1.
  - 2: The IPL<2:0> bits are concatenated with the IPL<3> bit (CORCON<3>) to form the CPU Interrupt Priority Level. The value in parentheses indicates the IPL, if IPL<3> = 1. User interrupts are disabled when IPL<3> = 1.
  - **3:** The IPL<2:0> Status bits are read-only when the NSTDIS bit (INTCON1<15>) = 1.

U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0		
—				IC4R<6:0>					
bit 15							bit 8		
U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0		
—				IC3R<6:0>					
bit 7							bit C		
Legend:									
R = Readable bit W = Writable bit U = Unimplemented bit, read as '0'									
-n = Value a	at POR	'1' = Bit is set		'0' = Bit is clea	ared	x = Bit is unkr	nown		
	0000001 =	nput tied to RPI nput tied to CMI nput tied to Vss	⊃1						
bit 7	Unimpleme	nted: Read as 'o	)'						
bit 6-0	(see Table 1	Assign Input Ca 1-2 for input pin nput tied to RPI	selection nun		onding RPn Pi	n bits			

### REGISTER 11-5: RPINR8: PERIPHERAL PIN SELECT INPUT REGISTER 8

				DD20			
U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
bit 15							bit 8
				RP35	iR<5:0>		
U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0

### REGISTER 11-18: RPOR0: PERIPHERAL PIN SELECT OUTPUT REGISTER 0

U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0					
—	—		RP20R<5:0>									
bit 7							bit 0					

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit	t, read as '0'
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15-14	Unimplemented: Read as '0'
bit 13-8	<b>RP35R&lt;5:0&gt;:</b> Peripheral Output Function is Assigned to RP35 Output Pin bits (see Table 11-3 for peripheral function numbers)
bit 7-6	Unimplemented: Read as '0'
bit 5-0	<b>RP20R&lt;5:0&gt;:</b> Peripheral Output Function is Assigned to RP20 Output Pin bits (see Table 11-3 for peripheral function numbers)

### REGISTER 11-19: RPOR1: PERIPHERAL PIN SELECT OUTPUT REGISTER 1

U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
—	—			RP37	′R<5:0>		
bit 15							bit 8

U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0			
—	—		RP36R<5:0>							
bit 7							bit 0			

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit	, read as '0'
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15-14	Unimplemented: Read as '0'
bit 13-8	<b>RP37R&lt;5:0&gt;:</b> Peripheral Output Function is Assigned to RP37 Output Pin bits (see Table 11-3 for peripheral function numbers)
bit 7-6	Unimplemented: Read as '0'
bit 5-0	<b>RP36R&lt;5:0&gt;:</b> Peripheral Output Function is Assigned to RP36 Output Pin bits (see Table 11-3 for peripheral function numbers)

### REGISTER 16-8: PDCx: PWMx GENERATOR DUTY CYCLE REGISTER

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
			PDC	<15:8>			
bit 15							bit 8
R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
			PDC	x<7:0>			
bit 7							bit 0
Legend:							
R = Readable	bit	W = Writable b	oit	U = Unimpler	mented bit, rea	d as '0'	
-n = Value at POR '1' = Bit is set '0' = Bit is cleared x = Bit is unkn		nown					

bit 15-0 **PDCx<15:0>:** PWMx Generator # Duty Cycle Value bits

### REGISTER 16-9: PHASEx: PWMx PRIMARY PHASE-SHIFT REGISTER

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
			PHAS	Ex<15:8>			
bit 15							bit 8
R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
			PHAS	SEx<7:0>			
bit 7							bit 0
Legend:							
R = Readable	bit	W = Writable b	pit	U = Unimplen	nented bit, rea	ad as '0'	
-n = Value at POR '1' = Bit is set			'0' = Bit is cleared x = Bit is unknow			nown	

bit 15-0 PHASEx<15:0>: PWMx Phase-Shift Value or Independent Time Base Period for the PWM Generator bits

Note 1: If ITB (PWMCONx<9>) = 0, the following applies based on the mode of operation: Complementary, Redundant and Push-Pull Output mode (PMOD<1:0> (IOCON<11:10>) = 00, 01 or 10), PHASEx<15:0> = Phase-shift value for PWMxH and PWMxL outputs

 If ITB (PWMCONx<9>) = 1, the following applies based on the mode of operation: Complementary, Redundant and Push-Pull Output mode (PMOD<1:0> (IOCONx<11:10>) = 00, 01 or 10), PHASEx<15:0> = Independent time base period value for PWMxH and PWMxL

U-0       R/W-0       R/W       R/W       R/W </th <th>R/W-0</th> <th>R/W-0</th> <th>R/W-0</th> <th>R/W-0</th> <th>R/W-0</th> <th>R/W-0</th> <th>U-0</th> <th>U-0</th>	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	U-0	U-0
U-0       U-0       RW-0       <	PHR	PHF	PLR	PLF	FLTLEBEN	CLLEBEN	—	_
-         BCH <sup>(1)</sup> BCL <sup>(1)</sup> BPH         BPHL         BPLH         BPHH	bit 15							bit
bit 7       t         Legend:         R = Readable bit       W = Writable bit       U = Unimplemented bit, read as '0'         in = Value at POR       '1' = Bit is set       '0' = Bit is cleared       x = Bit is unknown         bit 15       PHR: PWMxH Rising Edge Trigger Enable bit       1 = Rising edge of PWMxH will trigger Leading-Edge Blanking counter       0 = Leading-Edge Blanking ignores rising edge of PWMxH         bit 14       PHF: PWMxH Falling Edge Trigger Enable bit       1 = Falling edge of PWMxH will trigger Leading-Edge Blanking counter         0 = Leading-Edge Blanking ignores falling edge of PWMxL       1 = Rising edge of PWMxL will trigger Leading-Edge Blanking counter         0 = Leading-Edge Blanking ignores rising edge of PWMxL       1 = Rising edge of PWMxL will trigger Leading-Edge Blanking counter         0 = Leading-Edge Blanking ignores falling edge of PWMxL       1 = Falling edge of PWMxL will trigger Leading-Edge Blanking counter         0 = Leading-Edge Blanking is applied to selected Fault input       1 = Leading-Edge Blanking is applied to selected Fault input         0 = Leading-Edge Blanking is not applied to selected Current-limit input       0 = Leading-Edge Blanking is applied to selected current-limit input         0 = Leading-Edge Blanking is applied to selected current-limit input       0 = Leading-Edge Blanking is applied to selected current-limit input         0 = Leading-Edge Blanking is applied to selected Current-limit input       0 = Leading-Edge Blanking is applied to sel	U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
Legend: R = Readable bit W = Writable bit U = Unimplemented bit, read as '0' nn = Value at POR '1' = Bit is set '0' = Bit is cleared x = Bit is unknown bit 15 PHR: PWMxH Rising Edge Trigger Enable bit 1 = Rising edge of PWMxH will trigget Leading-Edge Blanking counter 0 = Leading-Edge Blanking ignores rising edge of PWMxH 1 = Falling edge of PWMxH will trigget Leading-Edge Blanking counter 0 = Leading-Edge Blanking ignores rising edge of PWMxH 1 = Falling edge of PWMxH will trigget Leading-Edge Blanking counter 0 = Leading-Edge Blanking ignores falling edge of PWMxH 1 = Rising edge of PWMxH will trigget Leading-Edge Blanking counter 0 = Leading-Edge Blanking ignores rising edge of PWMxL 1 = Rising edge of PWMxL will trigget Leading-Edge Blanking counter 0 = Leading-Edge Blanking ignores rising edge of PWMxL 1 = Falling edge of PWMxL will trigget Leading-Edge Blanking counter 0 = Leading-Edge Blanking ignores rising edge of PWMxL 1 = Falling edge of PWMxL will trigget Leading-Edge Blanking counter 0 = Leading-Edge Blanking ignores falling edge of PWMxL 1 = Falling edge of PWMxL will trigget Leading-Edge Blanking counter 0 = Leading-Edge Blanking ignores falling edge of PWMxL 1 = Leading-Edge Blanking is applied to selected Fault input 0 = Leading-Edge Blanking is applied to selected Fault input 1 = Leading-Edge Blanking is applied to selected Current-limit input 1 = Leading-Edge Blanking is not applied to selected current-limit input 1 = State blanking (of current-limit and/or Fault input signals) when selected blanking signal is high 1 = State blanking (of current-limit and/or Fault input signals) when selected blanking signal is low 0 = No blanking when selected blanking signal Low Enable bit 1 = State blanking (of current-limit and/or Fault input signals) when Selected blanking signal is low 0 = No blanking when PWMxH dupt is high 0 = No blanking when PWMxH dupt signals) when PWMxH output is high 0 = No blanking when PWMxH tow Enable bit 1 = State blanking (of current-limit and/	_	_	BCH <sup>(1)</sup>	BCL <sup>(1)</sup>	BPHH	BPHL	BPLH	BPLL
R = Readable bit       W = Writable bit       U = Unimplemented bit, read as '0'         in = Value at POR       '1' = Bit is set       '0' = Bit is cleared       x = Bit is unknown         bit 15       PHR: PWMxH Rising Edge Trigger Enable bit       1 = Rising edge of PWMxH will trigger Leading-Edge Blanking counter       0 = Leading-Edge Blanking ignores rising edge of PWMxH         bit 14       PHF: PWMxH Falling Edge Trigger Enable bit       1 = Falling edge of PWMxH will trigger Leading-Edge Blanking counter       0 = Leading-Edge Blanking ignores falling edge of PWMxH         bit 13       PLR: PWMxL Rising Edge Trigger Enable bit       1 = Rising edge of PWMxL will trigger Leading-Edge Blanking counter       0 = Leading-Edge Blanking ignores rising edge of PWMxL         bit 13       PLR: PWMxL Falling Edge Trigger Enable bit       1 = Falling edge of PWMxL will trigger Leading-Edge Blanking counter       0 = Leading-Edge Blanking is not applied to selected Fault input         bit 11       FLTLEBEN: Fault Input Leading-Edge Blanking Enable bit       1 = Leading-Edge Blanking is not applied to selected current-limit input         bit 5       BCH: Blanking is not applied to selected current-limit input       0 = Leading-Edge Blanking is not applied to selected current-limit input         bit 9-6       Unimplemented: Read as '0'       1 = State blanking (of current-limit and/or Fault input signals) when selected blanking signal is high         bit 4       BCL: Blanking in Selected Blanking signal is high       1 = State blanking	bit 7							bit
n = Value at POR       '1' = Bit is set       '0' = Bit is cleared       x = Bit is unknown         bit 15       PHR: PWMxH Rising Edge Trigger Enable bit       1 = Rising edge of PWMxH will trigger Leading-Edge Blanking counter         0 = Leading-Edge Blanking ignores rising edge of PWMxH       11 = Falling edge of PWMxH will trigger Leading-Edge Blanking counter         0 = Leading-Edge Blanking ignores falling edge of PWMxH       11 = Rising edge of PWMxL will trigger Leading-Edge Blanking counter         0 = Leading-Edge Blanking ignores falling edge of PWMxL       1 = Rising edge of PWMxL will trigger Leading-Edge Blanking counter         0 = Leading-Edge Blanking ignores fising edge of PWMxL       0 = Leading-Edge Blanking ignores falling edge of PWMxL         bit 12       PLF: PWMxL Falling Edge Trigger Enable bit       1 = Rising edge of PWMxL will trigger Leading-Edge Blanking counter         0 = Leading-Edge Blanking ignores falling edge of PWMxL       0 = Leading-Edge Blanking ignores falling edge of PWMxL         bit 11       FLTLEBEN: Fault Input Leading-Edge Blanking Enable bit       1 = Leading-Edge Blanking is not applied to selected Fault input         0 = Leading-Edge Blanking is not applied to selected Fault input       0 = Leading-Edge Blanking is not applied to selected current-limit input         0 = Leading-Edge Blanking is not applied to selected current-limit input       0 = Leading-Edge Blanking signal Figh Enable bit         1 = State blanking in Selected Blanking Singal High Enable bit <sup>(1)</sup> 1 = State blanking in Sel	Legend:							
<ul> <li>PHR: PWMxH Rising Edge Trigger Enable bit         <ol> <li>Rising edge of PWMxH will trigger Leading-Edge Blanking counter</li></ol></li></ul>	R = Readabl	e bit	W = Writable	bit	U = Unimpler	mented bit, read	as '0'	
<ul> <li>1 = Rising edge of PWMxH will trigger Leading-Edge Blanking counter</li> <li>0 = Leading-Edge Blanking ignores rising edge of PWMxH</li> <li>PHF: PWMxH Falling Edge Trigger Enable bit</li> <li>1 = Falling edge of PWMxH will trigger Leading-Edge Blanking counter</li> <li>0 = Leading-Edge Blanking ignores falling edge of PWMxH</li> <li>PLR: PVMxL Rising Edge Trigger Enable bit</li> <li>1 = Rising edge of PWMxL will trigger Leading-Edge Blanking counter</li> <li>0 = Leading-Edge Blanking ignores rising edge of PWMxL</li> <li>PLF: PWMxL Falling Edge Trigger Enable bit</li> <li>1 = Falling edge of PWMxL will trigger Leading-Edge Blanking counter</li> <li>0 = Leading-Edge Blanking ignores rising edge of PWMxL</li> <li>Det Leading-Edge Blanking ignores ralling edge of PWMxL</li> <li>D = Leading-Edge Blanking is applied to selected Fault input</li> <li>0 = Leading-Edge Blanking is not applied to selected Fault input</li> <li>0 = Leading-Edge Blanking is not applied to selected current-limit input</li> <li>0 = Leading-Edge Blanking is not applied to selected current-limit input</li> <li>0 = Leading-Edge Blanking is not applied to selected current-limit input</li> <li>0 = Leading-Edge Blanking is not applied to selected current-limit input</li> <li>0 = Leading-Edge Blanking is not applied to selected current-limit input</li> <li>0 = Leading-Edge Blanking Signal High Enable bit</li> <li>1 = Leading-Edge Blanking Signal Liph Enable bit<sup>(1)</sup></li> <li>1 = State blanking (or current-limit and/or Fault input signals) when selected blanking signal is high</li> <li>0 = No blanking when selected blanking signal is low</li> <li>0 = No blanking when selected blanking signal is low</li> <li>0 = No blanking when selected blanking signal is low</li> <li>0 = No blanking when PWMxH output is high</li> <li>0 = No blanking when PWMxH output is high</li> <li>0 = No blanking when PWMxH output is high</li> <li>0 = No b</li></ul>	-n = Value at	POR	'1' = Bit is set	:	'0' = Bit is cle	ared	x = Bit is unkr	nown
<ul> <li>1 = Falling edge of PWMxH will trigger Leading-Edge Blanking counter</li> <li>0 = Leading-Edge Blanking ignores falling edge of PWMxH</li> <li>bit 13 PLR: PWMxL Rising Edge Trigger Enable bit</li> <li>1 = Rising edge of PWMxL. will trigger Leading-Edge Blanking counter</li> <li>0 = Leading-Edge Blanking ignores rising edge of PWMxL</li> <li>bit 12 PLF: PWMxL Falling Edge Trigger Enable bit</li> <li>1 = Falling edge of PWMxL. will trigger Leading-Edge Blanking counter</li> <li>0 = Leading-Edge Blanking ignores falling edge of PWMxL</li> <li>bit 12 FLTLEBEN: Fault Input Leading-Edge Blanking Counter</li> <li>0 = Leading-Edge Blanking is applied to selected Fault input</li> <li>0 = Leading-Edge Blanking is applied to selected Fault input</li> <li>0 = Leading-Edge Blanking is applied to selected Fault input</li> <li>0 = Leading-Edge Blanking is applied to selected current-limit input</li> <li>0 = Leading-Edge Blanking is applied to selected current-limit input</li> <li>0 = Leading-Edge Blanking is applied to selected current-limit input</li> <li>0 = Leading-Edge Blanking is applied to selected current-limit input</li> <li>0 = Leading-Edge Blanking is applied to selected current-limit input</li> <li>0 = Leading-Edge Blanking is applied to selected current-limit input</li> <li>0 = Leading-Edge Blanking is applied to selected current-limit input</li> <li>0 = Leading-Edge Blanking is applied to selected current-limit input</li> <li>0 = Leading-Edge Blanking is applied to selected current-limit input</li> <li>0 = Leading-Edge Blanking is applied to selected current-limit input</li> <li>0 = Leading-Edge Blanking is applied to selected current-limit input</li> <li>0 = Leading-Edge Blanking is applied to selected current-limit input</li> <li>0 = No blanking (of current-limit and/or Fault input signals) when selected blanking signal is low</li> <li>0 = No blanking when PWMxH output is nigh</li> <li>0 = No bla</li></ul>	bit 15	1 = Rising ed	ge of PWMxH	will trigger Le	ading-Edge Bla			
<ul> <li>1 = Rising edge of PWMxL will trigger Leading-Edge Blanking counter</li> <li>0 = Leading-Edge Blanking ignores rising edge of PWMxL</li> <li>pLF: PWMxL Falling Edge Trigger Enable bit</li> <li>1 = Falling edge of PWMxL will trigger Leading-Edge Blanking counter</li> <li>0 = Leading-Edge Blanking ignores falling edge of PWMxL</li> <li>bit 11</li> <li>FLTLEBEN: Fault Input Leading-Edge Blanking Enable bit</li> <li>1 = Leading-Edge Blanking is applied to selected Fault input</li> <li>0 = Leading-Edge Blanking is not applied to selected Fault input</li> <li>0 = Leading-Edge Blanking is not applied to selected Fault input</li> <li>0 = Leading-Edge Blanking is not applied to selected current-limit input</li> <li>0 = Leading-Edge Blanking is not applied to selected current-limit input</li> <li>0 = Leading-Edge Blanking is not applied to selected current-limit input</li> <li>0 = Leading-Edge Blanking is not applied to selected current-limit input</li> <li>0 = Leading-Edge Blanking is not applied to selected current-limit input</li> <li>0 = Leading-Edge Blanking is not applied to selected current-limit input</li> <li>0 = Leading-Edge Blanking is not applied to selected current-limit input</li> <li>0 = Leading-Edge Blanking is not applied to selected current-limit input</li> <li>0 = Leading-Edge Blanking is not applied to selected current-limit input</li> <li>0 = Leading-Edge Blanking is not applied to selected current-limit input</li> <li>0 = Leading-Edge Blanking is not applied to selected current-limit input</li> <li>0 = Leading-Edge Blanking is not applied to selected current-limit input</li> <li>0 = No blanking when selected Blanking Signal Low Enable bit<sup>(1)</sup></li> <li>1 = State blanking (of current-limit and/or Fault input signals) when selected blanking signal is low</li> <li>0 = No blanking when PWMxH dutput is high</li> <li>0 = No blanking when PWMxH Low Enable bit</li> <li>1 = State blanking (of</li></ul>	bit 14	1 = Falling ed	lge of PWMxH	will trigger Le	eading-Edge Bla	0		
bit 12       PLF: PWMxL Falling Edge Trigger Enable bit         1 = Falling edge of PWMxL will trigger Leading-Edge Blanking counter         0 = Leading-Edge Blanking ignores falling edge of PWMxL         bit 11       FLTLEBEN: Fault Input Leading-Edge Blanking Enable bit         1 = Leading-Edge Blanking is not applied to selected Fault input         0 = Leading-Edge Blanking is not applied to selected Fault input         0 = Leading-Edge Blanking is applied to selected Fault input         0 = Leading-Edge Blanking is applied to selected current-limit input         0 = Leading-Edge Blanking is not applied to selected current-limit input         0 = Leading-Edge Blanking is not applied to selected current-limit input         0 = Leading-Edge Blanking is ont applied to selected current-limit input         0 = Leading-Edge Blanking is ont applied to selected current-limit input         0 = Leading-Edge Blanking is ont applied to selected current-limit input         0 = Leading-Edge Blanking is ont applied to selected current-limit input         0 = Leading-Edge Blanking is ont applied to selected current-limit input         0 = Leading-Edge Blanking is ont applied to selected current-limit input         0 = Leading-Edge Blanking is ont applied to selected current-limit input         0 = No blanking when selected Blanking signal Low Enable bit         1 = State blanking (of current-limit and/or Fault input signals) when selected blanking signal is low         0 = No blanking when P	bit 13	1 = Rising ed	ge of PWMxL	will trigger Le	ading-Edge Bla			
<ul> <li>1 = Leading-Edge Blanking is applied to selected Fault input</li> <li>0 = Leading-Edge Blanking is not applied to selected Fault input</li> <li>0 = Leading-Edge Blanking is not applied to selected Fault input</li> <li>1 = Leading-Edge Blanking is applied to selected current-limit input</li> <li>0 = Leading-Edge Blanking is not applied to selected current-limit input</li> <li>0 = Leading-Edge Blanking is not applied to selected current-limit input</li> <li>0 = Leading-Edge Blanking is not applied to selected current-limit input</li> <li>0 = Leading-Edge Blanking is not applied to selected current-limit input</li> <li>0 = Leading-Edge Blanking is not applied to selected current-limit input</li> <li>0 = Leading-Edge Blanking is not applied to selected current-limit input</li> <li>0 = Leading-Edge Blanking is not applied to selected current-limit input</li> <li>0 = Leading-Edge Blanking is not applied to selected current-limit input</li> <li>0 = Leading-Edge Blanking is not applied to selected current-limit input</li> <li>0 = No blanking (of current-limit and/or Fault input signals) when selected blanking signal is low</li> <li>0 = No blanking when selected blanking signal is low</li> <li>0 = No blanking (of current-limit and/or Fault input signals) when PWMxH output is high</li> <li>0 = No blanking (of current-limit and/or Fault input signals) when PWMxH output is low</li> <li>0 = No blanking when PWMxH output is low</li> <li>0 = No blanking (of current-limit and/or Fault input signals) when PWMxH output is low</li> <li>0 = No blanking when PWMxH output is low</li> <li>0 = No blanking (of current-limit and/or Fault input signals) when PWMxL output is low</li> <li>0 = No blanking when PWMxL output is low</li> <li>0 = No blanking when PWMxL output is high</li> <li>0 = No blanking when PWMxL output is high</li> <li>0 = No blanking when PWMxL output is high</li> <li>0 = No blanking when PWMxL output is high</li></ul>	bit 12	1 = Falling ed	lge of PWMxL	will trigger Le	ading-Edge Bla			
<ul> <li>1 = Leading-Edge Blanking is applied to selected current-limit input</li> <li>0 = Leading-Edge Blanking is not applied to selected current-limit input</li> <li>bit 9-6</li> <li>Unimplemented: Read as '0'</li> <li>bit 5</li> <li>BCH: Blanking in Selected Blanking Signal High Enable bit<sup>(1)</sup></li> <li>1 = State blanking (of current-limit and/or Fault input signals) when selected blanking signal is hig</li> <li>0 = No blanking when selected blanking Signal Low Enable bit<sup>(1)</sup></li> <li>1 = State blanking (of current-limit and/or Fault input signals) when selected blanking signal is hig</li> <li>bit 4</li> <li>BCL: Blanking in Selected Blanking Signal Low Enable bit<sup>(1)</sup></li> <li>1 = State blanking (of current-limit and/or Fault input signals) when selected blanking signal is low</li> <li>0 = No blanking when selected blanking signal is low</li> <li>0 = No blanking (of current-limit and/or Fault input signals) when PWMxH output is high</li> <li>0 = No blanking (of current-limit and/or Fault input signals) when PWMxH output is high</li> <li>0 = No blanking in PWMxH Low Enable bit</li> <li>1 = State blanking (of current-limit and/or Fault input signals) when PWMxH output is low</li> <li>0 = No blanking when PWMxH output is low</li> <li>bit 1</li> <li>BPLH: Blanking in PWMxH Low Enable bit</li> <li>1 = State blanking (of current-limit and/or Fault input signals) when PWMxL output is low</li> <li>0 = No blanking when PWMxL output is low</li> <li>bit 1</li> <li>BPLH: Blanking in PWMxL Ligh Enable bit</li> <li>1 = State blanking (of current-limit and/or Fault input signals) when PWMxL output is high</li> <li>0 = No blanking when PWMxL output is high</li> <li>0 = No blanking when PWMxL output is high</li> <li>0 = No blanking in PWMxL Low Enable bit</li> <li>1 = State blanking in PWMxL Low Enable bit</li> <li>1 = State blanking in PWMxL output is high</li> </ul>	bit 11	1 = Leading-E	Edge Blanking	is applied to	selected Fault in	nput		
bit 5       BCH: Blanking in Selected Blanking Signal High Enable bit <sup>(1)</sup> 1 = State blanking (of current-limit and/or Fault input signals) when selected blanking signal is high         bit 4       BCL: Blanking in Selected Blanking Signal Low Enable bit <sup>(1)</sup> 1 = State blanking (of current-limit and/or Fault input signals) when selected blanking signal is low         bit 4       BCL: Blanking in Selected Blanking Signal Low Enable bit <sup>(1)</sup> 1 = State blanking (of current-limit and/or Fault input signals) when selected blanking signal is low         bit 3       BPHH: Blanking in PWMxH High Enable bit         1 = State blanking (of current-limit and/or Fault input signals) when PWMxH output is high         0 = No blanking when PWMxH output is high         bit 2       BPHL: Blanking in PWMxH Low Enable bit         1 = State blanking (of current-limit and/or Fault input signals) when PWMxH output is low         0 = No blanking when PWMxH output is low         bit 1       State blanking in PWMxH Low Enable bit         1 = State blanking (of current-limit and/or Fault input signals) when PWMxH output is low         0 = No blanking when PWMxL output is low         bit 1       BPLH: Blanking in PWMxL High Enable bit         1 = State blanking (of current-limit and/or Fault input signals) when PWMxL output is high         0 = No blanking when PWMxL output is high         bit 0       BPLL: Blanking in PWMxL Low Enable bit	bit 10	1 = Leading-E	Edge Blanking	is applied to	selected current	t-limit input		
<ul> <li>1 = State blanking (of current-limit and/or Fault input signals) when selected blanking signal is hig</li> <li>0 = No blanking when selected blanking signal Low Enable bit<sup>(1)</sup></li> <li>1 = State blanking (of current-limit and/or Fault input signals) when selected blanking signal is low</li> <li>0 = No blanking when selected blanking signal is low</li> <li>0 = No blanking in PWMxH High Enable bit</li> <li>1 = State blanking (of current-limit and/or Fault input signals) when PWMxH output is high</li> <li>0 = No blanking when PWMxH output is high</li> <li>0 = No blanking in PWMxH High Enable bit</li> <li>1 = State blanking (of current-limit and/or Fault input signals) when PWMxH output is high</li> <li>0 = No blanking in PWMxH Low Enable bit</li> <li>1 = State blanking (of current-limit and/or Fault input signals) when PWMxH output is low</li> <li>0 = No blanking when PWMxH output is low</li> <li>0 = No blanking in PWMxH Low Enable bit</li> <li>1 = State blanking (of current-limit and/or Fault input signals) when PWMxH output is low</li> <li>0 = No blanking when PWMxH output is low</li> <li>bit 1 BPLH: Blanking in PWMxL High Enable bit</li> <li>1 = State blanking (of current-limit and/or Fault input signals) when PWMxL output is high</li> <li>0 = No blanking when PWMxL output is low</li> </ul>	bit 9-6	Unimplemen	ted: Read as '	0'				
<ul> <li>1 = State blanking (of current-limit and/or Fault input signals) when selected blanking signal is low</li> <li>0 = No blanking when selected blanking signal is low</li> <li>BPHH: Blanking in PWMxH High Enable bit</li> <li>1 = State blanking (of current-limit and/or Fault input signals) when PWMxH output is high</li> <li>0 = No blanking when PWMxH output is high</li> <li>bit 2</li> <li>BPHL: Blanking in PWMxH Low Enable bit</li> <li>1 = State blanking (of current-limit and/or Fault input signals) when PWMxH output is low</li> <li>0 = No blanking when PWMxH output is low</li> <li>0 = No blanking when PWMxH output is low</li> <li>bit 1</li> <li>BPLH: Blanking in PWMxL High Enable bit</li> <li>1 = State blanking (of current-limit and/or Fault input signals) when PWMxL output is high</li> <li>bit 1</li> <li>BPLH: Blanking in PWMxL High Enable bit</li> <li>1 = State blanking (of current-limit and/or Fault input signals) when PWMxL output is high</li> <li>bit 0</li> <li>BPLL: Blanking in PWMxL Low Enable bit</li> <li>1 = State blanking when PWMxL output is high</li> <li>bit 0</li> <li>BPLL: Blanking in PWMxL Low Enable bit</li> <li>1 = State blanking (of current-limit and/or Fault input signals) when PWMxL output is high</li> </ul>	bit 5	1 = State blar	nking (of currer	nt-limit and/or	Fault input sigr		cted blanking s	ignal is high
<ul> <li>1 = State blanking (of current-limit and/or Fault input signals) when PWMxH output is high</li> <li>0 = No blanking when PWMxH output is high</li> <li>bit 2</li> <li>BPHL: Blanking in PWMxH Low Enable bit</li> <li>1 = State blanking (of current-limit and/or Fault input signals) when PWMxH output is low</li> <li>0 = No blanking when PWMxH output is low</li> <li>bit 1</li> <li>BPLH: Blanking in PWMxL High Enable bit</li> <li>1 = State blanking (of current-limit and/or Fault input signals) when PWMxL output is high</li> <li>bit 1</li> <li>BPLH: Blanking (of current-limit and/or Fault input signals) when PWMxL output is high</li> <li>0 = No blanking when PWMxL output is high</li> <li>bit 0</li> <li>BPLL: Blanking in PWMxL Low Enable bit</li> <li>1 = State blanking (of current-limit and/or Fault input signals) when PWMxL output is high</li> </ul>	bit 4	1 = State blar	nking (of currer	nt-limit and/or	Fault input sigr		cted blanking s	ignal is low
1 = State blanking (of current-limit and/or Fault input signals) when PWMxH output is low         0 = No blanking when PWMxH output is low         bit 1       BPLH: Blanking in PWMxL High Enable bit         1 = State blanking (of current-limit and/or Fault input signals) when PWMxL output is high         0 = No blanking when PWMxL output is high         0 = No blanking when PWMxL output is high         bit 0       BPLL: Blanking in PWMxL Low Enable bit         1 = State blanking (of current-limit and/or Fault input signals) when PWMxL output is low	bit 3	<b>BPHH:</b> Blanking in PWMxH High Enable bit 1 = State blanking (of current-limit and/or Fault input signals) when PWMxH output is high						
bit 1       BPLH: Blanking in PWMxL High Enable bit         1 = State blanking (of current-limit and/or Fault input signals) when PWMxL output is high         0 = No blanking when PWMxL output is high         bit 0       BPLL: Blanking in PWMxL Low Enable bit         1 = State blanking (of current-limit and/or Fault input signals) when PWMxL output is low	bit 2	<b>BPHL:</b> Blanking in PWMxH Low Enable bit 1 = State blanking (of current-limit and/or Fault input signals) when PWMxH output is low						
bit 0 <b>BPLL:</b> Blanking in PWMxL Low Enable bit 1 = State blanking (of current-limit and/or Fault input signals) when PWMxL output is low	bit 1	<b>BPLH:</b> Blanki 1 = State blar	ing in PWMxL hking (of currer	High Enable I nt-limit and/or	bit Fault input sigr	nals) when PWN	/IxL output is hi	gh
$\sim$ i	bit 0	<b>BPLL:</b> Blanking in PWMxL Low Enable bit 1 = State blanking (of current-limit and/or Fault input signals) when PWMxL output is low						

## REGISTER 16-16: LEBCONX: PWMx LEADING-EDGE BLANKING CONTROL REGISTER

Note 1: The blanking signal is selected via the BLANKSELx bits in the AUXCONx register.

### 17.2 QEI Control Registers

	REGISTER 17-1:	QEI1CON: QEI1 CONTROL REGISTER
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U-0       R/W-0       R/W-0       R/W-0       R/W-0       R/W-0       R/W-0       R/W-0       R/W-0         —       INTDIV2 <sup>(3)</sup> INTDIV1 <sup>(3)</sup> INTDIV0 <sup>(3)</sup> CNTPOL       GATEN       CCM1       CCM0         bit 7									
bit 15       bit 2         U-0       R/W-0       R/W-0       R/W-0       R/W-0       R/W-0       R/W-0       R/W-0         -       INTDIV2 <sup>(3)</sup> INTDIV1 <sup>(3)</sup> INTDIV0 <sup>(3)</sup> CNTPOL       GATEN       CCM1       CCM0         -       INTDIV2 <sup>(3)</sup> INTDIV1 <sup>(3)</sup> INTDIV0 <sup>(3)</sup> CNTPOL       GATEN       CCM1       CCM0         -       INTDIV2 <sup>(3)</sup> INTDIV1 <sup>(3)</sup> INTDIV0 <sup>(3)</sup> CNTPOL       GATEN       CCM1       CCM0         bit 7       -       intdividue       W= Writable bit       U = Unimplemented bit, read as '0'       bit 15       GEIEN: Quadrature Encoder Interface Module Counter Enable bit       1 = Module counters are enabled       0 = Module counters are enabled       0 = Module counters are disabled, but SFRs can be read or written to         bit 13       GEISDL: QEI Stop in Idle Mode bit       1 = Discontinues module operation when device enters Idle mode       0 = Continues module operation in Idle mode         bit 12-10       PIMOD-2:0>: Position Counter Initialization Mode Select bits <sup>(1)</sup> 111 = Reserved       100 = Modulo Count mode for position counter         100 = Next index event after home event initializes position counter with contents of QEI1IC register       100 = Next index input event initializes position counter with contents of QEI1IC register       100 = Index input event dees not affect position coun	R/W-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	
U-0       R/W-0       R/W-0       R/W-0       R/W-0       R/W-0       R/W-0       R/W-0       R/W-0         -       INTDIV2 <sup>(3)</sup> INTDIV1 <sup>(3)</sup> INTDIV0 <sup>(3)</sup> CNTPOL       GATEN       CCM1       CCM0         bit 7       bit 0       Dit 7       Dit 7       Dit 7       Dit 7       Dit 7         Legend:       R = Readable bit       W = Writable bit       U = Unimplemented bit, read as '0'       Dit 7         en value at POR       '1' = Bit is set       '0' = Bit is cleared       x = Bit is unknown         bit 15       QEIEN:       Quadrature Encoder Interface Module Counter Enable bit       1 = Module counters are enabled       0         0 = Module counters are enabled       0 = Module counters are disabled, but SFRs can be read or written to       Dit 13       QEISDL: QEI Stop in Idle Mode bit         1 = Discontinues module operation in Idle mode       0 = Continues module operation in Idle mode       Di Continues module operation on In Idle mode         Dit 12-10       PIMOD<2:0>: Position Counter Initialization Mode Select bits <sup>(1)</sup> 111 = Reserved         100 = Modulo Count mode for position counter       101 = Resets the position counter       101 = Resets the position counter with contents of QEI1IC register         101 = Resets the position counter when the position counter with contents of QEI1IC register       000 = Index input e	QEIEN	_	QEISIDL	PIMOD2 <sup>(1)</sup>	PIMOD1 <sup>(1)</sup>	PIMOD0 <sup>(1)</sup>	IMV1 <sup>(2)</sup>	IMV0 <sup>(2)</sup>	
-       INTDIV2 <sup>(3)</sup> INTDIV0 <sup>(3)</sup> CNTPOL       GATEN       CCM1       CCM0         bit 7       bit 7       bit 0         Legend:       R = Readable bit       W = Writable bit       U = Unimplemented bit, read as '0'       bit 0         -n = Value at POR       '1' = Bit is set       '0' = Bit is cleared       x = Bit is unknown         bit 15       QEIEN: Quadrature Encoder Interface Module Counter Enable bit       1 = Module counters are disabled, but SFRs can be read or written to         bit 14       Unimplemented: Read as '0'       Bit is cleared       x = Bit is unknown         bit 13       QEISDL: QEI Stop in Idle Mode bit       1 = Discontinues module operation when device enters Idle mode       0 = Continues module operation in Idle mode         0 = Continues module operation unter Initialization Mode Select bits <sup>(1)</sup> 111 = Reserved       110 = Modulo Count mode for position counter         10 = Resets the position counter when the position counter with contents of QEI1IC register       100 = Second index event after home event initializes position counter with contents of QEI1IC register         10 = Next index input event frees the position counter       110 = Resets the position counter         11 = Reserved       11 = First index event after home event initializes position counter with contents of QEI1IC register         10 = Next index input event free home event initializes position counter with contents of QEI1IC register	bit 15	bit							
-       INTDIV2 <sup>(3)</sup> INTDIV0 <sup>(3)</sup> CNTPOL       GATEN       CCM1       CCM0         bit 7       bit 7       bit 0         Legend:       R = Readable bit       W = Writable bit       U = Unimplemented bit, read as '0'       bit 0         -n = Value at POR       '1' = Bit is set       '0' = Bit is cleared       x = Bit is unknown         bit 15       QEIEN: Quadrature Encoder Interface Module Counter Enable bit       1 = Module counters are disabled, but SFRs can be read or written to         bit 14       Unimplemented: Read as '0'       Bit is cleared       x = Bit is unknown         bit 13       QEISDL: QEI Stop in Idle Mode bit       1 = Discontinues module operation when device enters Idle mode       0 = Continues module operation in Idle mode         0 = Continues module operation unter Initialization Mode Select bits <sup>(1)</sup> 111 = Reserved       110 = Modulo Count mode for position counter         10 = Resets the position counter when the position counter with contents of QEI1IC register       100 = Second index event after home event initializes position counter with contents of QEI1IC register         10 = Next index input event frees the position counter       110 = Resets the position counter         11 = Reserved       11 = First index event after home event initializes position counter with contents of QEI1IC register         10 = Next index input event free home event initializes position counter with contents of QEI1IC register									
bit 7       bit 0         Legend:       W = Writable bit       U = Unimplemented bit, read as '0'         n = Value at POR       '1' = Bit is set       '0' = Bit is cleared       x = Bit is unknown         bit 15       QEIEN: Quadrature Encoder Interface Module Counter Enable bit       1 = Module counters are enabled       0 = Module counters are enabled         0 = Module counters are disabled, but SFRs can be read or written to       0 = Module counters are disabled, but SFRs can be read or written to         bit 14       Unimplemented: Read as '0'       0 = Continues module operation when device enters Idle mode         0 = Continues module operation when device enters Idle mode       0 = Continues module operation in Idle mode         bit 12-10       PIMOD-2:0-: Position Counter Initialization Mode Select bits <sup>(1)</sup> 111 = Reserved       110 = Resets the position counter         101 = Resets the position counter when the position counter with contents of QEI1IC register         101 = Nexet input event after home event initializes position counter with contents of QEI1IC register         010 = Next index input event resets the position counter         011 = Every index input event resets the position counter         012 = Nease B match occurs when QEB = 1         0 = Phase B match occurs when QEB = 0         bit 8       IMV0: Index Match Value for Phase A bit <sup>(2)</sup> 1 = Phase A match occurs when QEA = 1 <t< td=""><td>U-0</td><td></td><td></td><td></td><td>R/W-0</td><td>R/W-0</td><td>R/W-0</td><td>R/W-0</td></t<>	U-0				R/W-0	R/W-0	R/W-0	R/W-0	
Legend:         R = Readable bit       W = Writable bit       U = Unimplemented bit, read as '0'         In = Value at POR       '1' = Bit is set       '0' = Bit is cleared       x = Bit is unknown         bit 15       QEIEN: Quadrature Encoder Interface Module Counter Enable bit       1 = Module counters are enabled       0         0 = Module counters are enabled       0 = Module counters are disabled, but SFRs can be read or written to       0         bit 14       Unimplemented: Read as '0'       0         bit 13       QEISIDL: QEI Stop in Idle Mode bit       1 = Discontinues module operation when device enters Idle mode         0 = Continues module operation in Idle mode       0 = Continues module operation in Idle mode         11 = Reserved       111 = Reserved         110 = Modulo Count mode for position counter       101 = Resets the position counter when the position counter equals QEI1GEC register         100 = Second index event after home event initializes position counter with contents of QEI1IC register       100 = Second index event after home event initializes position counter with contents of QEI1IC register         101 = First index vent after home event initializes position counter with contents of QEI1IC register       001 = Every index input event resets the position counter         010 = Next index input event does not affect position counter       001 = Every index input event after home event initializes position counter with contents of QEI1IC register		INTDIV2 <sup>(3)</sup>	INTDIV1 <sup>(3)</sup>	INTDIV0 <sup>(3)</sup>	CNTPOL	GATEN	CCM1		
R = Readable bit       W = Writable bit       U = Unimplemented bit, read as '0'         In = Value at POR       '1' = Bit is set       '0' = Bit is cleared       x = Bit is unknown         bit 15       QEIEN: Quadrature Encoder Interface Module Counter Enable bit       1 = Module counters are enabled       0 = Bit is cleared       x = Bit is unknown         bit 15       QEISIDL: QEI Stop in Idle Mode bit       1 = Module counters are disabled, but SFRs can be read or written to       bit 14         Unimplemented: Read as '0'       East as '0'       East as '0'       East as '0'         bit 13       QEISIDL: QEI Stop in Idle Mode bit       1 = Discontinues module operation when device enters Idle mode       0 = Continues module operation in Idle mode         bit 12-10       PIMOD<2:0>: Position Counter Initialization Mode Select bits <sup>(1)</sup> 111 = Reserved         110 = Modulo Count mode for position counter       10 = Second index event after home event initializes position counter with contents of QEI1IC register         100 = Second index event after home event initializes position counter with contents of QEI1IC register       010 = Next index input event initializes the position counter         101 = Reserved       III = First index event after home event initializes position counter with contents of QEI1IC register       010 = Next index input event initializes position counter with contents of QEI1IC register         102 = Mext index input event does not affect position counter       01 = Phase	bit 7							bit 0	
R = Readable bit       W = Writable bit       U = Unimplemented bit, read as '0'         In = Value at POR       '1' = Bit is set       '0' = Bit is cleared       x = Bit is unknown         bit 15       QEIEN: Quadrature Encoder Interface Module Counter Enable bit       1 = Module counters are enabled       0 = Bit is cleared       x = Bit is unknown         bit 15       QEISIDL: QEI Stop in Idle Mode bit       1 = Module counters are disabled, but SFRs can be read or written to       bit 14         Unimplemented: Read as '0'       East as '0'       East as '0'       East as '0'         bit 13       QEISIDL: QEI Stop in Idle Mode bit       1 = Discontinues module operation when device enters Idle mode       0 = Continues module operation in Idle mode         bit 12-10       PIMOD<2:0>: Position Counter Initialization Mode Select bits <sup>(1)</sup> 111 = Reserved         110 = Modulo Count mode for position counter       10 = Second index event after home event initializes position counter with contents of QEI1IC register         100 = Second index event after home event initializes position counter with contents of QEI1IC register       010 = Next index input event initializes the position counter         101 = Reserved       III = First index event after home event initializes position counter with contents of QEI1IC register       010 = Next index input event initializes position counter with contents of QEI1IC register         102 = Mext index input event does not affect position counter       01 = Phase	Logondy								
n = Value at POR       '1' = Bit is set       '0' = Bit is cleared       x = Bit is unknown         bit 15       QEIEN: Quadrature Encoder Interface Module Counter Enable bit       1 = Module counters are enabled       0 = Bit is unknown         bit 15       QEIEN: Quadrature Encoder Interface Module Counter Enable bit       1 = Module counters are enabled       0 = Bit is unknown         bit 14       Unimplemented: Read as '0'       0'       0'       Bit is cleared       0 = Continues module operation when device enters ldle mode       0 = Continues module operation in ldle mode         bit 12-10       PIMOD<2:0>: Position Counter Initialization Mode Select bits <sup>(1)</sup> 111 = Reserved         110 = Modulo Count mode for position counter       10 = Second index event after home event initializes position counter with contents of QEI11C register         100 = Second index event after home event initializes position counter with contents of QEI11C register       10 = Next index input event resets the position counter with contents of QEI11C register         101 = Every index input event resets the position counter       00 = Index input event does not affect position counter         001 = Every index input event genst bit <sup>(2)</sup> 1 = Phase B match occurs when QEB = 1         011 = Phase B match occurs when QEB = 1       0 = Phase B match occurs when QEA = 1         015 = Phase A match occurs when QEA = 1       0 = Phase A match occurs when QEA = 1         015 = Phase A match occurs when QEA =		lo hit		hit	II – Unimplor	monted bit read	ac '0'		
bit 15       QEIEN: Quadrature Encoder Interface Module Counter Enable bit         1 = Module counters are enabled       0 = Module counters are disabled, but SFRs can be read or written to         bit 14       Unimplemented: Read as '0'         bit 13       QEISIDL: QEI Stop in Idle Mode bit         1 = Discontinues module operation when device enters Idle mode       0 = Continues module operation in Idle mode         0 = Continues module operation in Idle mode       0 = Continues module operation in Idle mode         11 = Discontinues module operation in Idle mode       0 = Continues module operation in Idle mode         0 = Continues module operation when device enters Idle mode       0 = Continues module operation in Idle mode         0 = Continues module operation in Idle mode       0 = Continues module operation in Idle mode         0 = Continues module operation in Idle mode       0 = Continues module operation in Idle mode         0 = Continues module operation in Idle mode       0 = Continues module operation in Idle mode         0 = Continues module operation counter Initialization Mode Select bits <sup>(1)</sup> 111 = Reserved         110 = Modulo Count mode for position counter       100 = Second index event after home event initializes position counter with contents of QEI1IC register         011 = First index event after home event initializes position counter with contents of QEI1IC register       010 = Next index input event resets the position counter         001 = Nevery index input eve					•				
<ul> <li>1 = Module counters are enabled</li> <li>0 = Module counters are disabled, but SFRs can be read or written to</li> <li>bit 14</li> <li>Unimplemented: Read as '0'</li> <li>bit 13</li> <li>QEISIDL: QEI Stop in Idle Mode bit</li> <li>1 = Discontinues module operation when device enters Idle mode</li> <li>0 = Continues module operation in Idle mode</li> <li>0 = Continues module operation in Idle mode</li> <li>0 = Continues module operation counter Initialization Mode Select bits<sup>(1)</sup></li> <li>111 = Reserved</li> <li>110 = Modulo Count mode for position counter</li> <li>101 = Resets the position counter when the position counter equals QEI1GEC register</li> <li>100 = Second index event after home event initializes position counter with contents of QEI1IC register</li> <li>010 = Next index input event initializes the position counter with contents of QEI1IC register</li> <li>010 = Next index input event resets the position counter with contents of QEI1IC register</li> <li>011 = Every index input event resets the position counter</li> <li>000 = Index input event does not affect position counter</li> <li>000 = Index input event does not affect position counter</li> <li>000 = Index Match Value for Phase B bit<sup>(2)</sup></li> <li>1 = Phase B match occurs when QEB = 1</li> <li>0 = Phase B match occurs when QEB = 0</li> <li>bit 8</li> <li>IMV0: Index Match Value for Phase A bit<sup>(2)</sup></li> <li>1 = Phase A match occurs when QEA = 1</li> <li>0 = Phase A match occurs when QEA = 1</li> <li>0 = Phase A match occurs when QEA = 0</li> <li>bit 7</li> <li>Unimplemented: Read as '0'</li> </ul>	-n = value a	PUR	I = Bit is set		0 = Bit is cle	ared	x = Bit is unkr	IOWN	
bit 13       QEISDL: QEI Stop in Idle Mode bit         1 = Discontinues module operation when device enters Idle mode       0 = Continues module operation in Idle mode         bit 12-10       PIMOD<2:0>: Position Counter Initialization Mode Select bits <sup>(1)</sup> 111 = Reserved       110 = Modulo Count mode for position counter         100 = Modulo Count mode for position counter       101 = Resets the position counter when the position counter equals QEI1GEC register         100 = Second index event after home event initializes position counter with contents of QEI1IC register       010 = Next index input event initializes the position counter with contents of QEI1IC register         011 = First index event after home event initializes position counter with contents of QEI1IC register       010 = Next index input event initializes the position counter with contents of QEI1IC register         011 = Every index input event resets the position counter       001 = Every index input event for position counter         001 = Index input event does not affect position counter       000 = Index input event does not affect position counter         001 = Phase B match occurs when QEB = 1       0 = Phase B match occurs when QEB = 0         0it 8       IMV0: Index Match Value for Phase A bit <sup>(2)</sup> 1 = Phase A match occurs when QEA = 1       0 = Phase A match occurs when QEA = 0         0it 7       Unimplemented: Read as '0'	bit 15	1 = Module co	ounters are ena	abled					
<ul> <li>1 = Discontinues module operation when device enters Idle mode</li> <li>0 = Continues module operation in Idle mode</li> <li>bit 12-10</li> <li>PIMOD&lt;2:0&gt;: Position Counter Initialization Mode Select bits<sup>(1)</sup></li> <li>111 = Reserved</li> <li>10 = Modulo Count mode for position counter</li> <li>10 = Resets the position counter when the position counter equals QEI1GEC register</li> <li>100 = Second index event after home event initializes position counter with contents of QEI1IC register</li> <li>010 = Next index event after home event initializes position counter with contents of QEI1IC register</li> <li>010 = Next index input event resets the position counter with contents of QEI1IC register</li> <li>000 = Index input event does not affect position counter</li> <li>000 = Index input event does not affect position counter</li> <li>000 = Index input event operation when QEB = 1</li> <li>0 = Phase B match occurs when QEB = 0</li> <li>bit 8</li> <li>IMV0: Index Match Value for Phase A bit<sup>(2)</sup></li> <li>1 = Phase A match occurs when QEA = 1</li> <li>0 = Phase A match occurs when QEA = 1</li> <li>0 = Phase A match occurs when QEA = 0</li> <li>bit 7</li> <li>Unimplemented: Read as '0'</li> </ul>	bit 14	Unimplemen	ted: Read as '	0'					
<ul> <li>0 = Continues module operation in Idle mode</li> <li>bit 12-10</li> <li>PIMOD&lt;2:0&gt;: Position Counter Initialization Mode Select bits<sup>(1)</sup></li> <li>111 = Reserved</li> <li>10 = Modulo Count mode for position counter</li> <li>101 = Resets the position counter when the position counter equals QEI1GEC register</li> <li>100 = Second index event after home event initializes position counter with contents of QEI1IC register</li> <li>010 = Next index input event after home event initializes position counter with contents of QEI1IC register</li> <li>010 = Next index input event resets the position counter with contents of QEI1IC register</li> <li>001 = Every index input event resets the position counter</li> <li>000 = Index input event does not affect position counter</li> <li>000 = Index input event does not affect position counter</li> <li>000 = Index input event does not affect position counter</li> <li>000 = Index input event QEB = 1</li> <li>0 = Phase B match occurs when QEB = 1</li> <li>0 = Phase B match occurs when QEB = 0</li> <li>bit 8</li> <li>IMV0: Index Match Value for Phase A bit<sup>(2)</sup></li> <li>1 = Phase A match occurs when QEA = 1</li> <li>0 = Phase A match occurs when QEA = 1</li> <li>0 = Phase A match occurs when QEA = 0</li> <li>bit 7</li> </ul>	bit 13	QEISIDL: QE	I Stop in Idle M	lode bit					
<ul> <li>111 = Reserved</li> <li>10 = Modulo Count mode for position counter</li> <li>101 = Resets the position counter when the position counter equals QEI1GEC register</li> <li>100 = Second index event after home event initializes position counter with contents of QEI1IC register</li> <li>011 = First index event after home event initializes position counter with contents of QEI1IC register</li> <li>010 = Next index input event initializes the position counter with contents of QEI1IC register</li> <li>011 = Every index input event resets the position counter with contents of QEI1IC register</li> <li>000 = Index input event does not affect position counter</li> <li>000 = Index input event does not affect position counter</li> <li>011 = Phase B match occurs when QEB = 1</li> <li>0 = Phase B match occurs when QEB = 0</li> <li>0 = Phase B match occurs when QEB = 0</li> <li>1 = Phase A match occurs when QEA = 1</li> <li>0 = Phase A match occurs when QEA = 1</li> <li>0 = Phase A match occurs when QEA = 1</li> <li>0 = Phase A match occurs when QEA = 0</li> <li>0 = Phase A match occurs when QEA = 0</li> </ul>						dle mode			
<ul> <li>110 = Modulo Count mode for position counter</li> <li>101 = Resets the position counter when the position counter equals QEI1GEC register</li> <li>100 = Second index event after home event initializes position counter with contents of QEI1IC register</li> <li>011 = First index event after home event initializes position counter with contents of QEI1IC register</li> <li>010 = Next index input event initializes the position counter with contents of QEI1IC register</li> <li>001 = Every index input event resets the position counter</li> <li>000 = Index input event does not affect position counter</li> <li>000 = Index input event for Phase B bit<sup>(2)</sup></li> <li>1 = Phase B match occurs when QEB = 1</li> <li>0 = Phase B match occurs when QEB = 0</li> <li>bit 8</li> <li>IMV0: Index Match Value for Phase A bit<sup>(2)</sup></li> <li>1 = Phase A match occurs when QEA = 1</li> <li>0 = Phase A match occurs when QEA = 1</li> <li>0 = Phase A match occurs when QEA = 0</li> <li>bit 7</li> <li>Unimplemented: Read as '0'</li> </ul>	bit 12-10	PIMOD<2:0>	: Position Cour	nter Initializatio	on Mode Selec	t bits <sup>(1)</sup>			
1 = Phase B match occurs when QEB = 1         0 = Phase B match occurs when QEB = 0         bit 8       IMV0: Index Match Value for Phase A bit <sup>(2)</sup> 1 = Phase A match occurs when QEA = 1         0 = Phase A match occurs when QEA = 0         bit 7       Unimplemented: Read as '0'		110 = Module 101 = Resets 100 = Second 011 = First in 010 = Next in 001 = Every i	b Count mode f the position co d index event a dex event after idex input even index input even	bunter when the fter home event home event in t initializes the put resets the p	e position cou at initializes posi nitializes positi position coun position counte	sition counter wit on counter with ter with contents	h contents of C contents of QE	EI1IC register	
0 = Phase B match occurs when QEB = 0         bit 8         IMV0: Index Match Value for Phase A bit <sup>(2)</sup> 1 = Phase A match occurs when QEA = 1         0 = Phase A match occurs when QEA = 0         bit 7         Unimplemented: Read as '0'	bit 9	IMV1: Index I	Match Value for	<sup>-</sup> Phase B bit <sup>(2</sup>	)				
bit 8       IMV0: Index Match Value for Phase A bit <sup>(2)</sup> 1 = Phase A match occurs when QEA = 1         0 = Phase A match occurs when QEA = 0         bit 7       Unimplemented: Read as '0'		1 = Phase B match occurs when QEB = 1							
1 = Phase A match occurs when QEA = 10 = Phase A match occurs when QEA = 0bit 7Unimplemented: Read as '0'					<b>N</b>				
0 = Phase A match occurs when QEA = 0         bit 7         Unimplemented: Read as '0'	bit 8				1				
bit 7 Unimplemented: Read as '0'									
	bit 7								
		•			inters onerate	as timers and th		> hits are	

**Note 1:** When CCM<1:0> = 10 or 11, all of the QEI counters operate as timers and the PIMOD<2:0> bits are ignored.

2: When CCM<1:0> = 00, and QEA and QEB values match the Index Match Value (IMV), the POSCNTH and POSCNTL registers are reset. QEA/QEB signals used for the index match have swap and polarity values applied, as determined by the SWPAB and QEAPOL/QEBPOL bits.

3: The selected clock rate should be at least twice the expected maximum quadrature count rate.

### REGISTER 17-13: QEI1LECH: QEI1 LESS THAN OR EQUAL COMPARE HIGH WORD REGISTER

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
			QEILE	C<31:24>			
bit 15							bit 8
R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
			QEILE	C<23:16>			
bit 7							bit 0
Legend:							
R = Readable	bit	W = Writable b	bit	U = Unimplem	ented bit, rea	d as '0'	
-n = Value at POR '1' = Bit is set '0' = Bit is cleared x = Bit is unknow			nown				

bit 15-0 QEILEC<31:16>: High Word Used to Form 32-Bit Less Than or Equal Compare Register (QEI1LEC) bits

## REGISTER 17-14: QEI1LECL: QEI1 LESS THAN OR EQUAL COMPARE LOW WORD REGISTER

R = Readable t		W = Writable '1' = Bit is set		U = Unimplen '0' = Bit is cle		ad as '0' x = Bit is unkr	
Legend:							
bit 7							bit
			QEIL	EC<7:0>			
R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
bit 15							bit
			QEILE	EC<15:8>			
R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0

bit 15-0 QEILEC<15:0>: Low Word Used to Form 32-Bit Less Than or Equal Compare Register (QEI1LEC) bits

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
CSS15	CSS14	CSS13	CSS12	CSS11	CSS10	CSS9	CSS8
bit 15				·	•	·	bit 8
R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
CSS7	CSS6	CSS5	CSS4	CSS3	CSS2	CSS1	CSS0
bit 7	-				•		bit (
Legend:							
R = Readable	bit	W = Writable	bit	U = Unimple	mented bit, rea	d as '0'	
-n = Value at POR '1' = Bit is set '0' = Bit is cle		eared	x = Bit is unk	nown			

# REGISTER 23-8: AD1CSSL: ADC1 INPUT SCAN SELECT REGISTER LOW<sup>(1,2)</sup>

bit 15-0 CSS<15:0>: ADC1 Input Scan Selection bits

1 = Selects ANx for input scan

0 = Skips ANx for input scan

**Note 1:** On devices with less than 16 analog inputs, all AD1CSSL bits can be selected by the user. However, inputs selected for scan, without a corresponding input on the device, convert VREFL.

**2:** CSSx = ANx, where x = 0-15.

U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	_	—		—	_
bit 15							bit
U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	CFSEL2	CFSEL1	CFSEL0	CFLTREN	CFDIV2	CFDIV1	CFDIV0
bit 7							bit
Legend:							
R = Readab	le bit	W = Writable	bit	U = Unimpler	mented bit, read	as '0'	
-n = Value a		'1' = Bit is set		'0' = Bit is cle		x = Bit is unk	nown
							-
bit 15-7	Unimplemen	ted: Read as	ʻ0'				
oit 6-4	CFSEL<2:0>	: Comparator	Filter Input Clo	ock Select bits			
	111 = T5CLK		·				
	110 = T4CLK						
	101 = T3CLK	( <sup>(1)</sup>					
	100 = T2CLK	<mark>(</mark> (2)					
	011 = Reserv						
	010 = SYNC	01 <sup>(3)</sup>					
	001 = Fosc <sup>(4</sup>	1)					
	000 = FP <sup>(4)</sup>						
bit 3		comparator Filt	er Enable bit				
	1 = Digital filt						
	•	er is disabled					
bit 2-0	CFDIV<2:0>:	: Comparator F	ilter Clock Div	vide Select bits			
	111 = Clock	Divide 1:128					
	110 = Clock	Divide 1:64					
	101 = Clock	Divide 1:32					
	100 = Clock	Divide 1:16					
	011 = Clock						
	010 = Clock						
	001 = Clock						
	000 = Clock	Divide 1:1					
Note 1: S	See the Type C Ti	mer Block Diag	gram (Figure 1	3-2).			
	See the Type B Ti						
•							

## REGISTER 25-6: CMxFLTR: COMPARATOR x FILTER CONTROL REGISTER

- 3: See the High-Speed PWMx Module Register Interconnection Diagram (Figure 16-2).
  - 4: See the Oscillator System Diagram (Figure 9-1).

Bit Field	Description
GCP	General Segment Code-Protect bit 1 = User program memory is not code-protected 0 = Code protection is enabled for the entire program memory space
GWRP	General Segment Write-Protect bit 1 = User program memory is not write-protected 0 = User program memory is write-protected
IESO	<ul> <li>Two-Speed Oscillator Start-up Enable bit</li> <li>1 = Start up device with FRC, then automatically switch to the user-selected oscillator source when ready</li> <li>0 = Start up device with user-selected oscillator source</li> </ul>
PWMLOCK <sup>(1)</sup>	PWM Lock Enable bit 1 = Certain PWM registers may only be written after a key sequence 0 = PWM registers may be written without a key sequence
FNOSC<2:0>	Oscillator Selection bits 111 = Fast RC Oscillator with Divide-by-N (FRCDIVN) 110 = Fast RC Oscillator with Divide-by-16 (FRCDIV16) 101 = Low-Power RC Oscillator (LPRC) 100 = Reserved; do not use 011 = Primary Oscillator with PLL module (XT + PLL, HS + PLL, EC + PLL) 010 = Primary Oscillator (XT, HS, EC) 001 = Fast RC Oscillator with Divide-by-N with PLL module (FRCPLL) 000 = Fast RC Oscillator (FRC)
FCKSM<1:0>	Clock Switching Mode bits 1x = Clock switching is disabled, Fail-Safe Clock Monitor is disabled 01 = Clock switching is enabled, Fail-Safe Clock Monitor is disabled 00 = Clock switching is enabled, Fail-Safe Clock Monitor is enabled
IOL1WAY	Peripheral Pin Select Configuration bit 1 = Allow only one reconfiguration 0 = Allow multiple reconfigurations
OSCIOFNC	OSC2 Pin Function bit (except in XT and HS modes) 1 = OSC2 is the clock output 0 = OSC2 is a general purpose digital I/O pin
POSCMD<1:0>	Primary Oscillator Mode Select bits 11 = Primary Oscillator is disabled 10 = HS Crystal Oscillator mode 01 = XT Crystal Oscillator mode 00 = EC (External Clock) mode
FWDTEN	<ul> <li>Watchdog Timer Enable bit</li> <li>1 = Watchdog Timer is always enabled (LPRC oscillator cannot be disabled. Clearing the SWDTEN bit in the RCON register will have no effect.)</li> <li>0 = Watchdog Timer is enabled/disabled by user software (LPRC can be disabled by clearing the SWDTEN bit in the RCON register)</li> </ul>
WINDIS	Watchdog Timer Window Enable bit 1 = Watchdog Timer in Non-Window mode 0 = Watchdog Timer in Window mode
PLLKEN	PLL Lock Enable bit 1 = PLL lock is enabled 0 = PLL lock is disabled nly available on dsPIC33EPXXXMC20X/50X and PIC24EPXXXMC20X devices.

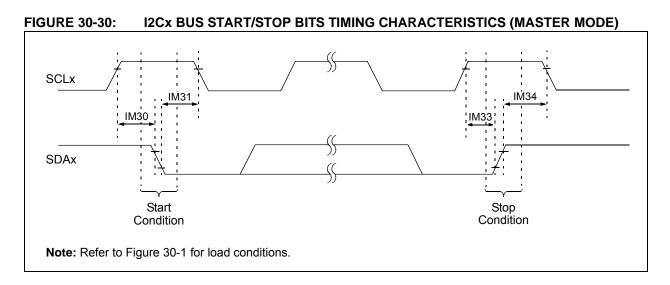
## TABLE 27-2: CONFIGURATION BITS DESCRIPTION

Note 1: This bit is only available on dsPIC33EPXXXMC20X/50X and PIC24EPXXXMC20X devices.

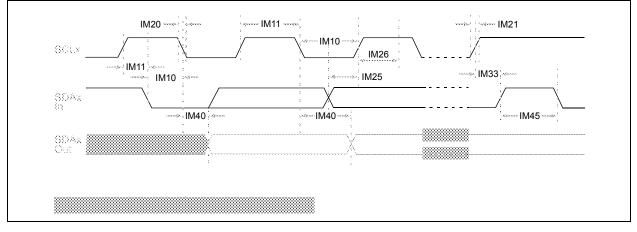
2: When JTAGEN = 1, an internal pull-up resistor is enabled on the TMS pin. Erased devices default to JTAGEN = 1. Applications requiring I/O pins in a high-impedance state (tri-state) in Reset should use pins other than TMS for this purpose.



### FIGURE 30-29: SPI1 SLAVE MODE (FULL-DUPLEX, CKE = 0, CKP = 0, SMP = 0) TIMING CHARACTERISTICS







### TABLE 30-54: OP AMP/COMPARATOR VOLTAGE REFERENCE SETTLING TIME SPECIFICATIONS

AC CHARACTERISTICS		$\begin{array}{l} \mbox{Standard Operating Conditions (see Note 2): 3.0V to 3.6V} \\ \mbox{(unless otherwise stated)} \\ \mbox{Operating temperature} & -40^\circ C \leq TA \leq +85^\circ C \mbox{ for Industrial} \\ & -40^\circ C \leq TA \leq +125^\circ C \mbox{ for Extended} \end{array}$					
Param.         Symbol         Characteristic         Min.         Typ.         Max.         Units         Cond						Conditions	
VR310	TSET	Settling Time	—	1	10	μS	(Note 1)

**Note 1:** Settling time is measured while CVRR = 1 and CVR<3:0> bits transition from '0000' to '1111'.

2: Device is functional at VBORMIN < VDD < VDDMIN, but will have degraded performance. Device functionality is tested, but not characterized. Analog modules (ADC, op amp/comparator and comparator voltage reference) may have degraded performance. Refer to Parameter BO10 in Table 30-13 for the minimum and maximum BOR values.

#### TABLE 30-55: OP AMP/COMPARATOR VOLTAGE REFERENCE SPECIFICATIONS

DC CHARACTERISTICS			$\begin{array}{l} \mbox{Standard Operating Conditions (see Note 1): 3.0V to 3.6V} \\ \mbox{(unless otherwise stated)} \\ \mbox{Operating temperature} & -40^{\circ}C \leq TA \leq +85^{\circ}C \mbox{ for Industrial} \\ & -40^{\circ}C \leq TA \leq +125^{\circ}C \mbox{ for Extended} \end{array}$						
Param No.	Symbol	Characteristics	Min.	Тур.	Max.	Units	Conditions		
VRD310	CVRES	Resolution	CVRSRC/24	_	CVRSRC/32	LSb			
VRD311	CVRAA	Absolute Accuracy <sup>(2)</sup>	—	±25	_	mV	CVRSRC = 3.3V		
VRD313	CVRSRC	Input Reference Voltage	0	_	AVDD + 0.3	V			
VRD314	CVRout	Buffer Output Resistance <sup>(2)</sup>	_	1.5k	_	Ω			

**Note 1:** Device is functional at VBORMIN < VDD < VDDMIN, but will have degraded performance. Device functionality is tested, but not characterized. Analog modules (ADC, op amp/comparator and comparator voltage reference) may have degraded performance. Refer to Parameter BO10 in Table 30-13 for the minimum and maximum BOR values.

2: Parameter is characterized but not tested in manufacturing.

AC CHARACTERISTICS			$ \begin{array}{l} \mbox{Standard Operating Conditions: 3.0V to 3.6V} \\ \mbox{(unless otherwise stated)}^{(1)} \\ \mbox{Operating temperature} & -40^{\circ}C \leq TA \leq +85^{\circ}C \mbox{ for Industrial} \\ & -40^{\circ}C \leq TA \leq +125^{\circ}C \mbox{ for Extended} \end{array} $					
Param No.	Symbol Characteristic		Min.	Тур.	Max.	Units	Conditions	
		ADC A	Accuracy	(12-Bit	Mode)			
AD20a	Nr	Resolution	12 Data Bits			bits		
AD21a INL		Integral Nonlinearity	-2.5		2.5	LSb	-40°C ≤ TA ≤ +85°C (Note 2)	
			-5.5	_	5.5	LSb	+85°C < TA ≤ +125°C (Note 2)	
AD22a DNL		Differential Nonlinearity	-1	—	1	LSb	-40°C $\leq$ TA $\leq$ +85°C (Note 2)	
			-1	—	1	LSb	+85°C < TA $\leq$ +125°C (Note 2)	
AD23a	Gerr	Gain Error <sup>(3)</sup>	-10	—	10	LSb	-40°C $\leq$ TA $\leq$ +85°C (Note 2)	
			-10	_	10	LSb	+85°C < TA $\leq$ +125°C (Note 2)	
AD24a	EOFF	Offset Error	-5	_	5	LSb	$-40^{\circ}C \leq TA \leq +85^{\circ}C \text{ (Note 2)}$	
			-5	_	5	LSb	+85°C < TA $\leq$ +125°C (Note 2)	
AD25a	—	Monotonicity	—	—	—		Guaranteed	
		Dynamic	Performa	ance (12-	Bit Mod	e)		
AD30a	THD	Total Harmonic Distortion <sup>(3)</sup>	_	75	_	dB		
AD31a	SINAD	Signal to Noise and Distortion <sup>(3)</sup>	—	68	_	dB		
AD32a	SFDR	Spurious Free Dynamic Range <sup>(3)</sup>	—	80	—	dB		
AD33a	Fnyq	Input Signal Bandwidth <sup>(3)</sup>	—	250	—	kHz		
AD34a	ENOB	Effective Number of Bits <sup>(3)</sup>	11.09	11.3	_	bits		

## TABLE 30-58: ADC MODULE SPECIFICATIONS (12-BIT MODE)

**Note 1:** Device is functional at VBORMIN < VDD < VDDMIN, but will have degraded performance. Device functionality is tested, but not characterized. Analog modules (ADC, op amp/comparator and comparator voltage reference) may have degraded performance. Refer to Parameter BO10 in Table 30-13 for the minimum and maximum BOR values.

2: For all accuracy specifications, VINL = AVSS = VREFL = 0V and AVDD = VREFH = 3.6V.

3: Parameters are characterized but not tested in manufacturing.

### TABLE 31-11: INTERNAL RC ACCURACY

AC CH	ARACTERISTICS	Standard Operating Conditions: 3.0V to 3.6V (unless otherwise stated) Operating temperature $-40^{\circ}C \le TA \le +150^{\circ}C$						
Param No.	Characteristic	Min	Тур	Max	Units	Conditions		
	LPRC @ 32.768 kHz <sup>(1,2)</sup>							
HF21	LPRC	-30	_	+30	%	$-40^{\circ}C \leq TA \leq +150^{\circ}C$	VDD = 3.0-3.6V	

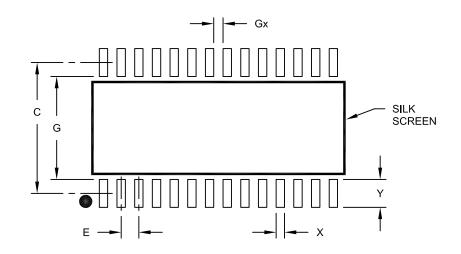
Note 1: Change of LPRC frequency as VDD changes.

2: LPRC accuracy impacts the Watchdog Timer Time-out Period (TwDT). See Section 27.5 "Watchdog Timer (WDT)" for more information.

NOTES:

28-Lead Plastic Small Outline (SO) - Wide, 7.50 mm Body [SOIC]

**Note:** For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



## RECOMMENDED LAND PATTERN

	MILLIMETERS				
Dimension	MIN	NOM	MAX		
Contact Pitch	1.27 BSC				
Contact Pad Spacing	С		9.40		
Contact Pad Width (X28)	Х			0.60	
Contact Pad Length (X28)	Y			2.00	
Distance Between Pads	Gx	0.67			
Distance Between Pads	G	7.40			

Notes:

1. Dimensioning and tolerancing per ASME Y14.5M

BSC: Basic Dimension. Theoretically exact value shown without tolerances.

Microchip Technology Drawing No. C04-2052A