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"[Embedded - Microcontrollers](#)" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

### Applications of "[Embedded - Microcontrollers](#)"

#### Details

Product Status	Obsolete
Core Processor	PIC
Core Size	16-Bit
Speed	60 MIPS
Connectivity	I <sup>2</sup> C, IrDA, LINbus, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, DMA, POR, PWM, WDT
Number of I/O	25
Program Memory Size	32KB (10.7K x 24)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	2K x 16
Voltage - Supply (Vcc/Vdd)	3V ~ 3.6V
Data Converters	A/D 8x10b/12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 150°C (TA)
Mounting Type	Surface Mount
Package / Case	36-VFTLA Exposed Pad
Supplier Device Package	36-VTLA (5x5)
Purchase URL	<a href="https://www.e-xfl.com/product-detail/microchip-technology/pic24ep32gp203-h-tl">https://www.e-xfl.com/product-detail/microchip-technology/pic24ep32gp203-h-tl</a>

**FIGURE 4-5: PROGRAM MEMORY MAP FOR dsPIC33EP512GP50X, dsPIC33EP512MC20X/50X AND PIC24EP512GP/MC20X DEVICES**

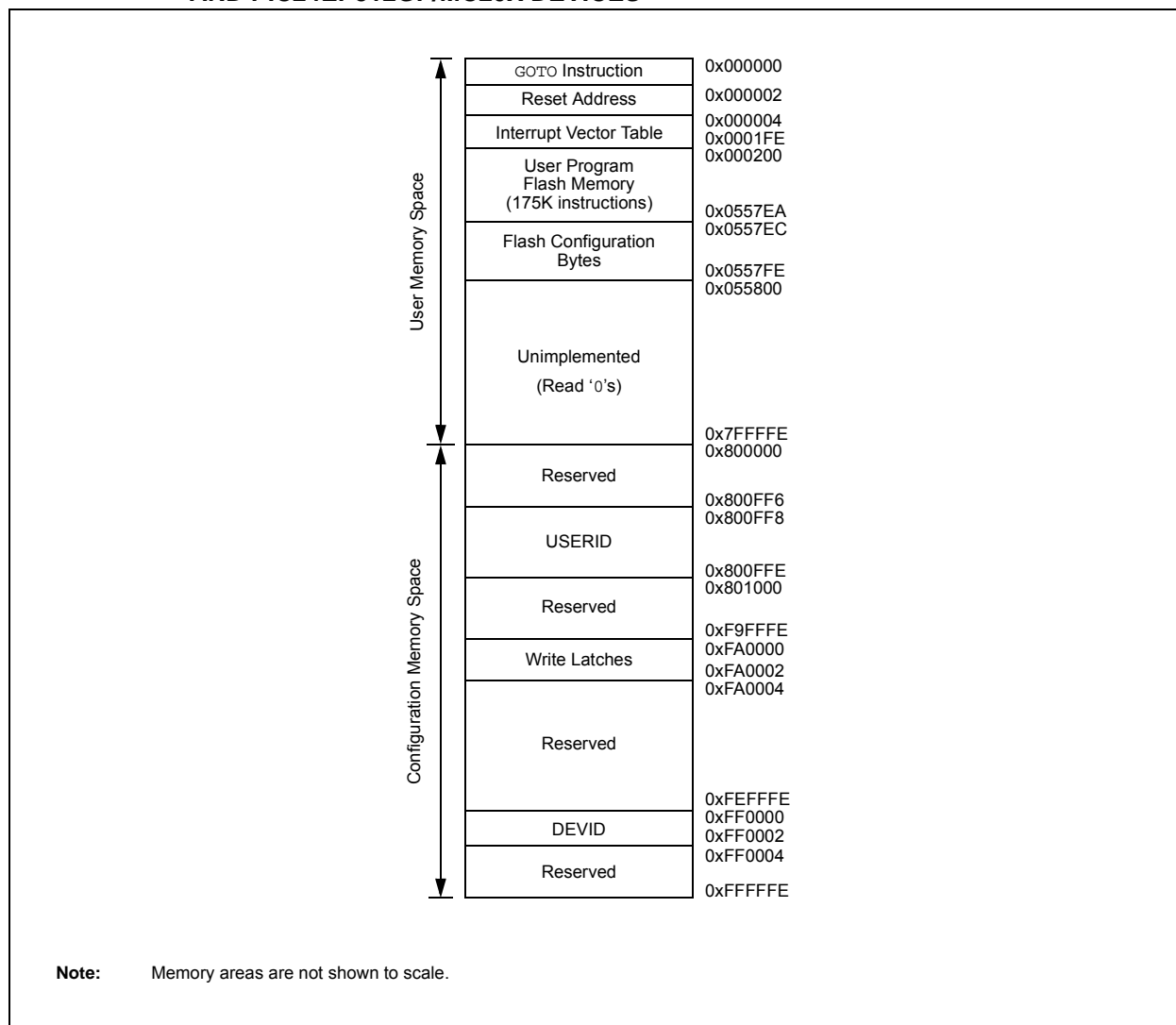
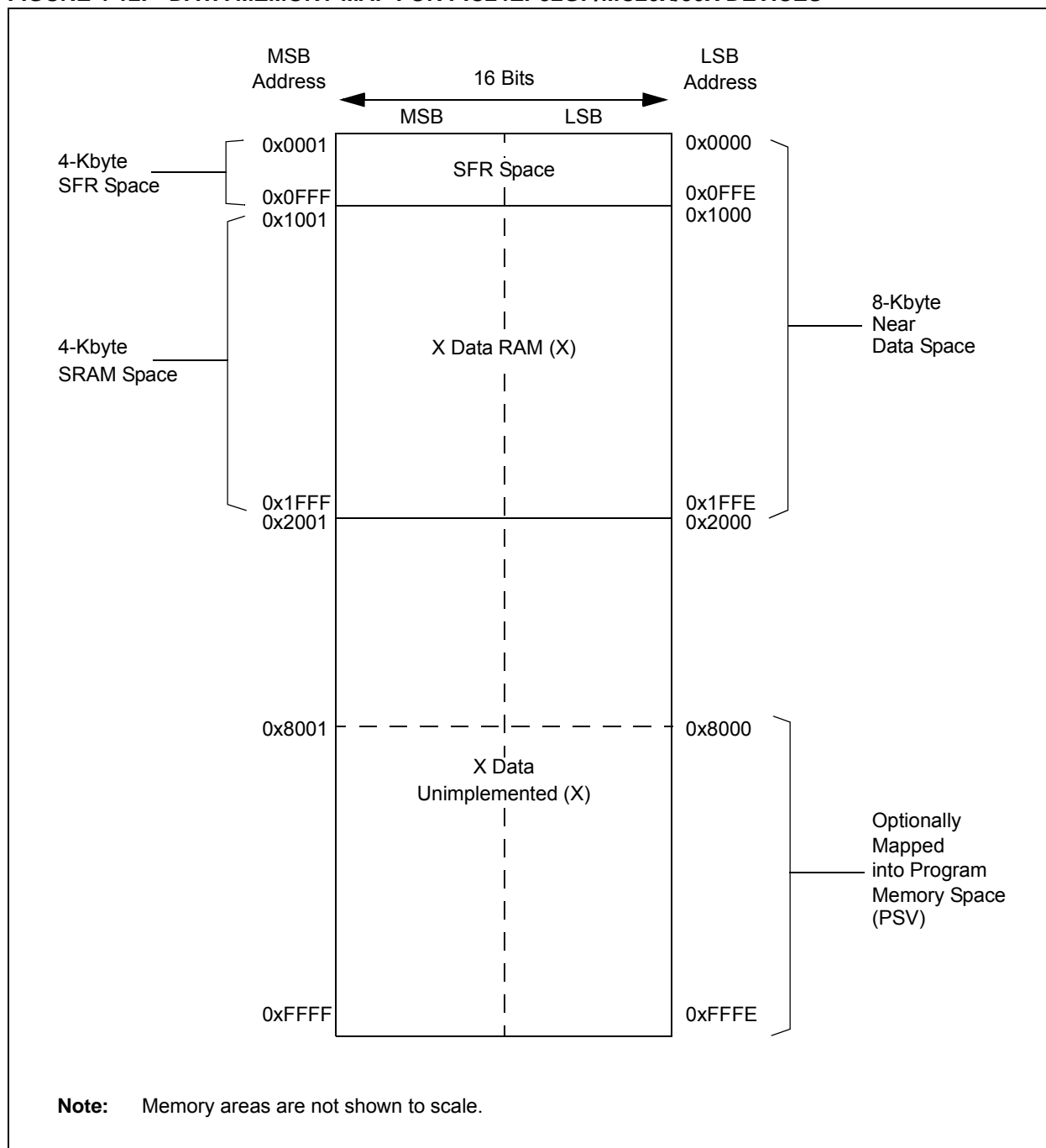


FIGURE 4-12: DATA MEMORY MAP FOR PIC24EP32GP/MC20X/50X DEVICES



**TABLE 4-5: INTERRUPT CONTROLLER REGISTER MAP FOR dsPIC33EPXXXGP50X DEVICES ONLY (CONTINUED)**

File Name	Addr.	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	All Resets
INTCON1	08C0	NSTDIS	OVAERR	OVBERR	COVAERR	COVBERR	OVATE	OVBT	COVTE	SFTACERR	DIV0ERR	DMACERR	MATHERR	ADDRERR	STKERR	OSCFAIL	—	0000
INTCON2	08C2	GIE	DISI	SWTRAP	—	—	—	—	—	—	—	—	—	—	INT2EP	INT1EP	INT0EP	8000
INTCON3	08C4	—	—	—	—	—	—	—	—	—	—	DAE	DOOVR	—	—	—	—	0000
INTCON4	08C6	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	SGHT	0000
INTTREG	08C8	—	—	—	—	ILR<3:0>				VECNUM<7:0>								0000

**Legend:** — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

**REGISTER 7-1: SR: CPU STATUS REGISTER<sup>(1)</sup>**

R/W-0	R/W-0	R/W-0	R/W-0	R/C-0	R/C-0	R-0	R/W-0
OA	OB	SA	SB	OAB	SAB	DA	DC
bit 15							bit 8

R/W-0 <sup>(3)</sup>	R/W-0 <sup>(3)</sup>	R/W-0 <sup>(3)</sup>	R-0	R/W-0	R/W-0	R/W-0	R/W-0
IPL<2:0> <sup>(2)</sup>			RA	N	OV	Z	C
bit 7							bit 0

<b>Legend:</b>	C = Clearable bit		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 7-5 **IPL<2:0>**: CPU Interrupt Priority Level Status bits<sup>(2,3)</sup>

- 111 = CPU Interrupt Priority Level is 7 (15); user interrupts are disabled
- 110 = CPU Interrupt Priority Level is 6 (14)
- 101 = CPU Interrupt Priority Level is 5 (13)
- 100 = CPU Interrupt Priority Level is 4 (12)
- 011 = CPU Interrupt Priority Level is 3 (11)
- 010 = CPU Interrupt Priority Level is 2 (10)
- 001 = CPU Interrupt Priority Level is 1 (9)
- 000 = CPU Interrupt Priority Level is 0 (8)

**Note 1:** For complete register details, see Register 3-1.

- 2:** The IPL<2:0> bits are concatenated with the IPL<3> bit (CORCON<3>) to form the CPU Interrupt Priority Level. The value in parentheses indicates the IPL, if IPL<3> = 1. User interrupts are disabled when IPL<3> = 1.
- 3:** The IPL<2:0> Status bits are read-only when the NSTDIS bit (INTCON1<15>) = 1.

**REGISTER 11-5: RPINR8: PERIPHERAL PIN SELECT INPUT REGISTER 8**

U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
—	IC4R<6:0>						
bit 15							bit 8

U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
—	IC3R<6:0>						
bit 7							bit 0

**Legend:**

R = Readable bit

W = Writable bit

U = Unimplemented bit, read as '0'

-n = Value at POR

'1' = Bit is set

'0' = Bit is cleared

x = Bit is unknown

bit 15 **Unimplemented:** Read as '0'

bit 14-8 **IC4R<6:0>:** Assign Input Capture 4 (IC4) to the Corresponding RPn Pin bits  
(see Table 11-2 for input pin selection numbers)

1111001 = Input tied to RPI121

.

.

.

0000001 = Input tied to CMP1

0000000 = Input tied to Vss

bit 7 **Unimplemented:** Read as '0'

bit 6-0 **IC3R<6:0>:** Assign Input Capture 3 (IC3) to the Corresponding RPn Pin bits  
(see Table 11-2 for input pin selection numbers)

1111001 = Input tied to RPI121

.

.

.

0000001 = Input tied to CMP1

0000000 = Input tied to Vss

**REGISTER 11-18: RPOR0: PERIPHERAL PIN SELECT OUTPUT REGISTER 0**

U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
—	—	RP35R<5:0>					
bit 15							bit 8

U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
—	—	RP20R<5:0>					
bit 7							bit 0

**Legend:**

R = Readable bit                      W = Writable bit                      U = Unimplemented bit, read as '0'  
-n = Value at POR                      '1' = Bit is set                      '0' = Bit is cleared                      x = Bit is unknown

bit 15-14            **Unimplemented:** Read as '0'  
bit 13-8            **RP35R<5:0>:** Peripheral Output Function is Assigned to RP35 Output Pin bits  
(see Table 11-3 for peripheral function numbers)  
bit 7-6            **Unimplemented:** Read as '0'  
bit 5-0            **RP20R<5:0>:** Peripheral Output Function is Assigned to RP20 Output Pin bits  
(see Table 11-3 for peripheral function numbers)

**REGISTER 11-19: RPOR1: PERIPHERAL PIN SELECT OUTPUT REGISTER 1**

U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
—	—	RP37R<5:0>					
bit 15							bit 8

U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
—	—	RP36R<5:0>					
bit 7							bit 0

**Legend:**

R = Readable bit                      W = Writable bit                      U = Unimplemented bit, read as '0'  
-n = Value at POR                      '1' = Bit is set                      '0' = Bit is cleared                      x = Bit is unknown

bit 15-14            **Unimplemented:** Read as '0'  
bit 13-8            **RP37R<5:0>:** Peripheral Output Function is Assigned to RP37 Output Pin bits  
(see Table 11-3 for peripheral function numbers)  
bit 7-6            **Unimplemented:** Read as '0'  
bit 5-0            **RP36R<5:0>:** Peripheral Output Function is Assigned to RP36 Output Pin bits  
(see Table 11-3 for peripheral function numbers)

**REGISTER 16-8: PDCx: PWMx GENERATOR DUTY CYCLE REGISTER**

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
PDCx<15:8>							
bit 15				bit 8			

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
PDCx<7:0>							
bit 7				bit 0			

**Legend:**

R = Readable bit                      W = Writable bit                      U = Unimplemented bit, read as '0'  
-n = Value at POR                      '1' = Bit is set                      '0' = Bit is cleared                      x = Bit is unknown

bit 15-0                      **PDCx<15:0>**: PWMx Generator # Duty Cycle Value bits

**REGISTER 16-9: PHASEx: PWMx PRIMARY PHASE-SHIFT REGISTER**

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
PHASEx<15:8>							
bit 15				bit 8			

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
PHASEx<7:0>							
bit 7				bit 0			

**Legend:**

R = Readable bit                      W = Writable bit                      U = Unimplemented bit, read as '0'  
-n = Value at POR                      '1' = Bit is set                      '0' = Bit is cleared                      x = Bit is unknown

bit 15-0                      **PHASEx<15:0>**: PWMx Phase-Shift Value or Independent Time Base Period for the PWM Generator bits

- Note 1:** If ITB (PWMCONx<9>) = 0, the following applies based on the mode of operation:  
Complementary, Redundant and Push-Pull Output mode (PMOD<1:0> (IOCON<11:10>) = 00, 01 or 10),  
PHASEx<15:0> = Phase-shift value for PWMxH and PWMxL outputs
- 2:** If ITB (PWMCONx<9>) = 1, the following applies based on the mode of operation:  
Complementary, Redundant and Push-Pull Output mode (PMOD<1:0> (IOCONx<11:10>) = 00, 01 or 10),  
PHASEx<15:0> = Independent time base period value for PWMxH and PWMxL



**REGISTER 16-16: LEBCONx: PWMx LEADING-EDGE BLANKING CONTROL REGISTER**

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	U-0	U-0
PHR	PHF	PLR	PLF	FLTLEBEN	CLLEBEN	—	—
bit 15						bit 8	
U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
—	—	BCH <sup>(1)</sup>	BCL <sup>(1)</sup>	BPHH	BPHL	BPLH	BPLL
bit 7						bit 0	

**Legend:**

R = Readable bit                      W = Writable bit                      U = Unimplemented bit, read as '0'  
-n = Value at POR                      '1' = Bit is set                      '0' = Bit is cleared                      x = Bit is unknown

- bit 15      **PHR:** PWMxH Rising Edge Trigger Enable bit  
1 = Rising edge of PWMxH will trigger Leading-Edge Blanking counter  
0 = Leading-Edge Blanking ignores rising edge of PWMxH
- bit 14      **PHF:** PWMxH Falling Edge Trigger Enable bit  
1 = Falling edge of PWMxH will trigger Leading-Edge Blanking counter  
0 = Leading-Edge Blanking ignores falling edge of PWMxH
- bit 13      **PLR:** PWMxL Rising Edge Trigger Enable bit  
1 = Rising edge of PWMxL will trigger Leading-Edge Blanking counter  
0 = Leading-Edge Blanking ignores rising edge of PWMxL
- bit 12      **PLF:** PWMxL Falling Edge Trigger Enable bit  
1 = Falling edge of PWMxL will trigger Leading-Edge Blanking counter  
0 = Leading-Edge Blanking ignores falling edge of PWMxL
- bit 11      **FLTLEBEN:** Fault Input Leading-Edge Blanking Enable bit  
1 = Leading-Edge Blanking is applied to selected Fault input  
0 = Leading-Edge Blanking is not applied to selected Fault input
- bit 10      **CLLEBEN:** Current-Limit Leading-Edge Blanking Enable bit  
1 = Leading-Edge Blanking is applied to selected current-limit input  
0 = Leading-Edge Blanking is not applied to selected current-limit input
- bit 9-6      **Unimplemented:** Read as '0'
- bit 5      **BCH:** Blanking in Selected Blanking Signal High Enable bit<sup>(1)</sup>  
1 = State blanking (of current-limit and/or Fault input signals) when selected blanking signal is high  
0 = No blanking when selected blanking signal is high
- bit 4      **BCL:** Blanking in Selected Blanking Signal Low Enable bit<sup>(1)</sup>  
1 = State blanking (of current-limit and/or Fault input signals) when selected blanking signal is low  
0 = No blanking when selected blanking signal is low
- bit 3      **BPHH:** Blanking in PWMxH High Enable bit  
1 = State blanking (of current-limit and/or Fault input signals) when PWMxH output is high  
0 = No blanking when PWMxH output is high
- bit 2      **BPHL:** Blanking in PWMxH Low Enable bit  
1 = State blanking (of current-limit and/or Fault input signals) when PWMxH output is low  
0 = No blanking when PWMxH output is low
- bit 1      **BPLH:** Blanking in PWMxL High Enable bit  
1 = State blanking (of current-limit and/or Fault input signals) when PWMxL output is high  
0 = No blanking when PWMxL output is high
- bit 0      **BPLL:** Blanking in PWMxL Low Enable bit  
1 = State blanking (of current-limit and/or Fault input signals) when PWMxL output is low  
0 = No blanking when PWMxL output is low

**Note 1:** The blanking signal is selected via the BLANKSELx bits in the AUXCONx register.

## 17.2 QEI Control Registers

REGISTER 17-1: QE1CON: QE1 CONTROL REGISTER

R/W-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
QE1EN	—	QE1SIDL	PIMOD2 <sup>(1)</sup>	PIMOD1 <sup>(1)</sup>	PIMOD0 <sup>(1)</sup>	IMV1 <sup>(2)</sup>	IMV0 <sup>(2)</sup>
bit 15							bit 8

U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
—	INTDIV2 <sup>(3)</sup>	INTDIV1 <sup>(3)</sup>	INTDIV0 <sup>(3)</sup>	CNTPOL	GATEN	CCM1	CCM0
bit 7							bit 0

**Legend:**

R = Readable bit                      W = Writable bit                      U = Unimplemented bit, read as '0'  
-n = Value at POR                      '1' = Bit is set                      '0' = Bit is cleared                      x = Bit is unknown

- bit 15            **QE1EN:** Quadrature Encoder Interface Module Counter Enable bit  
1 = Module counters are enabled  
0 = Module counters are disabled, but SFRs can be read or written to
- bit 14            **Unimplemented:** Read as '0'
- bit 13            **QE1SIDL:** QE1 Stop in Idle Mode bit  
1 = Discontinues module operation when device enters Idle mode  
0 = Continues module operation in Idle mode
- bit 12-10        **PIMOD<2:0>:** Position Counter Initialization Mode Select bits<sup>(1)</sup>  
111 = Reserved  
110 = Modulo Count mode for position counter  
101 = Resets the position counter when the position counter equals QE1GEC register  
100 = Second index event after home event initializes position counter with contents of QE1IC register  
011 = First index event after home event initializes position counter with contents of QE1IC register  
010 = Next index input event initializes the position counter with contents of QE1IC register  
001 = Every index input event resets the position counter  
000 = Index input event does not affect position counter
- bit 9            **IMV1:** Index Match Value for Phase B bit<sup>(2)</sup>  
1 = Phase B match occurs when QEB = 1  
0 = Phase B match occurs when QEB = 0
- bit 8            **IMV0:** Index Match Value for Phase A bit<sup>(2)</sup>  
1 = Phase A match occurs when QEA = 1  
0 = Phase A match occurs when QEA = 0
- bit 7            **Unimplemented:** Read as '0'

- Note 1:** When CCM<1:0> = 10 or 11, all of the QE1 counters operate as timers and the PIMOD<2:0> bits are ignored.
- 2:** When CCM<1:0> = 00, and QEA and QEB values match the Index Match Value (IMV), the POSCNTNTH and POSCNTL registers are reset. QEA/QEB signals used for the index match have swap and polarity values applied, as determined by the SWPAB and QEAPOL/QEBPOL bits.
- 3:** The selected clock rate should be at least twice the expected maximum quadrature count rate.

**REGISTER 17-13: QE11LECH: QE11 LESS THAN OR EQUAL COMPARE HIGH WORD REGISTER**

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
QEILEC<31:24>							
bit 15				bit 8			

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
QEILEC<23:16>							
bit 7				bit 0			

**Legend:**

R = Readable bit

W = Writable bit

U = Unimplemented bit, read as '0'

-n = Value at POR

'1' = Bit is set

'0' = Bit is cleared

x = Bit is unknown

bit 15-0      **QEILEC<31:16>**: High Word Used to Form 32-Bit Less Than or Equal Compare Register (QE11LEC) bits

**REGISTER 17-14: QE11LECL: QE11 LESS THAN OR EQUAL COMPARE LOW WORD REGISTER**

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
QEILEC<15:8>							
bit 15				bit 8			

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
QEILEC<7:0>							
bit 7				bit 0			

**Legend:**

R = Readable bit

W = Writable bit

U = Unimplemented bit, read as '0'

-n = Value at POR

'1' = Bit is set

'0' = Bit is cleared

x = Bit is unknown

bit 15-0      **QEILEC<15:0>**: Low Word Used to Form 32-Bit Less Than or Equal Compare Register (QE11LEC) bits

**REGISTER 23-8: AD1CSSL: ADC1 INPUT SCAN SELECT REGISTER LOW<sup>(1,2)</sup>**

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
CSS15	CSS14	CSS13	CSS12	CSS11	CSS10	CSS9	CSS8
bit 15							bit 8

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
CSS7	CSS6	CSS5	CSS4	CSS3	CSS2	CSS1	CSS0
bit 7							bit 0

**Legend:**

R = Readable bit                      W = Writable bit                      U = Unimplemented bit, read as '0'  
 -n = Value at POR                      '1' = Bit is set                      '0' = Bit is cleared                      x = Bit is unknown

bit 15-0                      **CSS<15:0>**: ADC1 Input Scan Selection bits

- 1 = Selects ANx for input scan
- 0 = Skips ANx for input scan

**Note 1:** On devices with less than 16 analog inputs, all AD1CSSL bits can be selected by the user. However, inputs selected for scan, without a corresponding input on the device, convert VREFL.

**2:** CSSx = ANx, where x = 0-15.

**REGISTER 25-6: CMxFLTR: COMPARATOR x FILTER CONTROL REGISTER**

U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
—	—	—	—	—	—	—	—
bit 15							bit 8

U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
—	CFSEL2	CFSEL1	CFSEL0	CFLTREN	CFDIV2	CFDIV1	CFDIV0
bit 7							bit 0

**Legend:**

R = Readable bit

W = Writable bit

U = Unimplemented bit, read as '0'

-n = Value at POR

'1' = Bit is set

'0' = Bit is cleared

x = Bit is unknown

bit 15-7 **Unimplemented:** Read as '0'

bit 6-4 **CFSEL<2:0>:** Comparator Filter Input Clock Select bits

111 = T5CLK<sup>(1)</sup>

110 = T4CLK<sup>(2)</sup>

101 = T3CLK<sup>(1)</sup>

100 = T2CLK<sup>(2)</sup>

011 = Reserved

010 = SYNCO1<sup>(3)</sup>

001 = Fosc<sup>(4)</sup>

000 = Fp<sup>(4)</sup>

bit 3 **CFLTREN:** Comparator Filter Enable bit

1 = Digital filter is enabled

0 = Digital filter is disabled

bit 2-0 **CFDIV<2:0>:** Comparator Filter Clock Divide Select bits

111 = Clock Divide 1:128

110 = Clock Divide 1:64

101 = Clock Divide 1:32

100 = Clock Divide 1:16

011 = Clock Divide 1:8

010 = Clock Divide 1:4

001 = Clock Divide 1:2

000 = Clock Divide 1:1

**Note 1:** See the Type C Timer Block Diagram (Figure 13-2).

**Note 2:** See the Type B Timer Block Diagram (Figure 13-1).

**Note 3:** See the High-Speed PWMx Module Register Interconnection Diagram (Figure 16-2).

**Note 4:** See the Oscillator System Diagram (Figure 9-1).

TABLE 27-2: CONFIGURATION BITS DESCRIPTION

Bit Field	Description
GCP	General Segment Code-Protect bit 1 = User program memory is not code-protected 0 = Code protection is enabled for the entire program memory space
GWRP	General Segment Write-Protect bit 1 = User program memory is not write-protected 0 = User program memory is write-protected
IESO	Two-Speed Oscillator Start-up Enable bit 1 = Start up device with FRC, then automatically switch to the user-selected oscillator source when ready 0 = Start up device with user-selected oscillator source
PWMLOCK <sup>(1)</sup>	PWM Lock Enable bit 1 = Certain PWM registers may only be written after a key sequence 0 = PWM registers may be written without a key sequence
FNOSC<2:0>	Oscillator Selection bits 111 = Fast RC Oscillator with Divide-by-N (FRCDIVN) 110 = Fast RC Oscillator with Divide-by-16 (FRCDIV16) 101 = Low-Power RC Oscillator (LPRC) 100 = Reserved; do not use 011 = Primary Oscillator with PLL module (XT + PLL, HS + PLL, EC + PLL) 010 = Primary Oscillator (XT, HS, EC) 001 = Fast RC Oscillator with Divide-by-N with PLL module (FRCPLL) 000 = Fast RC Oscillator (FRC)
FCKSM<1:0>	Clock Switching Mode bits 1x = Clock switching is disabled, Fail-Safe Clock Monitor is disabled 01 = Clock switching is enabled, Fail-Safe Clock Monitor is disabled 00 = Clock switching is enabled, Fail-Safe Clock Monitor is enabled
IOL1WAY	Peripheral Pin Select Configuration bit 1 = Allow only one reconfiguration 0 = Allow multiple reconfigurations
OSCIOFNC	OSC2 Pin Function bit (except in XT and HS modes) 1 = OSC2 is the clock output 0 = OSC2 is a general purpose digital I/O pin
POSCMD<1:0>	Primary Oscillator Mode Select bits 11 = Primary Oscillator is disabled 10 = HS Crystal Oscillator mode 01 = XT Crystal Oscillator mode 00 = EC (External Clock) mode
FWDTEN	Watchdog Timer Enable bit 1 = Watchdog Timer is always enabled (LPRC oscillator cannot be disabled. Clearing the SWDTEN bit in the RCON register will have no effect.) 0 = Watchdog Timer is enabled/disabled by user software (LPRC can be disabled by clearing the SWDTEN bit in the RCON register)
WINDIS	Watchdog Timer Window Enable bit 1 = Watchdog Timer in Non-Window mode 0 = Watchdog Timer in Window mode
PLLKEN	PLL Lock Enable bit 1 = PLL lock is enabled 0 = PLL lock is disabled

**Note 1:** This bit is only available on dsPIC33EPXXXMC20X/50X and PIC24EPXXXMC20X devices.

**2:** When JTAGEN = 1, an internal pull-up resistor is enabled on the TMS pin. Erased devices default to JTAGEN = 1. Applications requiring I/O pins in a high-impedance state (tri-state) in Reset should use pins other than TMS for this purpose.

**FIGURE 30-29: SPI1 SLAVE MODE (FULL-DUPLEX, CKE = 0, CKP = 0, SMP = 0)  
TIMING CHARACTERISTICS**

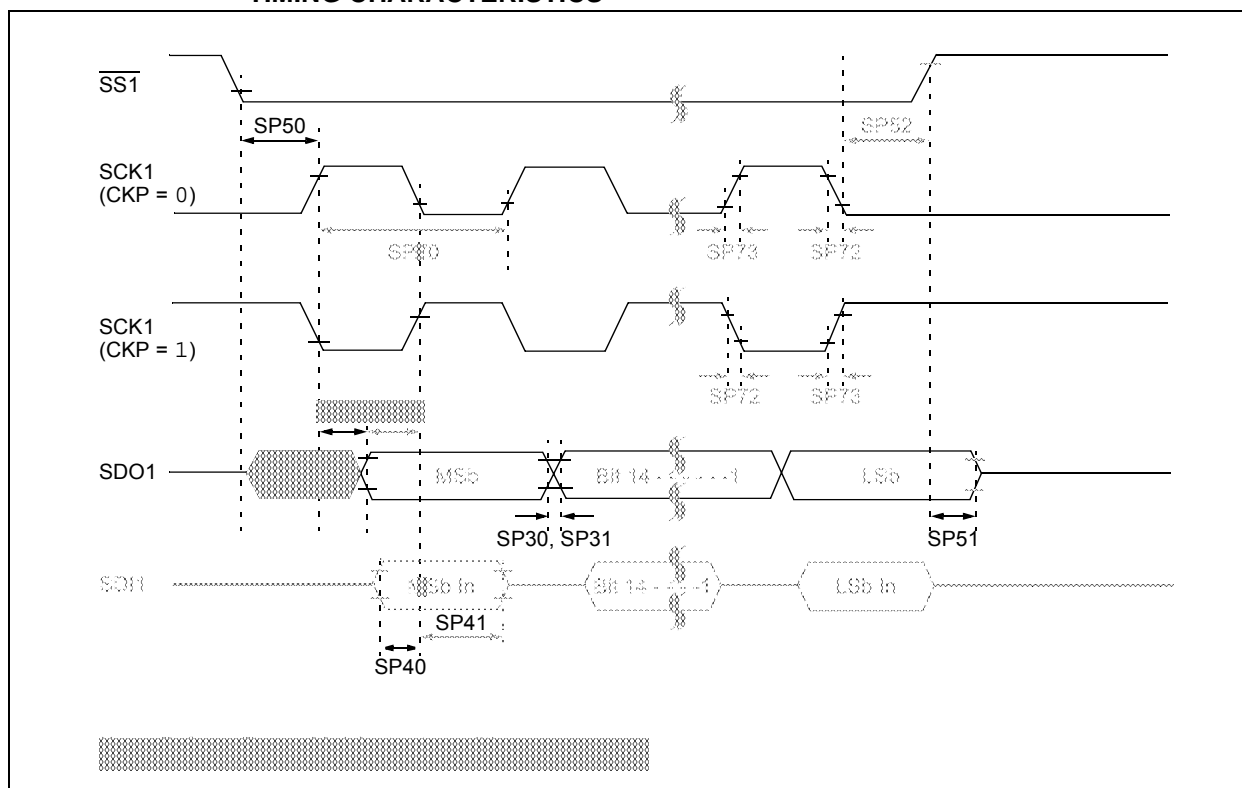


FIGURE 30-30: I2Cx BUS START/STOP BITS TIMING CHARACTERISTICS (MASTER MODE)

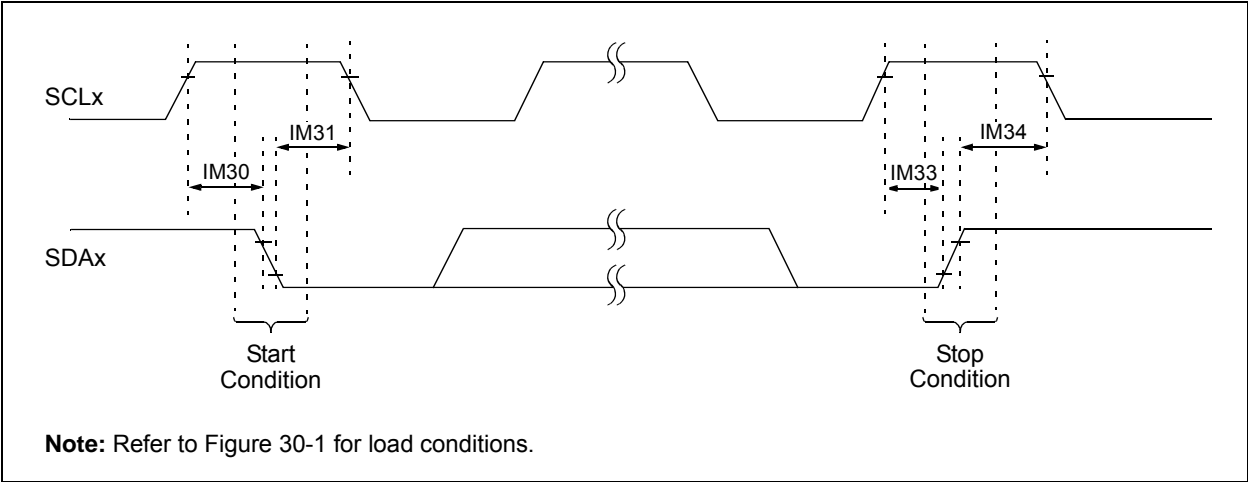


FIGURE 30-31: I2Cx BUS DATA TIMING CHARACTERISTICS (MASTER MODE)

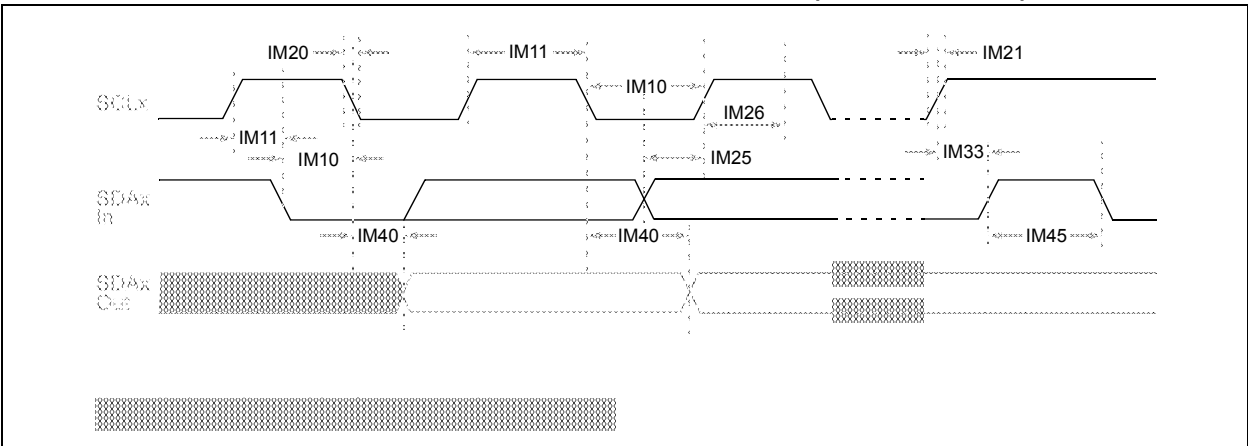




TABLE 30-54: OP AMP/COMPARATOR VOLTAGE REFERENCE SETTling TIME SPECIFICATIONS

AC CHARACTERISTICS			Standard Operating Conditions (see Note 2): 3.0V to 3.6V (unless otherwise stated) Operating temperature -40°C ≤ TA ≤ +85°C for Industrial -40°C ≤ TA ≤ +125°C for Extended				
Param.	Symbol	Characteristic	Min.	Typ.	Max.	Units	Conditions
VR310	TSET	Settling Time	—	1	10	μs	(Note 1)

**Note 1:** Settling time is measured while CVRR = 1 and CVR<3:0> bits transition from '0000' to '1111'.

**2:** Device is functional at VBORMIN < VDD < VDDMIN, but will have degraded performance. Device functionality is tested, but not characterized. Analog modules (ADC, op amp/comparator and comparator voltage reference) may have degraded performance. Refer to Parameter BO10 in Table 30-13 for the minimum and maximum BOR values.

TABLE 30-55: OP AMP/COMPARATOR VOLTAGE REFERENCE SPECIFICATIONS

DC CHARACTERISTICS			Standard Operating Conditions (see Note 1): 3.0V to 3.6V (unless otherwise stated) Operating temperature -40°C ≤ TA ≤ +85°C for Industrial -40°C ≤ TA ≤ +125°C for Extended				
Param No.	Symbol	Characteristics	Min.	Typ.	Max.	Units	Conditions
VRD310	CVRES	Resolution	CVRSRC/24	—	CVRSRC/32	LSb	
VRD311	CVRAA	Absolute Accuracy <sup>(2)</sup>	—	±25	—	mV	CVRSRC = 3.3V
VRD313	CVRSRC	Input Reference Voltage	0	—	AVDD + 0.3	V	
VRD314	CVRROUT	Buffer Output Resistance <sup>(2)</sup>	—	1.5k	—	Ω	

**Note 1:** Device is functional at VBORMIN < VDD < VDDMIN, but will have degraded performance. Device functionality is tested, but not characterized. Analog modules (ADC, op amp/comparator and comparator voltage reference) may have degraded performance. Refer to Parameter BO10 in Table 30-13 for the minimum and maximum BOR values.

**2:** Parameter is characterized but not tested in manufacturing.

TABLE 30-58: ADC MODULE SPECIFICATIONS (12-BIT MODE)

AC CHARACTERISTICS			Standard Operating Conditions: 3.0V to 3.6V (unless otherwise stated) <sup>(1)</sup> Operating temperature -40°C ≤ TA ≤ +85°C for Industrial -40°C ≤ TA ≤ +125°C for Extended				
Param No.	Symbol	Characteristic	Min.	Typ.	Max.	Units	Conditions
ADC Accuracy (12-Bit Mode)							
AD20a	Nr	Resolution	12 Data Bits			bits	
AD21a	INL	Integral Nonlinearity	-2.5	—	2.5	LSb	-40°C ≤ TA ≤ +85°C (Note 2)
			-5.5	—	5.5	LSb	+85°C < TA ≤ +125°C (Note 2)
AD22a	DNL	Differential Nonlinearity	-1	—	1	LSb	-40°C ≤ TA ≤ +85°C (Note 2)
			-1	—	1	LSb	+85°C < TA ≤ +125°C (Note 2)
AD23a	GERR	Gain Error <sup>(3)</sup>	-10	—	10	LSb	-40°C ≤ TA ≤ +85°C (Note 2)
			-10	—	10	LSb	+85°C < TA ≤ +125°C (Note 2)
AD24a	EOFF	Offset Error	-5	—	5	LSb	-40°C ≤ TA ≤ +85°C (Note 2)
			-5	—	5	LSb	+85°C < TA ≤ +125°C (Note 2)
AD25a	—	Monotonicity	—	—	—	—	Guaranteed
Dynamic Performance (12-Bit Mode)							
AD30a	THD	Total Harmonic Distortion <sup>(3)</sup>	—	75	—	dB	
AD31a	SINAD	Signal to Noise and Distortion <sup>(3)</sup>	—	68	—	dB	
AD32a	SFDR	Spurious Free Dynamic Range <sup>(3)</sup>	—	80	—	dB	
AD33a	FNYQ	Input Signal Bandwidth <sup>(3)</sup>	—	250	—	kHz	
AD34a	ENOB	Effective Number of Bits <sup>(3)</sup>	11.09	11.3	—	bits	

**Note 1:** Device is functional at VBORMIN < VDD < VDDMIN, but will have degraded performance. Device functionality is tested, but not characterized. Analog modules (ADC, op amp/comparator and comparator voltage reference) may have degraded performance. Refer to Parameter BO10 in Table 30-13 for the minimum and maximum BOR values.

**2:** For all accuracy specifications, VINL = AVSS = VREFL = 0V and AVDD = VREFH = 3.6V.

**3:** Parameters are characterized but not tested in manufacturing.

TABLE 31-11: INTERNAL RC ACCURACY

AC CHARACTERISTICS		Standard Operating Conditions: 3.0V to 3.6V (unless otherwise stated) Operating temperature $-40^{\circ}\text{C} \leq T_A \leq +150^{\circ}\text{C}$					
Param No.	Characteristic	Min	Typ	Max	Units	Conditions	
HF21	LPRC @ 32.768 kHz <sup>(1,2)</sup>						
	LPRC	-30	—	+30	%	$-40^{\circ}\text{C} \leq T_A \leq +150^{\circ}\text{C}$	VDD = 3.0-3.6V

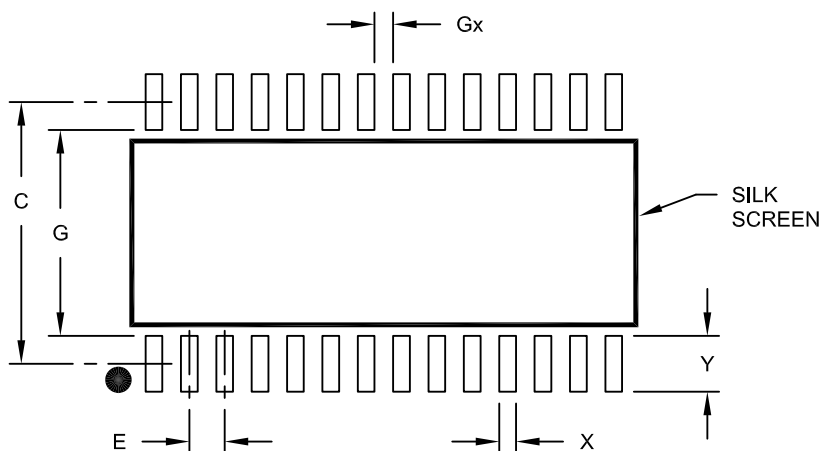
**Note 1:** Change of LPRC frequency as VDD changes.

**Note 2:** LPRC accuracy impacts the Watchdog Timer Time-out Period (TWDT). See **Section 27.5 “Watchdog Timer (WDT)”** for more information.

**NOTES:**

28-Lead Plastic Small Outline (SO) - Wide, 7.50 mm Body [SOIC]

**Note:** For the most current package drawings, please see the Microchip Packaging Specification located at <http://www.microchip.com/packaging>



RECOMMENDED LAND PATTERN

Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Contact Pitch	E	1.27 BSC		
Contact Pad Spacing	C		9.40	
Contact Pad Width (X28)	X			0.60
Contact Pad Length (X28)	Y			2.00
Distance Between Pads	Gx	0.67		
Distance Between Pads	G	7.40		

Notes:

1. Dimensioning and tolerancing per ASME Y14.5M

BSC: Basic Dimension. Theoretically exact value shown without tolerances.

Microchip Technology Drawing No. C04-2052A