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What is "[Embedded - Microcontrollers](#)"?

"[Embedded - Microcontrollers](#)" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "[Embedded - Microcontrollers](#)"

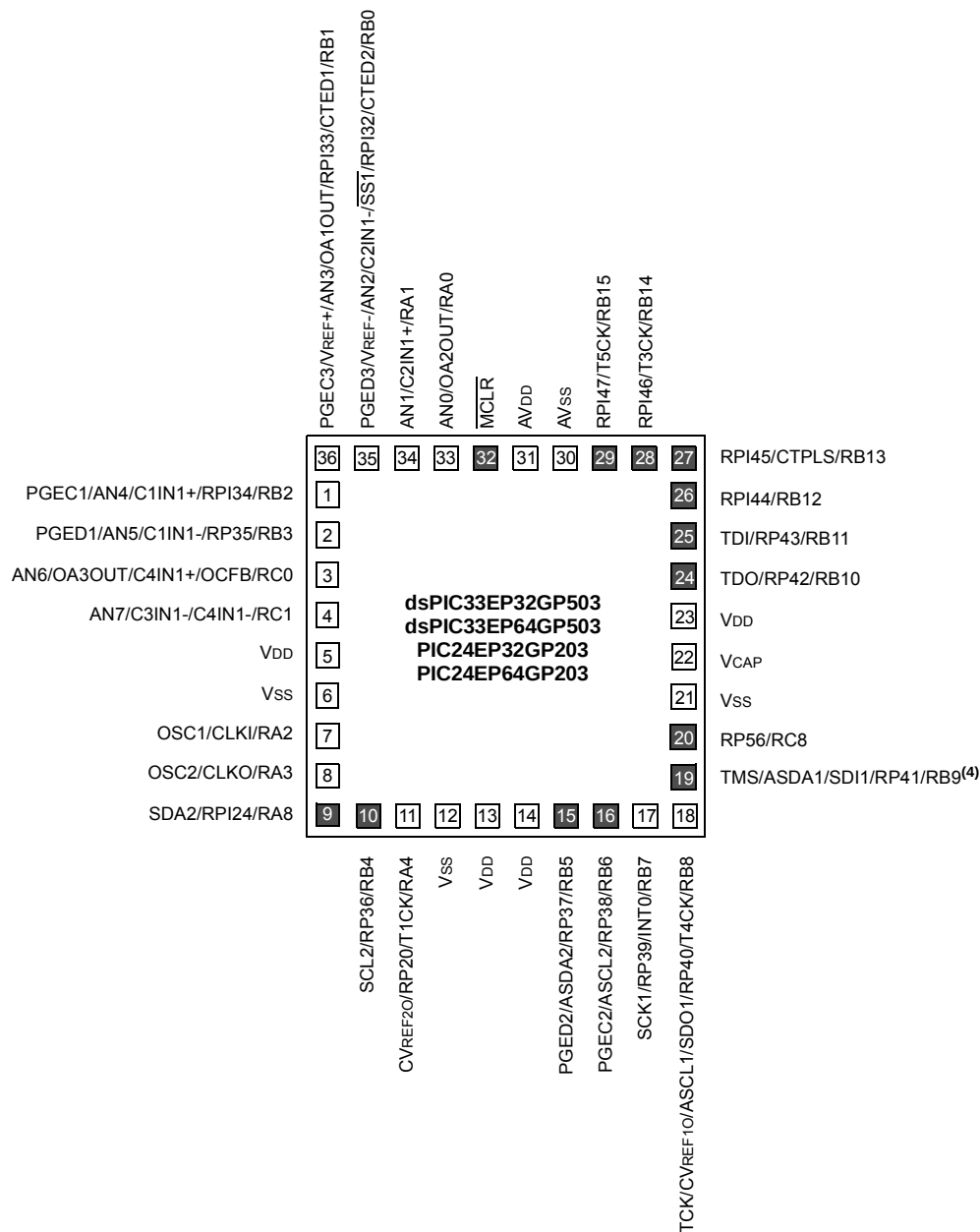
Details

Product Status	Obsolete
Core Processor	PIC
Core Size	16-Bit
Speed	60 MIPS
Connectivity	I ² C, IrDA, LINbus, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, DMA, POR, PWM, WDT
Number of I/O	35
Program Memory Size	32KB (10.7K x 24)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	2K x 16
Voltage - Supply (Vcc/Vdd)	3V ~ 3.6V
Data Converters	A/D 9x10b/12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 150°C (TA)
Mounting Type	Surface Mount
Package / Case	44-VFTLA Exposed Pad
Supplier Device Package	44-VTLA (6x6)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/pic24ep32gp204-h-tl

Pin Diagrams (Continued)

36-Pin VTLA^(1,2,3)

■ = Pins are up to 5V tolerant



- Note**
- 1: The RPN/RPIN pins can be used by any remappable peripheral with some limitation. See **Section 11.4 “Peripheral Pin Select (PPS)”** for available peripherals and for information on limitations.
 - 2: Every I/O port pin (RAX-RGX) can be used as a Change Notification pin (CNAX-CNGX). See **Section 11.0 “I/O Ports”** for more information.
 - 3: The metal pad at the bottom of the device is not connected to any pins and is recommended to be connected to VSS externally.
 - 4: There is an internal pull-up resistor connected to the TMS pin when the JTAG interface is active. See the JTAGEN bit field in Table 27-2.

FIGURE 2-5: SINGLE-PHASE SYNCHRONOUS BUCK CONVERTER

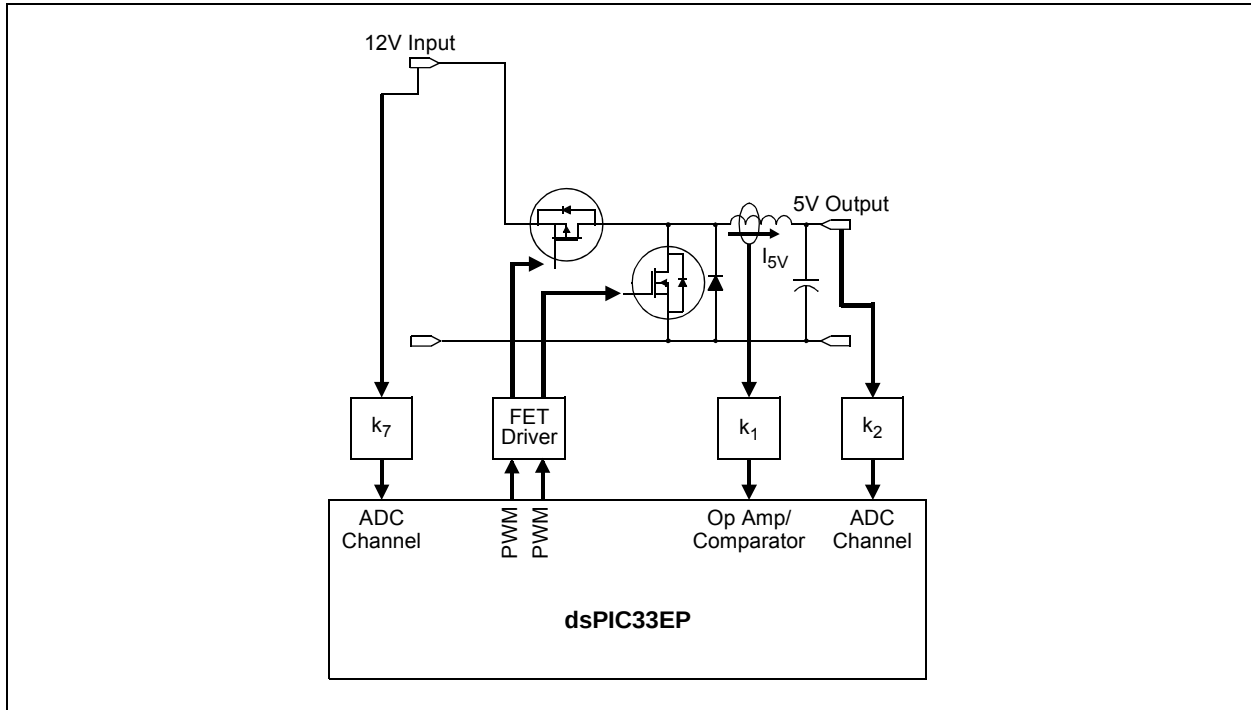


FIGURE 2-6: MULTIPHASE SYNCHRONOUS BUCK CONVERTER

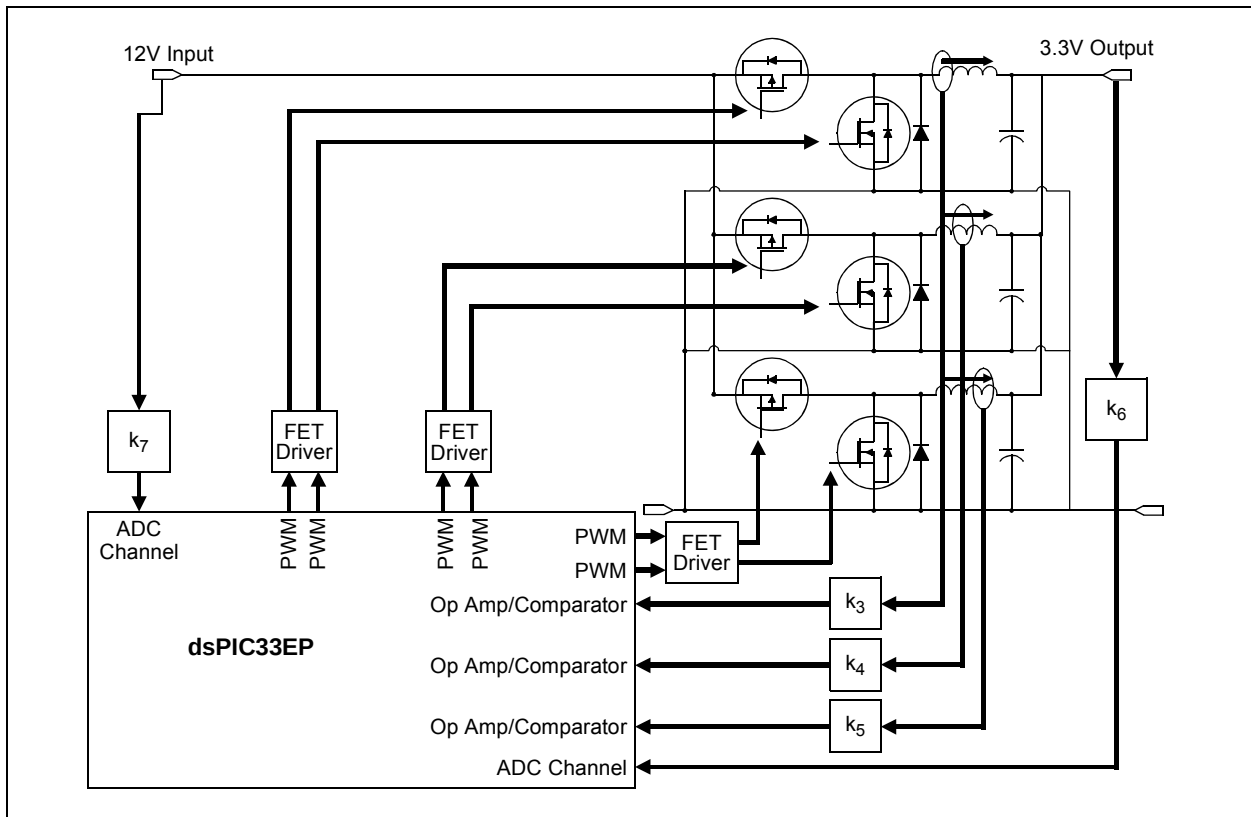
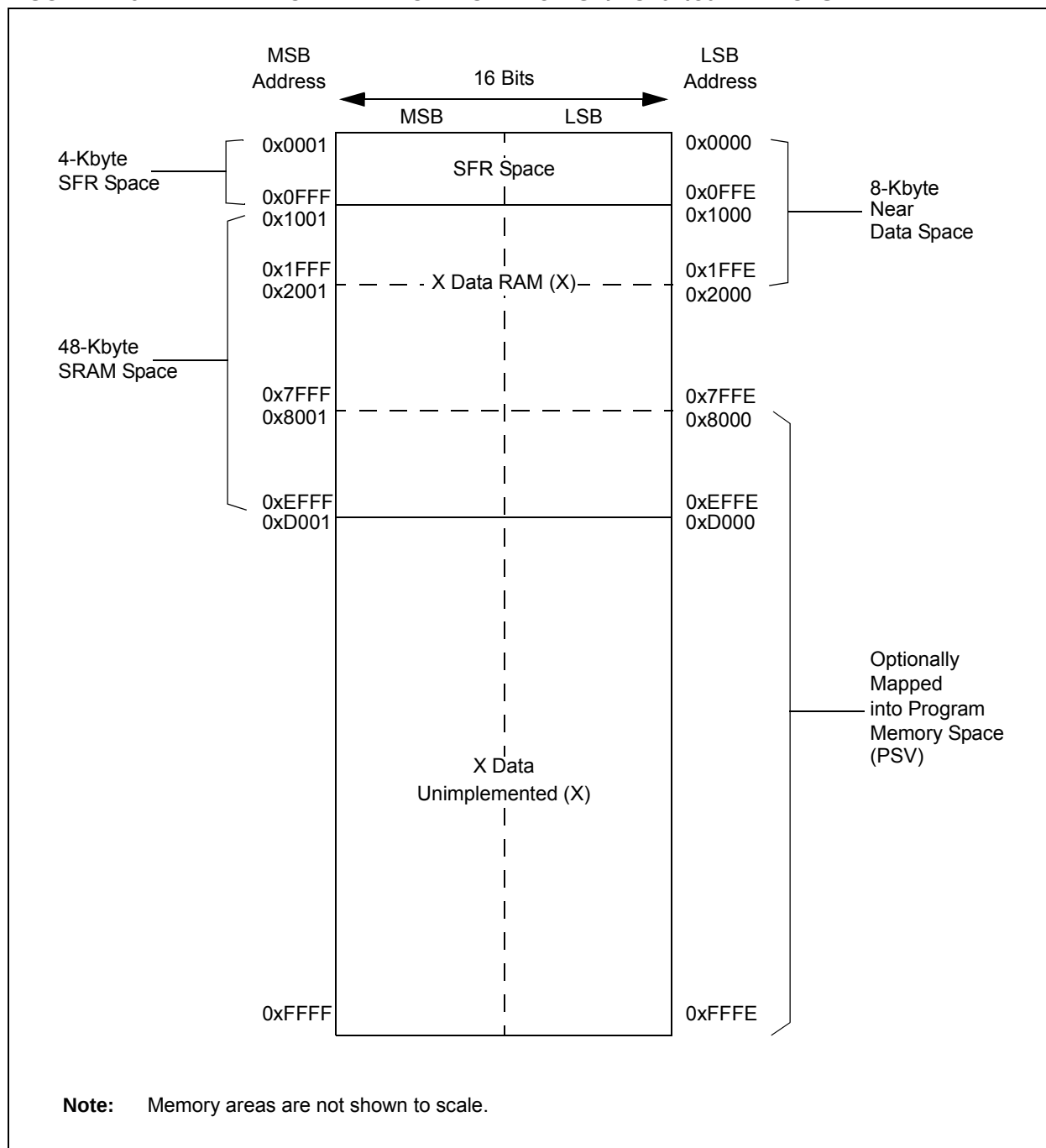


FIGURE 4-16: DATA MEMORY MAP FOR PIC24EP512GP/MC20X/50X DEVICES



4.4 Special Function Register Maps

TABLE 4-1: CPU CORE REGISTER MAP FOR dsPIC33EPXXMC20X/50X AND dsPIC33EPXXG50X DEVICES ONLY

File Name	Addr.	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	All Resets	
W0	0000	W0 (WREG)																	xxxx
W1	0002	W1																	xxxx
W2	0004	W2																	xxxx
W3	0006	W3																	xxxx
W4	0008	W4																	xxxx
W5	000A	W5																	xxxx
W6	000C	W6																	xxxx
W7	000E	W7																	xxxx
W8	0010	W8																	xxxx
W9	0012	W9																	xxxx
W10	0014	W10																	xxxx
W11	0016	W11																	xxxx
W12	0018	W12																	xxxx
W13	001A	W13																	xxxx
W14	001C	W14																	xxxx
W15	001E	W15																	xxxx
SPLIM	0020	SPLIM																	0000
ACCAL	0022	ACCAL																	0000
ACCAH	0024	ACCAH																	0000
ACCAU	0026	Sign Extension of ACCA<39>										ACCAU							0000
ACCBL	0028	ACCBL																	0000
ACCBH	002A	ACCBH																	0000
ACCBU	002C	Sign Extension of ACCB<39>										ACCBU							0000
PCL	002E	PCL<15:0>																—	0000
PCH	0030	—	—	—	—	—	—	—	—	—	PCH<6:0>							0000	
DSRPAG	0032	—	—	—	—	—	—	DSRPAG<9:0>											0001
DSWPAG	0034	—	—	—	—	—	—	—	DSWPAG<8:0>										0001
RCOUNT	0036	RCOUNT<15:0>																	0000
DCOUNT	0038	DCOUNT<15:0>																	0000
DOSTARTL	003A	DOSTARTL<15:1>																—	0000
DOSTARTH	003C	—	—	—	—	—	—	—	—	—	—	DOSTARTH<5:0>						0000	
DOENDL	003E	DOENDL<15:1>																—	0000
DOENDH	0040	—	—	—	—	—	—	—	—	—	—	DOENDH<5:0>						0000	

Legend: x = unknown value on Reset, — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

TABLE 4-3: INTERRUPT CONTROLLER REGISTER MAP FOR PIC24EPXXXGP20X DEVICES ONLY

File Name	Addr.	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	All Resets
IFS0	0800	—	DMA1IF	AD1IF	U1TXIF	U1RXIF	SPI1IF	SPI1EIF	T3IF	T2IF	OC2IF	IC2IF	DMA0IF	T1IF	OC1IF	IC1IF	INT0IF	0000
IFS1	0802	U2TXIF	U2RXIF	INT2IF	T5IF	T4IF	OC4IF	OC3IF	DMA2IF	—	—	—	INT1IF	CNIF	CMIF	M12C1IF	SI2C1IF	0000
IFS2	0804	—	—	—	—	—	—	—	—	—	IC4IF	IC3IF	DMA3IF	—	—	SPI2IF	SPI2EIF	0000
IFS3	0806	—	—	—	—	—	—	—	—	—	—	—	—	—	M12C2IF	SI2C2IF	—	0000
IFS4	0808	—	—	CTMUIF	—	—	—	—	—	—	—	—	—	CRCIF	U2EIF	U1EIF	—	0000
IFS8	0810	JTAGIF	ICDIF	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
IFS9	0812	—	—	—	—	—	—	—	—	—	PTG3IF	PTG2IF	PTG1IF	PTG0IF	PTGWDTIF	PTGSTIEIF	—	0000
IEC0	0820	—	DMA1IE	AD1IE	U1TXIE	U1RXIE	SPI1IE	SPI1EIE	T3IE	T2IE	OC2IE	IC2IE	DMA0IE	T1IE	OC1IE	IC1IE	INT0IE	0000
IEC1	0822	U2TXIE	U2RXIE	INT2IE	T5IE	T4IE	OC4IE	OC3IE	DMA2IE	—	—	—	INT1IE	CNIE	CMIE	M12C1IE	SI2C1IE	0000
IEC2	0824	—	—	—	—	—	—	—	—	—	IC4IE	IC3IE	DMA3IE	—	—	SPI2IE	SPI2EIE	0000
IEC3	0826	—	—	—	—	—	—	—	—	—	—	—	—	—	M12C2IE	SI2C2IE	—	0000
IEC4	0828	—	—	CTMUIE	—	—	—	—	—	—	—	—	—	CRCIE	U2EIE	U1EIE	—	0000
IEC8	0830	JTAGIE	ICDIE	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
IEC9	0832	—	—	—	—	—	—	—	—	—	PTG3IE	PTG2IE	PTG1IE	PTG0IE	PTGWDTIE	PTGSTIEIE	—	0000
IPC0	0840	—	T1IP<2:0>			—	OC1IP<2:0>			—	IC1IP<2:0>			—	INT0IP<2:0>			4444
IPC1	0842	—	T2IP<2:0>			—	OC2IP<2:0>			—	IC2IP<2:0>			—	DMA0IP<2:0>			4444
IPC2	0844	—	U1RXIP<2:0>			—	SPI1IP<2:0>			—	SPI1EIP<2:0>			—	T3IP<2:0>			4444
IPC3	0846	—	—	—	—	—	DMA1IP<2:0>			—	AD1IP<2:0>			—	U1TXIP<2:0>			0444
IPC4	0848	—	CNIP<2:0>			—	CMIP<2:0>			—	M12C1IP<2:0>			—	SI2C1IP<2:0>			4444
IPC5	084A	—	—	—	—	—	—	—	—	—	—	—	—	—	INT1IP<2:0>			0004
IPC6	084C	—	T4IP<2:0>			—	OC4IP<2:0>			—	OC3IP<2:0>			—	DMA2IP<2:0>			4444
IPC7	084E	—	U2TXIP<2:0>			—	U2RXIP<2:0>			—	INT2IP<2:0>			—	T5IP<2:0>			4444
IPC8	0850	—	—	—	—	—	—	—	—	—	SPI2IP<2:0>			—	SPI2EIP<2:0>			0044
IPC9	0852	—	—	—	—	—	IC4IP<2:0>			—	IC3IP<2:0>			—	DMA3IP<2:0>			0444
IPC12	0858	—	—	—	—	—	M12C2IP<2:0>			—	SI2C2IP<2:0>			—	—	—	—	0440
IPC16	0860	—	CRCIP<2:0>			—	U2EIP<2:0>			—	U1EIP<2:0>			—	—	—	—	4440
IPC19	0866	—	—	—	—	—	—	—	—	—	CTMUIP<2:0>			—	—	—	—	0040
IPC35	0886	—	JTAGIP<2:0>			—	ICDIP<2:0>			—	—	—	—	—	—	—	—	4400
IPC36	0888	—	PTG0IP<2:0>			—	PTGWDTIP<2:0>			—	PTGSTIEIP<2:0>			—	—	—	—	4440
IPC37	088A	—	—	—	—	—	PTG3IP<2:0>			—	PTG2IP<2:0>			—	PTG1IP<2:0>			0444
INTCON1	08C0	NSTDIS	OVAERR	OVBERR	—	—	—	—	—	—	DIV0ERR	DMACERR	MATHERR	ADDRERR	STKERR	OSCFAIL	—	0000
INTCON2	08C2	GIE	DISI	SWTRAP	—	—	—	—	—	—	—	—	—	—	INT2EP	INT1EP	INT0EP	8000
INTCON3	08C4	—	—	—	—	—	—	—	—	—	—	DAE	DOOVR	—	—	—	—	0000
INTCON4	08C6	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	SGHT	0000
INTTREG	08C8	—	—	—	—	ILR<3:0>				VECNUM<7:0>								0000

Legend: — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

TABLE 4-7: INTERRUPT CONTROLLER REGISTER MAP FOR dsPIC33EPXXXMC50X DEVICES ONLY

File Name	Addr.	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	All Resets
IFS0	0800	—	DMA1IF	AD1IF	U1TXIF	U1RXIF	SPI1IF	SPI1EIF	T3IF	T2IF	OC2IF	IC2IF	DMA0IF	T1IF	OC1IF	IC1IF	INT0IF	0000
IFS1	0802	U2TXIF	U2RXIF	INT2IF	T5IF	T4IF	OC4IF	OC3IF	DMA2IF	—	—	—	INT1IF	CNIF	CMIF	M12C1IF	SI2C1IF	0000
IFS2	0804	—	—	—	—	—	—	—	—	—	IC4IF	IC3IF	DMA3IF	C1IF	C1RXIF	SPI2IF	SPI2EIF	0000
IFS3	0806	—	—	—	—	—	QE11IF	PSEMIF	—	—	—	—	—	—	M12C2IF	SI2C2IF	—	0000
IFS4	0808	—	—	CTMUIF	—	—	—	—	—	—	C1TXIF	—	—	CRCIF	U2EIF	U1EIF	—	0000
IFS5	080A	PWM2IF	PWM1IF	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
IFS6	080C	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	PWM3IF	0000
IFS8	0810	JTAGIF	ICDIF	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
IFS9	0812	—	—	—	—	—	—	—	—	—	PTG3IF	PTG2IF	PTG1IF	PTG0IF	PTGWDTIF	PTGSTEIF	—	0000
IEC0	0820	—	DMA1IE	AD1IE	U1TXIE	U1RXIE	SPI1IE	SPI1EIE	T3IE	T2IE	OC2IE	IC2IE	DMA0IE	T1IE	OC1IE	IC1IE	INT0IE	0000
IEC1	0822	U2TXIE	U2RXIE	INT2IE	T5IE	T4IE	OC4IE	OC3IE	DMA2IE	—	—	—	INT1IE	CNIE	CMIE	M12C1IE	SI2C1IE	0000
IEC2	0824	—	—	—	—	—	—	—	—	—	IC4IE	IC3IE	DMA3IE	C1IE	C1RXIE	SPI2IE	SPI2EIE	0000
IEC3	0826	—	—	—	—	—	QE11IE	PSEMIE	—	—	—	—	—	—	M12C2IE	SI2C2IE	—	0000
IEC4	0828	—	—	CTMUIE	—	—	—	—	—	—	C1TXIE	—	—	CRCIE	U2EIE	U1EIE	—	0000
IEC5	082A	PWM2IE	PWM1IE	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
IEC6	082C	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	PWM3IE	0000
IEC7	082E	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
IEC8	0830	JTAGIE	ICDIE	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
IEC9	0832	—	—	—	—	—	—	—	—	—	PTG3IE	PTG2IE	PTG1IE	PTG0IE	PTGWDTIE	PTGSTIEIE	—	0000
IPC0	0840	—	T1IP<2:0>			—	OC1IP<2:0>			—	IC1IP<2:0>			—	INT0IP<2:0>			4444
IPC1	0842	—	T2IP<2:0>			—	OC2IP<2:0>			—	IC2IP<2:0>			—	DMA0IP<2:0>			4444
IPC2	0844	—	U1RXIP<2:0>			—	SPI1IP<2:0>			—	SPI1EIP<2:0>			—	T3IP<2:0>			4444
IPC3	0846	—	—	—	—	—	DMA1IP<2:0>			—	AD1IP<2:0>			—	U1TXIP<2:0>			0444
IPC4	0848	—	CNIP<2:0>			—	CMIP<2:0>			—	M12C1IP<2:0>			—	SI2C1IP<2:0>			4444
IPC5	084A	—	—	—	—	—	—	—	—	—	—	—	—	—	INT1IP<2:0>			0004
IPC6	084C	—	T4IP<2:0>			—	OC4IP<2:0>			—	OC3IP<2:0>			—	DMA2IP<2:0>			4444
IPC7	084E	—	U2TXIP<2:0>			—	U2RXIP<2:0>			—	INT2IP<2:0>			—	T5IP<2:0>			4444
IPC8	0850	—	C1IP<2:0>			—	C1RXIP<2:0>			—	SPI2IP<2:0>			—	SPI2EIP<2:0>			4444
IPC9	0852	—	—	—	—	—	IC4IP<2:0>			—	IC3IP<2:0>			—	DMA3IP<2:0>			0444
IPC12	0858	—	—	—	—	—	M12C2IP<2:0>			—	SI2C2IP<2:0>			—	—	—	—	0440
IPC14	085C	—	—	—	—	—	QE11IP<2:0>			—	PSEMIP<2:0>			—	—	—	—	0440
IPC16	0860	—	CRCIP<2:0>			—	U2EIP<2:0>			—	U1EIP<2:0>			—	—	—	—	4440
IPC17	0862	—	—	—	—	—	C1TXIP<2:0>			—	—	—	—	—	—	—	—	0400
IPC19	0866	—	—	—	—	—	—	—	—	—	CTMUIP<2:0>			—	—	—	—	0040

Legend: — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

TABLE 4-17: I2C1 AND I2C2 REGISTER MAP

File Name	Addr.	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	All Resets	
I2C1RCV	0200	—	—	—	—	—	—	—	—	I2C1 Receive Register									0000
I2C1TRN	0202	—	—	—	—	—	—	—	—	I2C1 Transmit Register									00FF
I2C1BRG	0204	—	—	—	—	—	—	—	Baud Rate Generator										0000
I2C1CON	0206	I2CEN	—	I2CSIDL	SCLREL	IPMIEN	A10M	DISSLW	SMEN	GCEN	STREN	ACKDT	ACKEN	RCEN	PEN	RSEN	SEN	1000	
I2C1STAT	0208	ACKSTAT	TRSTAT	—	—	—	BCL	GCSTAT	ADD10	IWCOL	I2COV	D_A	P	S	R_W	RBF	TBF	0000	
I2C1ADD	020A	—	—	—	—	—	—	I2C1 Address Register											0000
I2C1MSK	020C	—	—	—	—	—	—	I2C1 Address Mask											0000
I2C2RCV	0210	—	—	—	—	—	—	—	—	I2C2 Receive Register									0000
I2C2TRN	0212	—	—	—	—	—	—	—	—	I2C2 Transmit Register									00FF
I2C2BRG	0214	—	—	—	—	—	—	—	Baud Rate Generator										0000
I2C2CON	0216	I2CEN	—	I2CSIDL	SCLREL	IPMIEN	A10M	DISSLW	SMEN	GCEN	STREN	ACKDT	ACKEN	RCEN	PEN	RSEN	SEN	1000	
I2C2STAT	0218	ACKSTAT	TRSTAT	—	—	—	BCL	GCSTAT	ADD10	IWCOL	I2COV	D_A	P	S	R_W	RBF	TBF	0000	
I2C2ADD	021A	—	—	—	—	—	—	I2C2 Address Register											0000
I2C2MSK	021C	—	—	—	—	—	—	I2C2 Address Mask											0000

Legend: — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

TABLE 4-18: UART1 AND UART2 REGISTER MAP

SFR Name	Addr.	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	All Resets
U1MODE	0220	UARTEN	—	USIDL	IREN	RTSMD	—	UEN<1:0>		WAKE	LPBACK	ABAUD	URXINV	BRGH	PDSEL<1:0>		STSEL	0000
U1STA	0222	UTXISEL1	UTXINV	UTXISEL0	—	UTXBRK	UTXEN	UTXBF	TRMT	URXISEL<1:0>		ADDEN	RIDLE	PERR	FERR	OERR	URXDA	0110
U1TXREG	0224	—	—	—	—	—	—	—	UART1 Transmit Register									xxxx
U1RXREG	0226	—	—	—	—	—	—	—	UART1 Receive Register									0000
U1BRG	0228	Baud Rate Generator Prescaler																0000
U2MODE	0230	UARTEN	—	USIDL	IREN	RTSMD	—	UEN<1:0>		WAKE	LPBACK	ABAUD	URXINV	BRGH	PDSEL<1:0>		STSEL	0000
U2STA	0232	UTXISEL1	UTXINV	UTXISEL0	—	UTXBRK	UTXEN	UTXBF	TRMT	URXISEL<1:0>		ADDEN	RIDLE	PERR	FERR	OERR	URXDA	0110
U2TXREG	0234	—	—	—	—	—	—	—	UART2 Transmit Register									xxxx
U2RXREG	0236	—	—	—	—	—	—	—	UART2 Receive Register									0000
U2BRG	0238	Baud Rate Generator Prescaler																0000

Legend: x = unknown value on Reset, — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

REGISTER 6-1: RCON: RESET CONTROL REGISTER⁽¹⁾

R/W-0	R/W-0	U-0	U-0	R/W-0	U-0	R/W-0	R/W-0
TRAPR	IOPUWR	—	—	VREGSF	—	CM	VREGS
bit 15						bit 8	

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-1	R/W-1
EXTR	SWR	SWDTEN ⁽²⁾	WDTO	SLEEP	IDLE	BOR	POR
bit 7						bit 0	

Legend:

R = Readable bit

W = Writable bit

U = Unimplemented bit, read as '0'

-n = Value at POR

'1' = Bit is set

'0' = Bit is cleared

x = Bit is unknown

- bit 15 **TRAPR:** Trap Reset Flag bit
1 = A Trap Conflict Reset has occurred
0 = A Trap Conflict Reset has not occurred
- bit 14 **IOPUWR:** Illegal Opcode or Uninitialized W Access Reset Flag bit
1 = An illegal opcode detection, an illegal address mode or Uninitialized W register used as an Address Pointer caused a Reset
0 = An illegal opcode or Uninitialized W register Reset has not occurred
- bit 13-12 **Unimplemented:** Read as '0'
- bit 11 **VREGSF:** Flash Voltage Regulator Standby During Sleep bit
1 = Flash voltage regulator is active during Sleep
0 = Flash voltage regulator goes into Standby mode during Sleep
- bit 10 **Unimplemented:** Read as '0'
- bit 9 **CM:** Configuration Mismatch Flag bit
1 = A Configuration Mismatch Reset has occurred.
0 = A Configuration Mismatch Reset has not occurred
- bit 8 **VREGS:** Voltage Regulator Standby During Sleep bit
1 = Voltage regulator is active during Sleep
0 = Voltage regulator goes into Standby mode during Sleep
- bit 7 **EXTR:** External Reset ($\overline{\text{MCLR}}$) Pin bit
1 = A Master Clear (pin) Reset has occurred
0 = A Master Clear (pin) Reset has not occurred
- bit 6 **SWR:** Software RESET (Instruction) Flag bit
1 = A RESET instruction has been executed
0 = A RESET instruction has not been executed
- bit 5 **SWDTEN:** Software Enable/Disable of WDT bit⁽²⁾
1 = WDT is enabled
0 = WDT is disabled
- bit 4 **WDTO:** Watchdog Timer Time-out Flag bit
1 = WDT time-out has occurred
0 = WDT time-out has not occurred

Note 1: All of the Reset status bits can be set or cleared in software. Setting one of these bits in software does not cause a device Reset.

2: If the FWDTEN Configuration bit is '1' (unprogrammed), the WDT is always enabled, regardless of the SWDTEN bit setting.

REGISTER 8-2: DMAxREQ: DMA CHANNEL x IRQ SELECT REGISTER

R/S-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
FORCE ⁽¹⁾	—	—	—	—	—	—	—
bit 15							bit 8

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
IRQSEL7	IRQSEL6	IRQSEL5	IRQSEL4	IRQSEL3	IRQSEL2	IRQSEL1	IRQSEL0
bit 7							bit 0

Legend:	S = Settable bit
R = Readable bit	W = Writable bit
-n = Value at POR	'1' = Bit is set
	'0' = Bit is cleared
	x = Bit is unknown

- bit 15 **FORCE:** Force DMA Transfer bit⁽¹⁾
 1 = Forces a single DMA transfer (Manual mode)
 0 = Automatic DMA transfer initiation by DMA request
- bit 14-8 **Unimplemented:** Read as '0'
- bit 7-0 **IRQSEL<7:0>:** DMA Peripheral IRQ Number Select bits
 01000110 = ECAN1 – TX Data Request⁽²⁾
 00100110 = IC4 – Input Capture 4
 00100101 = IC3 – Input Capture 3
 00100010 = ECAN1 – RX Data Ready⁽²⁾
 00100001 = SPI2 Transfer Done
 00011111 = UART2TX – UART2 Transmitter
 00011110 = UART2RX – UART2 Receiver
 00011100 = TMR5 – Timer5
 00011011 = TMR4 – Timer4
 00011010 = OC4 – Output Compare 4
 00011001 = OC3 – Output Compare 3
 00001101 = ADC1 – ADC1 Convert done
 00001100 = UART1TX – UART1 Transmitter
 00001011 = UART1RX – UART1 Receiver
 00001010 = SPI1 – Transfer Done
 00001000 = TMR3 – Timer3
 00000111 = TMR2 – Timer2
 00000110 = OC2 – Output Compare 2
 00000101 = IC2 – Input Capture 2
 00000010 = OC1 – Output Compare 1
 00000001 = IC1 – Input Capture 1
 00000000 = INT0 – External Interrupt 0

- Note 1:** The FORCE bit cannot be cleared by user software. The FORCE bit is cleared by hardware when the forced DMA transfer is complete or the channel is disabled (CHEN = 0).
- 2:** This selection is available in dsPIC33EPXXXGP/MC50X devices only.

REGISTER 11-22: RPOR4: PERIPHERAL PIN SELECT OUTPUT REGISTER 4

U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
—	—	RP43R<5:0>					
bit 15							bit 8

U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
—	—	RP42R<5:0>					
bit 7							bit 0

Legend:

R = Readable bit

W = Writable bit

U = Unimplemented bit, read as '0'

-n = Value at POR

'1' = Bit is set

'0' = Bit is cleared

x = Bit is unknown

bit 15-14 **Unimplemented:** Read as '0'bit 13-8 **RP43R<5:0>**: Peripheral Output Function is Assigned to RP43 Output Pin bits
(see Table 11-3 for peripheral function numbers)bit 7-6 **Unimplemented:** Read as '0'bit 5-0 **RP42R<5:0>**: Peripheral Output Function is Assigned to RP42 Output Pin bits
(see Table 11-3 for peripheral function numbers)**REGISTER 11-23: RPOR5: PERIPHERAL PIN SELECT OUTPUT REGISTER 5**

U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
—	—	RP55R<5:0>					
bit 15							bit 8

U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
—	—	RP54R<5:0>					
bit 7							bit 0

Legend:

R = Readable bit

W = Writable bit

U = Unimplemented bit, read as '0'

-n = Value at POR

'1' = Bit is set

'0' = Bit is cleared

x = Bit is unknown

bit 15-14 **Unimplemented:** Read as '0'bit 13-8 **RP55R<5:0>**: Peripheral Output Function is Assigned to RP55 Output Pin bits
(see Table 11-3 for peripheral function numbers)bit 7-6 **Unimplemented:** Read as '0'bit 5-0 **RP54R<5:0>**: Peripheral Output Function is Assigned to RP54 Output Pin bits
(see Table 11-3 for peripheral function numbers)

12.1 Timer1 Resources

Many useful resources are provided on the main product page of the Microchip web site for the devices listed in this data sheet. This product page, which can be accessed using this link, contains the latest updates and additional information.

Note: In the event you are not able to access the product page using the link above, enter this URL in your browser:
<http://www.microchip.com/wwwproducts/Devices.aspx?dDocName=en555464>

12.1.1 KEY RESOURCES

- **“Timers”** (DS70362) in the *“dsPIC33/PIC24 Family Reference Manual”*
- Code Samples
- Application Notes
- Software Libraries
- Webinars
- All Related *“dsPIC33/PIC24 Family Reference Manual”* Sections
- Development Tools

REGISTER 14-2: ICxCON2: INPUT CAPTURE x CONTROL REGISTER 2 (CONTINUED)

bit 4-0 **SYNCSEL<4:0>**: Input Source Select for Synchronization and Trigger Operation bits⁽⁴⁾

11111 = No Sync or Trigger source for ICx
 11110 = Reserved
 11101 = Reserved
 11100 = CTMU module synchronizes or triggers ICx
 11011 = ADC1 module synchronizes or triggers ICx⁽⁵⁾
 11010 = CMP3 module synchronizes or triggers ICx⁽⁵⁾
 11001 = CMP2 module synchronizes or triggers ICx⁽⁵⁾
 11000 = CMP1 module synchronizes or triggers ICx⁽⁵⁾
 10111 = Reserved
 10110 = Reserved
 10101 = Reserved
 10100 = Reserved
 10011 = IC4 module synchronizes or triggers ICx
 10010 = IC3 module synchronizes or triggers ICx
 10001 = IC2 module synchronizes or triggers ICx
 10000 = IC1 module synchronizes or triggers ICx
 01111 = Timer5 synchronizes or triggers ICx
 01110 = Timer4 synchronizes or triggers ICx
 01101 = Timer3 synchronizes or triggers ICx **(default)**
 01100 = Timer2 synchronizes or triggers ICx
 01011 = Timer1 synchronizes or triggers ICx
 01010 = PTGOx module synchronizes or triggers ICx⁽⁶⁾
 01001 = Reserved
 01000 = Reserved
 00111 = Reserved
 00110 = Reserved
 00101 = Reserved
 00100 = OC4 module synchronizes or triggers ICx
 00011 = OC3 module synchronizes or triggers ICx
 00010 = OC2 module synchronizes or triggers ICx
 00001 = OC1 module synchronizes or triggers ICx
 00000 = No Sync or Trigger source for ICx

- Note 1:** The IC32 bit in both the Odd and Even IC must be set to enable Cascade mode.
- 2:** The input source is selected by the SYNCSEL<4:0> bits of the ICxCON2 register.
- 3:** This bit is set by the selected input source (selected by SYNCSEL<4:0> bits). It can be read, set and cleared in software.
- 4:** Do not use the ICx module as its own Sync or Trigger source.
- 5:** This option should only be selected as a trigger source and not as a synchronization source.
- 6:** Each Input Capture x (ICx) module has one PTG input source. See **Section 24.0 “Peripheral Trigger Generator (PTG) Module”** for more information.
- PTGO8 = IC1
 PTGO9 = IC2
 PTGO10 = IC3
 PTGO11 = IC4

NOTES:

24.4 Step Commands and Format

TABLE 24-1: PTG STEP COMMAND FORMAT

Step Command Byte:			
STEPx<7:0>			
CMD<3:0>		OPTION<3:0>	
bit 7	bit 4	bit 3	bit 0

bit 7-4	CMD<3:0>	Step Command	Command Description
	0000	PTGCTRL	Execute control command as described by OPTION<3:0>.
	0001	PTGADD	Add contents of PTGADJ register to target register as described by OPTION<3:0>.
		PTGCOPY	Copy contents of PTGHOLD register to target register as described by OPTION<3:0>.
	001x	PTGSTRB	Copy the value contained in CMD<0>:OPTION<3:0> to the CH0SA<4:0> bits (AD1CHS0<4:0>).
	0100	PTGWHI	Wait for a low-to-high edge input from the selected PTG trigger input as described by OPTION<3:0>.
	0101	PTGWLO	Wait for a high-to-low edge input from the selected PTG trigger input as described by OPTION<3:0>.
	0110	Reserved	Reserved.
	0111	PTGIRQ	Generate individual interrupt request as described by OPTION3<0>.
	100x	PTGTRIG	Generate individual trigger output as described by <<CMD<0>:OPTION<3:0>>.
	101x	PTGJMP	Copy the value indicated in <<CMD<0>:OPTION<3:0>> to the Queue Pointer (PTGQPTR) and jump to that Step queue.
	110x	PTGJMPC0	PTGC0 = PTGC0LIM: Increment the Queue Pointer (PTGQPTR). PTGC0 ≠ PTGC0LIM: Increment Counter 0 (PTGC0) and copy the value indicated in <<CMD<0>:OPTION<3:0>> to the Queue Pointer (PTGQPTR), and jump to that Step queue
	111x	PTGJMPC1	PTGC1 = PTGC1LIM: Increment the Queue Pointer (PTGQPTR). PTGC1 ≠ PTGC1LIM: Increment Counter 1 (PTGC1) and copy the value indicated in <<CMD<0>:OPTION<3:0>> to the Queue Pointer (PTGQPTR), and jump to that Step queue.

- Note 1:** All reserved commands or options will execute but have no effect (i.e., execute as a NOP instruction).
Note 2: Refer to Table 24-2 for the trigger output descriptions.
Note 3: This feature is only available on dsPIC33EPXXXMC20X/50X and PIC24EPXXXMC20X devices.

TABLE 28-2: INSTRUCTION SET OVERVIEW (CONTINUED)

Base Instr #	Assembly Mnemonic	Assembly Syntax	Description	# of Words	# of Cycles ⁽²⁾	Status Flags Affected
25	DAW	DAW Wn	Wn = decimal adjust Wn	1	1	C
26	DEC	DEC f	$f = f - 1$	1	1	C,DC,N,OV,Z
		DEC f, WREG	WREG = $f - 1$	1	1	C,DC,N,OV,Z
		DEC Ws, Wd	Wd = Ws - 1	1	1	C,DC,N,OV,Z
27	DEC2	DEC2 f	$f = f - 2$	1	1	C,DC,N,OV,Z
		DEC2 f, WREG	WREG = $f - 2$	1	1	C,DC,N,OV,Z
		DEC2 Ws, Wd	Wd = Ws - 2	1	1	C,DC,N,OV,Z
28	DISI	DISI #lit14	Disable Interrupts for k instruction cycles	1	1	None
29	DIV	DIV.S Wm, Wn	Signed 16/16-bit Integer Divide	1	18	N,Z,C,OV
		DIV.SD Wm, Wn	Signed 32/16-bit Integer Divide	1	18	N,Z,C,OV
		DIV.U Wm, Wn	Unsigned 16/16-bit Integer Divide	1	18	N,Z,C,OV
		DIV.UD Wm, Wn	Unsigned 32/16-bit Integer Divide	1	18	N,Z,C,OV
30	DIVF	DIVF Wm, Wn ⁽¹⁾	Signed 16/16-bit Fractional Divide	1	18	N,Z,C,OV
31	DO	DO #lit15, Expr ⁽¹⁾	Do code to PC + Expr, lit15 + 1 times	2	2	None
		DO Wn, Expr ⁽¹⁾	Do code to PC + Expr, (Wn) + 1 times	2	2	None
32	ED	ED Wm*Wm, Acc, Wx, Wy, Wxd ⁽¹⁾	Euclidean Distance (no accumulate)	1	1	OA,OB,OAB,SA,SB,SAB
33	EDAC	EDAC Wm*Wm, Acc, Wx, Wy, Wxd ⁽¹⁾	Euclidean Distance	1	1	OA,OB,OAB,SA,SB,SAB
34	EXCH	EXCH Wns, Wnd	Swap Wns with Wnd	1	1	None
35	FBCL	FBCL Ws, Wnd	Find Bit Change from Left (MSb) Side	1	1	C
36	FF1L	FF1L Ws, Wnd	Find First One from Left (MSb) Side	1	1	C
37	FF1R	FF1R Ws, Wnd	Find First One from Right (LSb) Side	1	1	C
38	GOTO	GOTO Expr	Go to address	2	4	None
		GOTO Wn	Go to indirect	1	4	None
		GOTO.L Wn	Go to indirect (long address)	1	4	None
39	INC	INC f	$f = f + 1$	1	1	C,DC,N,OV,Z
		INC f, WREG	WREG = $f + 1$	1	1	C,DC,N,OV,Z
		INC Ws, Wd	Wd = Ws + 1	1	1	C,DC,N,OV,Z
40	INC2	INC2 f	$f = f + 2$	1	1	C,DC,N,OV,Z
		INC2 f, WREG	WREG = $f + 2$	1	1	C,DC,N,OV,Z
		INC2 Ws, Wd	Wd = Ws + 2	1	1	C,DC,N,OV,Z
41	IOR	IOR f	$f = f . \text{IOR} . \text{WREG}$	1	1	N,Z
		IOR f, WREG	WREG = $f . \text{IOR} . \text{WREG}$	1	1	N,Z
		IOR #lit10, Wn	Wd = lit10 . IOR. Wd	1	1	N,Z
		IOR Wb, Ws, Wd	Wd = Wb . IOR. Ws	1	1	N,Z
		IOR Wb, #lit5, Wd	Wd = Wb . IOR. lit5	1	1	N,Z
42	LAC	LAC Wso, #Slit4, Acc	Load Accumulator	1	1	OA,OB,OAB,SA,SB,SAB
43	LNK	LNK #lit14	Link Frame Pointer	1	1	SFA
44	LSR	LSR f	$f = \text{Logical Right Shift } f$	1	1	C,N,OV,Z
		LSR f, WREG	WREG = Logical Right Shift f	1	1	C,N,OV,Z
		LSR Ws, Wd	Wd = Logical Right Shift Ws	1	1	C,N,OV,Z
		LSR Wb, Wns, Wnd	Wnd = Logical Right Shift Wb by Wns	1	1	N,Z
		LSR Wb, #lit5, Wnd	Wnd = Logical Right Shift Wb by lit5	1	1	N,Z
45	MAC	MAC Wm*Wn, Acc, Wx, Wxd, Wy, Wyd, AWB ⁽¹⁾	Multiply and Accumulate	1	1	OA,OB,OAB,SA,SB,SAB
		MAC Wm*Wm, Acc, Wx, Wxd, Wy, Wyd ⁽¹⁾	Square and Accumulate	1	1	OA,OB,OAB,SA,SB,SAB

Note 1: These instructions are available in dsPIC33EPXXXMC20X/50X and PIC24EPXXXMC20X devices only.

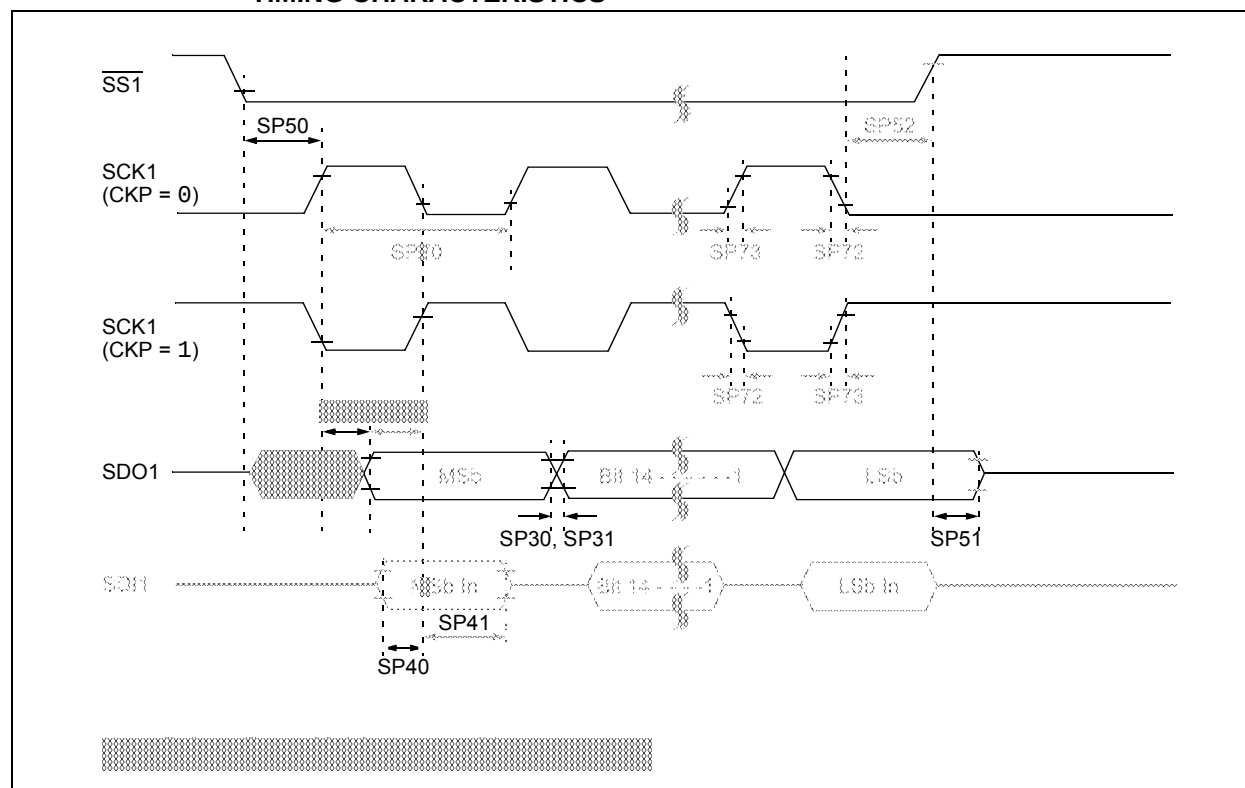
2: Read and Read-Modify-Write (e.g., bit operations and logical operations) on non-CPU SFRs incur an additional instruction cycle.

TABLE 30-22: RESET, WATCHDOG TIMER, OSCILLATOR START-UP TIMER, POWER-UP TIMER TIMING REQUIREMENTS

AC CHARACTERISTICS			Standard Operating Conditions: 3.0V to 3.6V (unless otherwise stated) Operating temperature $-40^{\circ}\text{C} \leq T_A \leq +85^{\circ}\text{C}$ for Industrial $-40^{\circ}\text{C} \leq T_A \leq +125^{\circ}\text{C}$ for Extended				
Param No.	Symbol	Characteristic ⁽¹⁾	Min.	Typ. ⁽²⁾	Max.	Units	Conditions
SY00	TPU	Power-up Period	—	400	600	μs	
SY10	TOST	Oscillator Start-up Time	—	1024 TOSC	—	—	TOSC = OSC1 period
SY12	TWDT	Watchdog Timer Time-out Period	0.81	0.98	1.22	ms	WDTPRE = 0, WDTPOST<3:0> = 0000, using LPRC tolerances indicated in F21 (see Table 30-20) at +85°C
			3.26	3.91	4.88	ms	WDTPRE = 1, WDTPOST<3:0> = 0000, using LPRC tolerances indicated in F21 (see Table 30-20) at +85°C
SY13	TIOZ	I/O High-Impedance from MCLR Low or Watchdog Timer Reset	0.68	0.72	1.2	μs	
SY20	TMCLR	MCLR Pulse Width (low)	2	—	—	μs	
SY30	TBOR	BOR Pulse Width (low)	1	—	—	μs	
SY35	TFSCM	Fail-Safe Clock Monitor Delay	—	500	900	μs	-40°C to +85°C
SY36	TVREG	Voltage Regulator Standby-to-Active mode Transition Time	—	—	30	μs	
SY37	TOSCDFRC	FRC Oscillator Start-up Delay	46	48	54	μs	
SY38	TOSCDLPRC	LPRC Oscillator Start-up Delay	—	—	70	μs	

Note 1: These parameters are characterized but not tested in manufacturing.**2:** Data in "Typical" column is at 3.3V, +25°C unless otherwise stated.

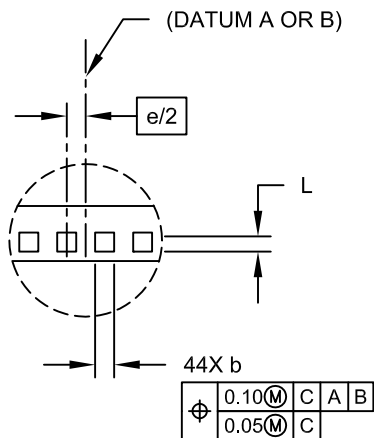
FIGURE 30-29: SPI1 SLAVE MODE (FULL-DUPLEX, CKE = 0, CKP = 0, SMP = 0)
TIMING CHARACTERISTICS



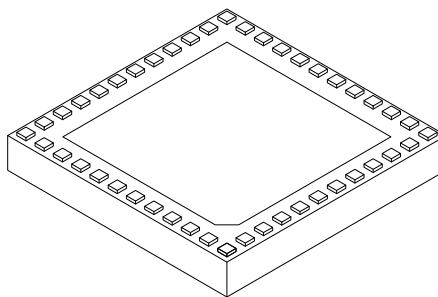
NOTES:

44-Terminal Very Thin Leadless Array Package (TL) – 6x6x0.9 mm Body With Exposed Pad [VTLA]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at <http://www.microchip.com/packaging>



DETAIL A



Dimension	Units	MILLIMETERS		
	Limits	MIN	NOM	MAX
Number of Pins	N	44		
Number of Pins per Side	ND	12		
Number of Pins per Side	NE	10		
Pitch	e	0.50 BSC		
Overall Height	A	0.80	0.90	1.00
Standoff	A1	0.025	-	0.075
Overall Width	E	6.00 BSC		
Exposed Pad Width	E2	4.40	4.55	4.70
Overall Length	D	6.00 BSC		
Exposed Pad Length	D2	4.40	4.55	4.70
Contact Width	b	0.20	0.25	0.30
Contact Length	L	0.20	0.25	0.30
Contact-to-Exposed Pad	K	0.20	-	-

Notes:

- Pin 1 visual index feature may vary, but must be located within the hatched area.
- Package is saw singulated.
- Dimensioning and tolerancing per ASME Y14.5M.
 - BSC: Basic Dimension. Theoretically exact value shown without tolerances.
 - REF: Reference Dimension, usually without tolerance, for information purposes only.

Microchip Technology Drawing C04-157C Sheet 2 of 2

PMD (PIC24EPXXXMC20X Devices).....	94	CMxMSKCON (Comparator x Mask Gating Control).....	368
PORTA (PIC24EPXXXGP/MC202, dsPIC33EPXXXGP/MC202/502 Devices)	104	CMxMSKSR (Comparator x Mask Source Select Control).....	366
PORTA (PIC24EPXXXGP/MC203, dsPIC33EPXXXGP/MC203/503 Devices)	103	CORCON (Core Control).....	42, 133
PORTA (PIC24EPXXXGP/MC204, dsPIC33EPXXXGP/MC204/504 Devices)	102	CRCCON1 (CRC Control 1).....	375
PORTA (PIC24EPXXXGP/MC206, dsPIC33EPXXXGP/MC206/506 Devices)	99	CRCCON2 (CRC Control 2).....	376
PORTB (PIC24EPXXXGP/MC202, dsPIC33EPXXXGP/MC202/502 Devices)	104	CRCXORH (CRC XOR Polynomial High)	377
PORTB (PIC24EPXXXGP/MC203, dsPIC33EPXXXGP/MC203/503 Devices)	103	CRCXORL (CRC XOR Polynomial Low).....	377
PORTB (PIC24EPXXXGP/MC204, dsPIC33EPXXXGP/MC204/504 Devices)	102	CTMUCON1 (CTMU Control 1).....	317
PORTB (PIC24EPXXXGP/MC206, dsPIC33EPXXXGP/MC206/506 Devices)	99	CTMUCON2 (CTMU Control 2).....	318
PORTC (PIC24EPXXXGP/MC203, dsPIC33EPXXXGP/MC203/503 Devices)	103	CTMUICON (CTMU Current Control).....	319
PORTC (PIC24EPXXXGP/MC204, dsPIC33EPXXXGP/MC204/504 Devices)	102	CVRCON (Comparator Voltage Reference Control).....	371
PORTC (PIC24EPXXXGP/MC206, dsPIC33EPXXXGP/MC206/506 Devices)	99	CxBUFPNT1 (ECANx Filter 0-3 Buffer Pointer 1)	300
PORTD (PIC24EPXXXGP/MC206, dsPIC33EPXXXGP/MC206/506 Devices)	100	CxBUFPNT2 (ECANx Filter 4-7 Buffer Pointer 2)	301
PORTE (PIC24EPXXXGP/MC206, dsPIC33EPXXXGP/MC206/506 Devices)	100	CxBUFPNT3 (ECANx Filter 8-11 Buffer Pointer 3)	301
PORTF (PIC24EPXXXGP/MC206, dsPIC33EPXXXGP/MC206/506 Devices)	100	CxBUFPNT4 (ECANx Filter 12-15 Buffer Pointer 4)	302
PORTG (PIC24EPXXXGP/MC206 and dsPIC33EPXXXGP/MC206/506 Devices)	101	CxCFG1 (ECANx Baud Rate Configuration 1).....	298
PTG.....	78	CxCFG2 (ECANx Baud Rate Configuration 2).....	299
PWM (dsPIC33EPXXXMC20X/50X, PIC24EPXXXMC20X Devices).....	79	CxCTRL1 (ECANx Control 1).....	290
PWM Generator 1 (dsPIC33EPXXXMC20X/50X, PIC24EPXXXMC20X Devices).....	79	CxCTRL2 (ECANx Control 2).....	291
PWM Generator 2 (dsPIC33EPXXXMC20X/50X, PIC24EPXXXMC20X Devices).....	80	CxEC (ECANx Transmit/Receive Error Count)	298
PWM Generator 3 (dsPIC33EPXXXMC20X/50X, PIC24EPXXXMC20X Devices).....	80	CxFCTRL (ECANx FIFO Control).....	293
QE11 (dsPIC33EPXXXMC20X/50X, PIC24EPXXXMC20X Devices).....	81	CxFEN1 (ECANx Acceptance Filter Enable 1).....	300
Reference Clock	93	CxFIFO (ECANx FIFO Status)	294
SPI1 and SPI2	83	CxFMSKSEL1 (ECANx Filter 7-0 Mask Selection 1).....	304
System Control	93	CxFMSKSEL2 (ECANx Filter 15-8 Mask Selection 2).....	305
Time1 through Time5.....	75	CxINTE (ECANx Interrupt Enable)	297
UART1 and UART2	82	CxINTF (ECANx Interrupt Flag).....	295
Registers		CxRXFnEID (ECANx Acceptance Filter n Extended Identifier)	304
AD1CHS0 (ADC1 Input Channel 0 Select)	333	CxRXFnSID (ECANx Acceptance Filter n Standard Identifier)	303
AD1CHS123 (ADC1 Input Channel 1, 2, 3 Select)	331	CxRXFUL1 (ECANx Receive Buffer Full 1).....	307
AD1CON1 (ADC1 Control 1)	325	CxRXFUL2 (ECANx Receive Buffer Full 2).....	307
AD1CON2 (ADC1 Control 2)	327	CxRXMnEID (ECANx Acceptance Filter Mask n Extended Identifier)	306
AD1CON3 (ADC1 Control 3)	329	CxRXMnSID (ECANx Acceptance Filter Mask n Standard Identifier)	306
AD1CON4 (ADC1 Control 4)	330	CxRXOVF1 (ECANx Receive Buffer Overflow 1).....	308
AD1CSSH (ADC1 Input Scan Select High)	335	CxRXOVF2 (ECANx Receive Buffer Overflow 2).....	308
AD1CSSL (ADC1 Input Scan Select Low).....	336	CxTRMnCON (ECANx TX/RX Buffer mn Control)	309
ALTDTRx (PWMx Alternate Dead-Time)	238	CxVEC (ECANx Interrupt Code).....	292
AUXCONx (PWMx Auxiliary Control).....	247	DEVID (Device ID).....	383
CHOP (PWMx Chop Clock Generator).....	234	DEVREV (Device Revision).....	383
CLKDIV (Clock Divisor).....	158	DMALCA (DMA Last Channel Active Status)	150
CM4CON (Comparator 4 Control)	364	DMAPPS (DMA Ping-Pong Status)	151
CMSTAT (Op Amp/Comparator Status)	360	DMAPOW (DMA Peripheral Write Collision Status).....	148
CMxCON (Comparator x Control, x = 1,2,3).....	362	DMARQC (DMA Request Collision Status).....	149
CMxFLTR (Comparator x Filter Control).....	370	DMAxCNT (DMA Channel x Transfer Count).....	146
		DMAxCON (DMA Channel x Control).....	142
		DMAxPAD (DMA Channel x Peripheral Address).....	146
		DMAxREQ (DMA Channel x IRQ Select).....	143