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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "<u>Embedded -</u> <u>Microcontrollers</u>"

Details

Product Status	Active
Core Processor	PIC
Core Size	16-Bit
Speed	70 MIPs
Connectivity	I ² C, IrDA, LINbus, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, DMA, POR, PWM, WDT
Number of I/O	35
Program Memory Size	32KB (10.7K x 24)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	2K x 16
Voltage - Supply (Vcc/Vdd)	3V ~ 3.6V
Data Converters	A/D 9x10b/12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	44-VFTLA Exposed Pad
Supplier Device Package	44-VTLA (6x6)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/pic24ep32gp204-i-tl

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TABLE 2: dsPIC33EPXXXMC20X/50X and PIC24EPXXXMC20X MOTOR CONTROL FAMILIES

		<u>~</u>				Re	mappa	ble P	eriphe	erals											
Device	Page Erase Size (Instructions)	Program Flash Memory (Kbyte	RAM (Kbytes)	16-Bit/32-Bit Timers	Input Capture	Output Compare	Motor Control PWM ⁽⁴⁾ (Channels)	Quadrature Encoder Interface	UART	SPI ⁽²⁾	ECAN™ Technology	External Interrupts ⁽³⁾	I²C™	CRC Generator	10-Bit/12-Bit ADC (Channels)	Op Amps/Comparators	СТМИ	PTG	l/O Pins	Pins	Packages
PIC24EP32MC202	512	32	4																		
PIC24EP64MC202	1024	64	8																		SPDIP,
PIC24EP128MC202	1024	128	16	5	4	4	6	1	2	2	_	3	2	1	6	2/3 ⁽¹⁾	Yes	Yes	21	28	SOIC,
PIC24EP256MC202	1024	256	32																		QFN-S
PIC24EP512MC202	1024	512	48																		
PIC24EP32MC203	512	32	4	-			_	4	0	0		0	0	4	•	2/4	V	Vee	05	20	
PIC24EP64MC203	1024	64	8	5	4	4	ю	1	2	2	_	3	2	1	8	3/4	res	res	25	30	VILA
PIC24EP32MC204	512	32	4																		
PIC24EP64MC204	1024	64	8																		VTLA ⁽⁵⁾ ,
PIC24EP128MC204	1024	128	16	5	4	4	6	1	2	2	_	3	2	1	9	3/4	Yes	Yes	35	44/	TQFP,
PIC24EP256MC204	1024	256	32																	40	UQFN,
PIC24EP512MC204	1024	512	48																		
PIC24EP64MC206	1024	64	8																		
PIC24EP128MC206	1024	128	16	_					-			•									TQFP.
PIC24EP256MC206	1024	256	32	5	4	4	6	1	2	2	_	3	2		10	3/4	res	res	53	64	QFN
PIC24EP512MC206	1024	512	48																		
dsPIC33EP32MC202	512	32	4																		
dsPIC33EP64MC202	1024	64	8																		SPDIP,
dsPIC33EP128MC202	1024	128	16	5	4	4	6	1	2	2	_	3	2	1	6	2/3(1)	Yes	Yes	21	28	SOIC,
dsPIC33EP256MC202	1024	256	32																		QFN-S
dsPIC33EP512MC202	1024	512	48																		
dsPIC33EP32MC203	512	32	4	_		_			-	_		-	-		-						
dsPIC33EP64MC203	1024	64	8	5	4	4	6	1	2	2	—	3	2	1	8	3/4	Yes	Yes	25	36	VTLA
dsPIC33EP32MC204	512	32	4																		
dsPIC33EP64MC204	1024	64	8																		VTLA ⁽⁵⁾ ,
dsPIC33EP128MC204	1024	128	16	5	4	4	6	1	2	2	_	3	2	1	9	3/4	Yes	Yes	35	44/	TQFP,
dsPIC33EP256MC204	1024	256	32																	40	UQFN,
dsPIC33EP512MC204	1024	512	48																		
dsPIC33EP64MC206	1024	64	8																		
dsPIC33EP128MC206	1024	128	16	_					-			-	-								TOFP
dsPIC33EP256MC206	1024	256	32	5	4	4	6	1	2	2	—	3	2	1	16	3/4	Yes	Yes	53	64	QFN
dsPIC33EP512MC206	1024	512	48																		
dsPIC33EP32MC502	512	32	4																		
dsPIC33EP64MC502	1024	64	8																		SPDIP,
dsPIC33EP128MC502	1024	128	16	5	4	4	6	1	2	2	1	3	2	1	6	2/3(1)	Yes	Yes	21	28	SOIC,
dsPIC33EP256MC502	1024	256	32																		QFN-S
dsPIC33EP512MC502	1024	512	48																		_
dsPIC33EP32MC503	512	32	4	_			6		_	6			-		_			~	a-		
dsPIC33EP64MC503	1024	64	8	5	4	4	6	1	2	2	1	3	2	1	8	3/4	res	res	25	36	VILA

Note 1: On 28-pin devices, Comparator 4 does not have external connections. Refer to Section 25.0 "Op Amp/Comparator Module" for details. 2: Only SPI2 is remappable.

3: INTO is not remappable.

4: Only the PWM Faults are remappable.

5: The SSOP and VTLA packages are not available for devices with 512 Kbytes of memory.

Pin Diagrams (Continued)



2.7 Oscillator Value Conditions on Device Start-up

If the PLL of the target device is enabled and configured for the device start-up oscillator, the maximum oscillator source frequency must be limited to 3 MHz < F_{IN} < 5.5 MHz to comply with device PLL start-up conditions. This means that if the external oscillator frequency is outside this range, the application must start-up in the FRC mode first. The default PLL settings after a POR with an oscillator frequency outside this range will violate the device operating speed.

Once the device powers up, the application firmware can initialize the PLL SFRs, CLKDIV and PLLFBD, to a suitable value, and then perform a clock switch to the Oscillator + PLL clock source. Note that clock switching must be enabled in the device Configuration Word.

2.8 Unused I/Os

Unused I/O pins should be configured as outputs and driven to a logic low state.

Alternatively, connect a 1k to 10k resistor between Vss and unused pins, and drive the output to logic low.

2.9 Application Examples

- · Induction heating
- Uninterruptable Power Supplies (UPS)
- DC/AC inverters
- · Compressor motor control
- · Washing machine 3-phase motor control
- BLDC motor control
- · Automotive HVAC, cooling fans, fuel pumps
- Stepper motor control
- · Audio and fluid sensor monitoring
- · Camera lens focus and stability control
- Speech (playback, hands-free kits, answering machines, VoIP)
- Consumer audio
- Industrial and building control (security systems and access control)
- · Barcode reading
- Networking: LAN switches, gateways
- Data storage device management
- · Smart cards and smart card readers

Examples of typical application connections are shown in Figure 2-4 through Figure 2-8.

FIGURE 2-4: BOOST CONVERTER IMPLEMENTATION



TABLE 4-27: PERIPHERAL PIN SELECT OUTPUT REGISTER MAP FOR dsPIC33EPXXXGP/MC204/504 AND PIC24EPXXXGP/MC204 DEVICES ONLY DEVICES ONLY

File Name	Addr.	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	All Resets	
RPOR0	0680				RP35R<5:0>					_	_	RP20R<5:0>							
RPOR1	0682	—	—		RP37R<5:0>					—			RP36R<5:0>						
RPOR2	0684	—	—		RP39R<5:0>					_	_	RP38R<5:0>						0000	
RPOR3	0686	_	_			RP41	R<5:0>			—	_	RP40R<5:0>						0000	
RPOR4	0688	_	_			RP43	R<5:0>			—	_	RP42R<5:0>						0000	
RPOR5	068A	_	_		RP55R<5:0>					—	_			RP54	R<5:0>			0000	
RPOR6	068C	_	_			RP57			_	—			RP56	R<5:0>			0000		

Legend: — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

TABLE 4-28: PERIPHERAL PIN SELECT OUTPUT REGISTER MAP FOR dsPIC33EPXXXGP/MC206/506 AND PIC24EPXXXGP/MC206 DEVICES ONLY DEVICES ONLY

File Name	Addr.	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	All Resets
RPOR0	0680	—	—			RP35	R<5:0>			_	_			RP20I	R<5:0>			0000
RPOR1	0682	_	_		RP37R<5:0>					_	_		RP36R<5:0>					
RPOR2	0684	_	_		RP39R<5:0>				—	—		RP38R<5:0>						
RPOR3	0686	_	_			RP41	R<5:0>			—	—			RP40	R<5:0>			0000
RPOR4	0688	_	_			RP43	R<5:0>			—	—			RP42I	R<5:0>			0000
RPOR5	068A	_	_			RP55I	R<5:0>			—	—			RP54I	R<5:0>			0000
RPOR6	068C	_	_			RP57I	R<5:0>			—	—			RP56I	R<5:0>			0000
RPOR7	068E	_	_			RP97	R<5:0>			—	—	_	_	_	_	_	_	0000
RPOR8	0690	_	_			RP118	R<5:0>			—	—	_	_	_	_	_	_	0000
RPOR9	0692	_	_	_								0000						

Legend: — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

				(,			
R/SO-0 ⁽¹	⁾ R/W-0 ⁽¹⁾	R/W-0 ⁽¹⁾	R/W-0	U-0	U-0	U-0	U-0
WR	WREN	WRERR	NVMSIDL ⁽²⁾			—	—
bit 15							bit 8
U-0	U-0	U-0	U-0	R/W-0 ⁽¹⁾	R/W-0 ⁽¹⁾	R/W-0 ⁽¹⁾	R/W-0 ⁽¹⁾
	—	—		NVMOP3 ^(3,4)	NVMOP2 ^(3,4)	NVMOP1 ^(3,4)	NVMOP0 ^(3,4)
bit 7							bit 0
						_	
Legend:		SO = Settab	le Only bit				
R = Reada	ble bit	W = Writable	e bit	U = Unimplem	ented bit, read	as '0'	
-n = Value	at POR	'1' = Bit is se	t	'0' = Bit is clea	ired	x = Bit is unkn	iown
bit 15	WR: Write Co 1 = Initiates a cleared by 0 = Program	ntrol bit ⁽¹⁾ a Flash memo y hardware o or erase oper	ory program or nce the operati ation is comple	erase operation on is complete ate and inactive	on; the operatio	n is self-timed	and the bit is
bit 14	WREN: Write 1 = Enables F 0 = Inhibits Fl	Enable bit ⁽¹⁾ ⁻ lash program ash program/	n/erase operati ⁄erase operatio	ons			
bit 13	WRERR: Writ 1 = An improp on any se 0 = The progr	e Sequence E per program of t attempt of th ram or erase	Error Flag bit ⁽¹⁾ rerase sequence e WR bit) operation comp	ce attempt or ter	mination has oc	curred (bit is se	t automatically
bit 12	NVMSIDL: N\ 1 = Flash volt 0 = Flash volt	/M Stop in Idl age regulator age regulator	e Control bit ⁽²⁾ goes into Star is active durin	ndby mode duri g Idle mode	ng Idle mode		
bit 11-4	Unimplement	ted: Read as	'0'	-			
bit 3-0	NVMOP<3:0> 1111 = Reser 1110 = Reser 1101 = Reser 1000 = Reser 1011 = Reser 0011 = Memo 0010 = Reser 0001 = Memo 0000 = Reser	: NVM Opera ved ved ved ved ved ved ory page erase ved ory double-wo ved	tion Select bits e operation rd program ope	5 ^(1,3,4) eration ⁽⁵⁾			
Note 1: 2: 3: 4: 5:	These bits can only If this bit is set, the (TVREG) before Fla All other combination Execution of the PV Two adjacent word	/ be reset on a re will be mini sh memory be ons of NVMO wrsav instruc s on a 4-word	a POR. mal power sav ecomes operat P<3:0> are uni tion is ignored I boundary are	rings (IIDLE) and ional. implemented. while any of the programmed d	d upon exiting lo e NVM operatio uring execution	the mode, there ns are in progra	is a delay ess. on.

REGISTER 5-1: NVMCON: NONVOLATILE MEMORY (NVM) CONTROL REGISTER

U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
—	—	—	_	—	—	—	—
bit 15				·	-		bit 8
U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
				SS2R<6:0>			
bit 7	<u>.</u>						bit 0
Logondi							

REGISTER 11-13: RPINR23: PERIPHERAL PIN SELECT INPUT REGISTER 23

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read	l as '0'
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15-7	Unimplemented: Read as '0'
bit 6-0	SS2R<6:0>: Assign SPI2 Slave Select (SS2) to the Corresponding RPn Pin bits (see Table 11-2 for input pin selection numbers)
	1111001 = Input tied to RPI121
	•
	0000001 = Input tied to CMP1 0000000 = Input tied to Vss

REGISTER 11-14: RPINR26: PERIPHERAL PIN SELECT INPUT REGISTER 26 (dsPIC33EPXXXGP/MC50X DEVICES ONLY)

U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
—	—	—	—	—	—	—	—
bit 15							bit 8
U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
—				C1RXR<6:0>	>		
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read	as '0'
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15-7	Unimplemented: Read as '0'
bit 6-0	C1RXR<6:0>: Assign CAN1 RX Input (CRX1) to the Corresponding RPn Pin bits (see Table 11-2 for input pin selection numbers)
	1111001 = Input tied to RPI121
	•
	0000001 = Input tied to CMP1 0000000 = Input tied to Vss

U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
_	CLSRC4	CLSRC3	CLSRC2	CLSRC1	CLSRC0	CLPOL ⁽²⁾	CLMOD
bit 15			•			•	bit 8
R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-0	R/W-0	R/W-0
FLTSRC4	FLTSRC3	FLTSRC2	FLTSRC1	FLTSRC0	FLTPOL ⁽²⁾	FLTMOD1	FLTMOD0
bit 7							bit 0
Legend:							
R = Readable	bit	W = Writable	bit	U = Unimple	mented bit, read	l as '0'	
-n = Value at I	POR	'1' = Bit is set		'0' = Bit is cle	eared	x = Bit is unkr	nown
bit 15	Unimplemen	ted: Read as '	0'				
bit 14-10	CLSRC<4:0>	Current-Limit	Control Signa	al Source Sele	ct for PWM Ger	erator # bits	
	11111 = Fau	lt 32					
	11110 = Res	served					
	•						
	•	anyod					
	01100 = Res 01011 = Con	nparator 4					
	01010 = Op	Amp/Comparat	or 3				
	01001 = Op	Amp/Comparat	or 2				
	01000 = Op	Amp/Comparat	or 1				
	00111 = Res	erved					
	00101 = Res	erved					
	00100 = Res	erved					
	00011 = Fau	lt 4					
	00010 = Fau	lt 3 lt 2					
	00000 = Fau	It 1 (default)					
bit 9	CLPOL: Curr	ent-Limit Polar	ity for PWM G	enerator # bit	2)		
	1 = The selec	cted current-lim	it source is ac	tive-low			
	0 = The selec	cted current-lim	it source is ac	tive-high			
bit 8	CLMOD: Cur	rent-Limit Mode	e Enable for P	WM Generato	r # bit		
	1 = Current-L	imit mode is er	nabled				
	0 = Current-L	imit mode is di	sabled				
Note 1: If the	he PWMLOCK	Configuration b	it (FOSCSEL·	<6>) is a '1', th	ne IOCONx regi	ster can only be	e written after
the	unlock sequen	ice has been ex	cecuted.				

REGISTER 16-15: FCLCONx: PWMx FAULT CURRENT-LIMIT CONTROL REGISTER⁽¹⁾

2: These bits should be changed only when PTEN = 0. Changing the clock selection during operation will yield unpredictable results.

REGISTER 17-2: QEI1IOC: QEI1 I/O CONTROL REGISTER (CONTINUED)

- bit 2 INDEX: Status of INDXx Input Pin After Polarity Control
 - 1 = Pin is at logic '1'
 - 0 = Pin is at logic '0'
- bit 1 QEB: Status of QEBx Input Pin After Polarity Control And SWPAB Pin Swapping 1 = Pin is at logic '1' 0 = Pin is at logic '0'
- bit 0 **QEA:** Status of QEAx Input Pin After Polarity Control And SWPAB Pin Swapping 1 = Pin is at logic '1'
 - 0 = Pin is at logic '0'

U-0	U-0	U-0	R-0	R-0	R-0	R-0	R-0
—	_	_	FILHIT4	FILHIT3	FILHIT2	FILHIT1	FILHIT0
bit 15							bit 8
U-0	R-1	R-0	R-0	R-0	R-0	R-0	R-0
	ICODE6	ICODE5	ICODE4	ICODE3	ICODE2	ICODE1	ICODE0
bit 7			1	1	I	1	bit 0
Legend:							
R = Readable	bit	W = Writable	bit	U = Unimpler	mented bit, read	l as '0'	
-n = Value at I	POR	'1' = Bit is set		'0' = Bit is cle	ared	x = Bit is unkn	own
bit 15-13	Unimplemen	ted: Read as '	0'				
bit 12-8	FILHIT<4:0>:	Filter Hit Num	ber bits				
	10000-1111	1 = Reserved					
	01111 = Filte	r 15					
	•						
	•						
	•						
	00001 = Filte 00000 = Filte	r 1 r 0					
bit 7	Unimplemen	ted: Read as '	0'				
bit 6-0	ICODE<6:0>:	: Interrupt Flag	Code bits				
	1000101-11	11111 = Rese	rved				
	1000100 = F	IFO almost full	interrupt				
	1000011 = R 1000010 = W	ake-up interru	pt				
	1000001 = E	rror interrupt					
	1000000 = N	o interrupt					
	•						
	•						
	•						
	0010000-01	11111 = Kese B15 buffer inte	rved				
	•		nupt				
	•						
	•						
	0001001 = R	B9 buffer inter	rupt				
	0001000 = R	B8 buffer inter	rupt				
	0000111 = T	RB7 buffer inte	rrupt				
	0000110 = 1	RB5 buffer inte	errupt				
	0000100 = T	RB4 buffer inte	errupt				
	0000011 = T	RB3 buffer inte	rrupt				
	0000010 = T	RB2 buffer inte	rrupt				
	0000001 = T	RB1 buffer inte	errupt				
			πupι				

REGISTER 21-3: CxVEC: ECANx INTERRUPT CODE REGISTER

REGISTER 21-13: CxBUFPNT2: ECANx FILTER 4-7 BUFFER POINTER REGISTER 2

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	
	F7BP	<3:0>			F6BI	><3:0>		
bit 15							bit 8	
R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	
	F5BP	<3:0>		F4BP<3:0>				
bit 7							bit 0	
Legend:								
R = Readable	bit	W = Writable	bit	U = Unimplemented bit, read as '0'				
-n = Value at POR '1' = Bit is set			'0' = Bit is cleared x = Bit is unknown					
bit 15-12	F7BP<3:0>: 1111 = Filter	RX Buffer Masl	k for Filter 7 b	its ffer				

1110 = Filter hits received in RX Buffer 14
•
•
0001 = Filter hits received in RX Buffer 1 0000 = Filter hits received in RX Buffer 0
F6BP<3:0>: RX Buffer Mask for Filter 6 bits (same values as bits<15:12>)
F5BP<3:0>: RX Buffer Mask for Filter 5 bits (same values as bits<15:12>)
F4BP<3:0>: RX Buffer Mask for Filter 4 bits (same values as bits<15:12>)

REGISTER 21-14: CxBUFPNT3: ECANx FILTER 8-11 BUFFER POINTER REGISTER 3

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0		
F11BP<3:0>					F10B	P<3:0>			
bit 15							bit 8		
R/W_0	R/M-0	R/M/-0	R/M-0	R/\\/_0	R/W/-0	R/M/-0	R/\/_0		
10,00-0	F9BP	>	1000-0	10,00-0	F8B	P<3:0>	1477-0		
bit 7							bit 0		
Legend:									
R = Readable	e bit	W = Writable	bit	U = Unimpler	nented bit, rea	d as '0'			
-n = Value at	POR	'1' = Bit is set		'0' = Bit is cleared		x = Bit is unknown			
bit 15-12	F11BP<3:0> 1111 = Filter 1110 = Filter • • • 0001 = Filter 0000 = Filter	RX Buffer Mar hits received ir hits received ir hits received ir hits received ir	sk for Filter 1 n RX FIFO bu n RX Buffer 1 n RX Buffer 1 n RX Buffer 0	1 bits iffer 4					
bit 11-8 bit 7-4	F10BP<3:0> F9BP<3:0>:	RX Buffer Ma	sk for Filter 1 k for Filter 9 k	0 bits (same val bits (same value	lues as bits<15 s as bits<15:1	5:12>) 2>)			
bit 3-0	F8BP<3:0>:	F8BP<3:0>: RX Buffer Mask for Filter 8 bits (same values as bits<15:12>)							

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REGISTER 21-20:	CxRXMnSID: ECANx ACCEPTANCE FILTER MASK n STANDARD IDENTIFIER
	REGISTER (n = 0-2)

R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	
SID10	SID9	SID8	SID7	SID6	SID5	SID4	SID3	
bit 15	•		•	•			bit 8	
R/W-x	R/W-x	R/W-x	U-0	R/W-x	U-0	R/W-x	R/W-x	
SID2	SID1	SID0	_	MIDE	—	EID17	EID16	
bit 7							bit 0	
Legend:								
R = Readable bit W = Writable bit			U = Unimplemented bit, read as '0'					
-n = Value at F	POR	'1' = Bit is set		'0' = Bit is cleared x = Bit is unknown				
bit 15-5	SID<10:0>: S	Standard Identif	ier bits					
	1 = Includes I	bit, SIDx, in filte	er comparisor	1				
		s a don't care ir	n filter compa	rison				
bit 4	Unimplemen	ted: Read as '	0'					
bit 3	MIDE: Identif	ier Receive Mo	de bit					
	1 = Matches	only message ty	/pes (standar	d or extended a	ddress) that corre	espond to EXID	E bit in the filter	
	0 = Matches	either standard	or extended a	address messag	ge if filters match	(i.e., if (Filter SI	D) = (Message	
	SID) or if	(Filter SID/EID)		SID/EID))				
bit 2	Unimplemen	ted: Read as '	0'					
bit 1-0	EID<17:16>:	Extended Iden	tifier bits					
	1 = Includes	bit, EIDx, in filt	er compariso	n				
	0 = EIDx bit	is a don't care i	n filter compa	arison				

REGISTER 21-21: CxRXMnEID: ECANx ACCEPTANCE FILTER MASK n EXTENDED IDENTIFIER REGISTER (n = 0-2)

R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x
EID15	EID14	EID13	EID12	EID11	EID11 EID10		EID8
bit 15							bit 8
R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x
EID7	EID6	EID5	EID4	EID3	EID2	EID1	EID0
bit 7	·				•		bit 0
Legend:							
R = Readable bit W = Writable bit			bit	U = Unimpler	mented bit, read	d as '0'	

R = Readable bit	W = Writable bit	U = Unimplemented bit, read	as '0'
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15-0 EID<15:0>: Extended Identifier bits

1 = Includes bit, EIDx, in filter comparison

0 = EIDx bit is a don't care in filter comparison

REGISTER 23-1: AD1CON1: ADC1 CONTROL REGISTER 1 (CONTINUED)

bit 7-5	SSRC<2:0>: Sample Trigger Source Select bits
	If SSRCG = 1: 111 = Reserved 110 = PTGO15 primary trigger compare ends sampling and starts conversion ⁽¹⁾ 101 = PTGO14 primary trigger compare ends sampling and starts conversion ⁽¹⁾ 100 = PTGO13 primary trigger compare ends sampling and starts conversion ⁽¹⁾ 011 = PTGO12 primary trigger compare ends sampling and starts conversion ⁽¹⁾ 010 = PWM Generator 3 primary trigger compare ends sampling and starts conversion ⁽²⁾ 001 = PWM Generator 2 primary trigger compare ends sampling and starts conversion ⁽²⁾ 000 = PWM Generator 1 primary trigger compare ends sampling and starts conversion ⁽²⁾
	If SSRCG = 0: 111 = Internal counter ends sampling and starts conversion (auto-convert) 110 = CTMU ends sampling and starts conversion 101 = Reserved
	 101 - Reserved 100 = Timer5 compare ends sampling and starts conversion 011 = PWM primary Special Event Trigger ends sampling and starts conversion 010 = Timer3 compare ends sampling and starts conversion 001 = Active transition on the INT0 pin ends sampling and starts conversion 000 = Clearing the Sample bit (SAMP) ends sampling and starts conversion (Manual mode)
bit 4	SSRCG: Sample Trigger Source Group bit
	See SSRC<2:0> for details.
bit 3	SIMSAM: Simultaneous Sample Select bit (only applicable when CHPS<1:0> = 01 or 1x) In 12-bit mode (AD21B = 1), SIMSAM is Unimplemented and is Read as '0': 1 = Samples CH0, CH1, CH2, CH3 simultaneously (when CHPS<1:0> = 1x); or samples CH0 and CH1 simultaneously (when CHPS<1:0> = 01) 0 = Samples multiple channels individually in sequence
bit 2	ASAM: ADC1 Sample Auto-Start bit
	 1 = Sampling begins immediately after the last conversion; SAMP bit is auto-set 0 = Sampling begins when the SAMP bit is set
bit 1	SAMP: ADC1 Sample Enable bit
	 1 = ADC Sample-and-Hold amplifiers are sampling 0 = ADC Sample-and-Hold amplifiers are holding If ASAM = 0, software can write '1' to begin sampling. Automatically set by hardware if ASAM = 1. If SSRC<2:0> = 000, software can write '0' to end sampling and start conversion. If SSRC<2:0> ≠ 000, automatically cleared by hardware to end sampling and start conversion.
bit 0	DONE: ADC1 Conversion Status bit ⁽³⁾
	 1 = ADC conversion cycle has completed 0 = ADC conversion has not started or is in progress Automatically set by hardware when the ADC conversion is complete. Software can write '0' to clear the DONE status bit (software is not allowed to write '1'). Clearing this bit does NOT affect any operation in progress. Automatically cleared by hardware at the start of a new conversion.
Note 1:	See Section 24.0 "Peripheral Trigger Generator (PTG) Module" for information on this selection.

- 2: This setting is available in dsPIC33EPXXXMC20X/50X and PIC24EPXXXMC20X devices only.
- **3:** Do not clear the DONE bit in software if Auto-Sample is enabled (ASAM = 1).

U-0	U-0	U-0	U-0	U-0	U-0	U-0	R/W-0				
			_	—	—		ADDMAEN				
bit 15							bit 8				
U-0	U-0	U-0	U-0	U-0	R/W-0	R/W-0	R/W-0				
—	—	—	—	—	DMABL2	DMABL1	DMABL0				
bit 7							bit 0				
Legend:											
R = Readable	e bit	W = Writable b	pit	U = Unimple	mented bit, read	d as '0'					
-n = Value at	POR	'1' = Bit is set		'0' = Bit is cleared		x = Bit is unknown					
L											
bit 15-9	Unimplemen	ted: Read as 'o)'								
bit 8	ADDMAEN: /	ADC1 DMA Ena	able bit								
	1 = Conversio	on results are st	ored in the Al	DC1BUF0 regi	ster for transfer	to RAM using	DMA				
	0 = Conversio	on results are st	ored in ADC1	BUF0 through	ADC1BUFF reg	gisters; DMA w	vill not be used				
bit 7-3	Unimplemen	ted: Read as '0)'								
bit 2-0	DMABL<2:0>	Selects Number Selects Number	per of DMA Bu	uffer Locations	per Analog Inp	ut bits					
	111 = Allocat	es 128 words o	f buffer to eac	h analog input	t						
	110 = Allocat	es 64 words of	buffer to each	analog input							
	101 = Allocates 32 words of buffer to each analog input										
	100 = Allocat	es 16 words of	buffer to each	analog input							
		es 8 words of b	uffer to each a	analog input							
		es 2 words of h	uffer to each :	analog input							
	000 = Allocat	es 1 word of bu	ffer to each a	nalog input							
		000 – Allocates I word of buller to each allolog liput									

REGISTER 23-4: AD1CON4: ADC1 CONTROL REGISTER 4

NOTES:

DC CHARACTERISTICS		$\begin{array}{l} \mbox{Standard Operating Conditions: 3.0V to 3.6V} \\ \mbox{(unless otherwise stated)} \\ \mbox{Operating temperature} & -40^{\circ}C \leq TA \leq +85^{\circ}C \mbox{ for Industrial} \\ & -40^{\circ}C \leq TA \leq +125^{\circ}C \mbox{ for Extended} \end{array}$						
Param No.	Symbol	Characteristic	Min. Typ. Max. Units Conditions					
	lı∟	Input Leakage Current ^(1,2)						
DI50		I/O Pins 5V Tolerant ⁽³⁾	-1	—	+1	μA	$Vss \le VPIN \le VDD$, Pin at high-impedance	
DI51		I/O Pins Not 5V Tolerant ⁽³⁾	-1	_	+1	μA	$\label{eq:VSS} \begin{split} &Vss \leq V \text{PIN} \leq V \text{DD}, \\ &\text{Pin at high-impedance}, \\ &-40^\circ\text{C} \leq \text{TA} \leq +85^\circ\text{C} \end{split}$	
DI51a		I/O Pins Not 5V Tolerant ⁽³⁾	-1	_	+1	μA	Analog pins shared with external reference pins, $-40^{\circ}C \le TA \le +85^{\circ}C$	
DI51b		I/O Pins Not 5V Tolerant ⁽³⁾	-1	_	+1	μA	$\label{eq:VSS} \begin{array}{l} VSS \leq VPIN \leq VDD, \\ Pin \text{ at high-impedance}, \\ -40^\circC \leq TA \leq +125^\circC \end{array}$	
DI51c		I/O Pins Not 5V Tolerant ⁽³⁾	-1	_	+1	μA	Analog pins shared with external reference pins, $-40^{\circ}C \le TA \le +125^{\circ}C$	
DI55		MCLR	-5	_	+5	μA	$Vss \leq V \text{PIN} \leq V \text{DD}$	
DI56		OSC1	-5	_	+5	μA	$\label{eq:VSS} \begin{array}{l} VSS \leq VPIN \leq VDD, \\ XT \text{ and } HS \text{ modes} \end{array}$	

TABLE 30-11: DC CHARACTERISTICS: I/O PIN INPUT SPECIFICATIONS (CONTINUED)

Note 1: The leakage current on the MCLR pin is strongly dependent on the applied voltage level. The specified levels represent normal operating conditions. Higher leakage current can be measured at different input voltages.

- 2: Negative current is defined as current sourced by the pin.
- 3: See the "Pin Diagrams" section for the 5V tolerant I/O pins.
- 4: VIL source < (Vss 0.3). Characterized but not tested.
- **5:** Non-5V tolerant pins VIH source > (VDD + 0.3), 5V tolerant pins VIH source > 5.5V. Characterized but not tested.
- 6: Digital 5V tolerant pins cannot tolerate any "positive" input injection current from input sources > 5.5V.
- 7: Non-zero injection currents can affect the ADC results by approximately 4-6 counts.

8: Any number and/or combination of I/O pins not excluded under IICL or IICH conditions are permitted provided the mathematical "absolute instantaneous" sum of the input injection currents from all pins do not exceed the specified limit. Characterized but not tested.



FIGURE 30-19: SPI2 SLAVE MODE (FULL-DUPLEX, CKE = 1, CKP = 1, SMP = 0) TIMING CHARACTERISTICS



FIGURE 30-36: ADC CONVERSION (12-BIT MODE) TIMING CHARACTERISTICS (ASAM = 0, SSRC<2:0> = 000, SSRCG = 0)

33.2 Package Details

28-Lead Skinny Plastic Dual In-Line (SP) – 300 mil Body [SPDIP]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



	Units		INCHES	
Dimensio	n Limits	MIN	NOM	MAX
Number of Pins	Ν		28	
Pitch	е		.100 BSC	
Top to Seating Plane	А	-	-	.200
Molded Package Thickness	A2	.120	.135	.150
Base to Seating Plane	A1	.015	-	-
Shoulder to Shoulder Width	E	.290	.310	.335
Molded Package Width	E1	.240	.285	.295
Overall Length	D	1.345	1.365	1.400
Tip to Seating Plane	L	.110	.130	.150
Lead Thickness	С	.008	.010	.015
Upper Lead Width	b1	.040	.050	.070
Lower Lead Width	b	.014	.018	.022
Overall Row Spacing §	eВ	_	_	.430

Notes:

1. Pin 1 visual index feature may vary, but must be located within the hatched area.

2. § Significant Characteristic.

3. Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed .010" per side.

4. Dimensioning and tolerancing per ASME Y14.5M.

BSC: Basic Dimension. Theoretically exact value shown without tolerances.

Microchip Technology Drawing C04-070B

36-Terminal Very Thin Thermal Leadless Array Package (TL) – 5x5x0.9 mm Body with Exposed Pad [VTLA]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging





DETAIL A

	Units	N	MILLIMETERS	
Dimension	Limits	MIN	NOM	MAX
Number of Pins	Ν	36		
Number of Pins per Side	ND	10		
Number of Pins per Side	NE	8		
Pitch	е	0.50 BSC		
Overall Height	А	0.80	0.90	1.00
Standoff	A1	0.025	-	0.075
Overall Width	E	5.00 BSC		
Exposed Pad Width	E2	3.60	3.75	3.90
Overall Length	D	5.00 BSC		
Exposed Pad Length	D2	3.60	3.75	3.90
Contact Width	b	0.20	0.25	0.30
Contact Length	L	0.20	0.25	0.30
Contact-to-Exposed Pad	K	0.20	-	-

Notes:

1. Pin 1 visual index feature may vary, but must be located within the hatched area.

2. Package is saw singulated.

3. Dimensioning and tolerancing per ASME Y14.5M.

BSC: Basic Dimension. Theoretically exact value shown without tolerances.

REF: Reference Dimension, usually without tolerance, for information purposes only.

Microchip Technology Drawing C04-187C Sheet 2 of 2

NOTES: