What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"
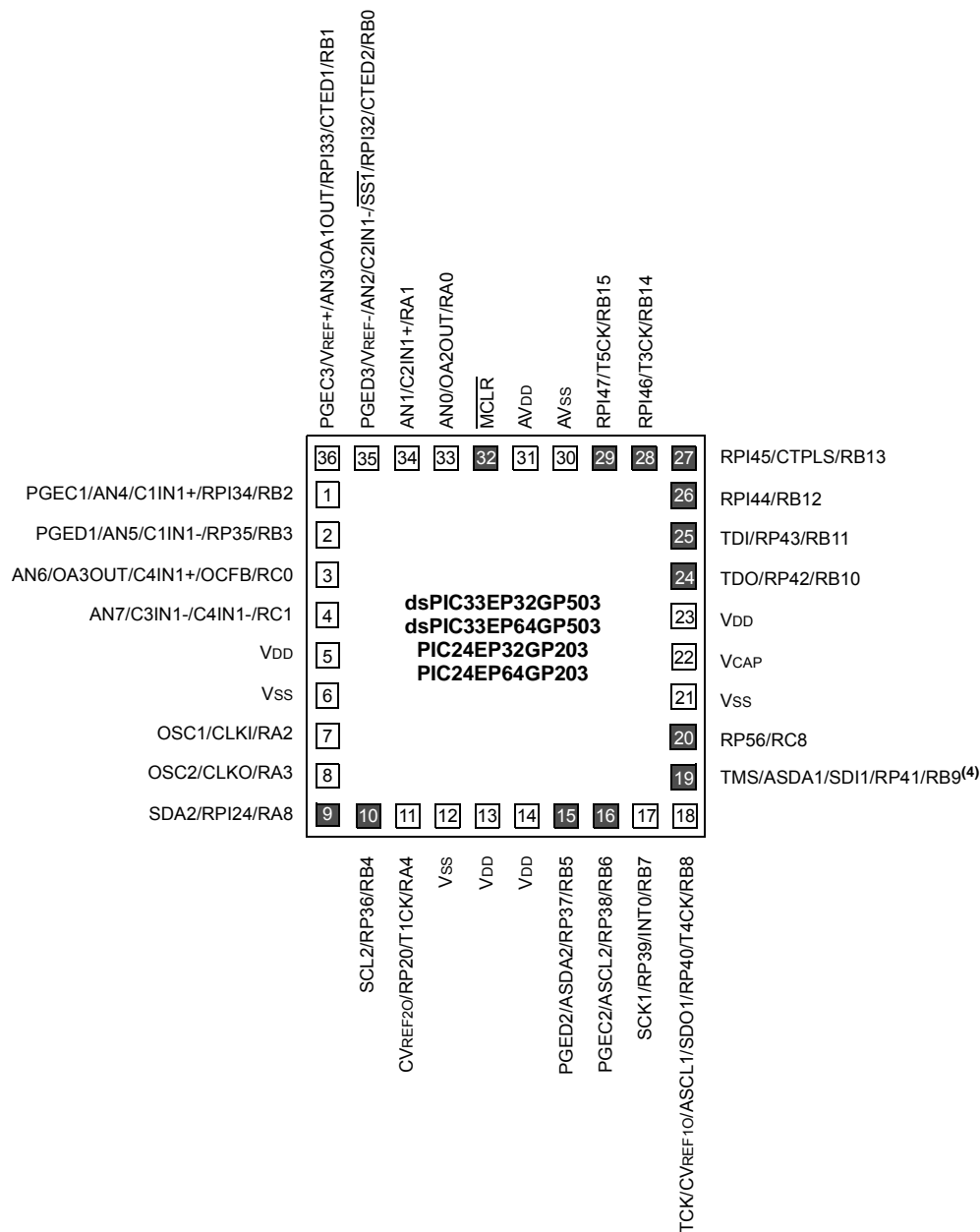
Details

Product Status	Active
Core Processor	PIC
Core Size	16-Bit
Speed	70 MIPs
Connectivity	I²C, IrDA, LINbus, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, DMA, POR, PWM, WDT
Number of I/O	35
Program Memory Size	32KB (10.7K x 24)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	2K x 16
Voltage - Supply (Vcc/Vdd)	3V ~ 3.6V
Data Converters	A/D 9x10b/12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	44-TQFP
Supplier Device Package	44-TQFP (10x10)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/pic24ep32gp204t-i-pt

Pin Diagrams (Continued)

36-Pin VTLA[1,2,3]

■ = Pins are up to 5V tolerant

Top pins (left to right, 36–27):
- 36: PGEC3/VREF+/AN3/OA1OUT/RPI33/CTED1/RB1
- 35: PGED3/VREF-/AN2/C2IN1-/SS1/RPI32/CTED2/RB0
- 34: AN1/C2IN1+/RA1
- 33: AN0/OA2OUT/RA0
- 32: MCLR
- 31: AVDD
- 30: AVSS
- 29: RPI47/T5CK/RB15
- 28: RPI46/T3CK/RB14

Left pins (1–9):
- 1: PGEC1/AN4/C1IN1+/RPI34/RB2
- 2: PGED1/AN5/C1IN1-/RP35/RB3
- 3: AN6/OA3OUT/C4IN1+/OCFB/RC0
- 4: AN7/C3IN1-/C4IN1-/RC1
- 5: VDD
- 6: VSS
- 7: OSC1/CLKI/RA2
- 8: OSC2/CLKO/RA3
- 9: SDA2/RPI24/RA8

Center device labels:
dsPIC33EP32GP503
dsPIC33EP64GP503
PIC24EP32GP203
PIC24EP64GP203

Right pins (27–19):
- 27: RPI45/CTPLS/RB13
- 26: RPI44/RB12
- 25: TDI/RP43/RB11
- 24: TDO/RP42/RB10
- 23: VDD
- 22: VCAP
- 21: VSS
- 20: RP56/RC8
- 19: TMS/ASDA1/SDI1/RP41/RB9[4]

Bottom pins (10–18):
- 10: SCL2/RP36/RB4
- 11: CVREF2O/RP20/T1CK/RA4
- 12: VSS
- 13: VDD
- 14: VDD
- 15: PGED2/ASDA2/RP37/RB5
- 16: PGEC2/ASCL2/RP38/RB6
- 17: SCK1/RP39/INT0/RB7
- 18: TCK/CVREF1O/ASCL1/SDO1/RP40/T4CK/RB8

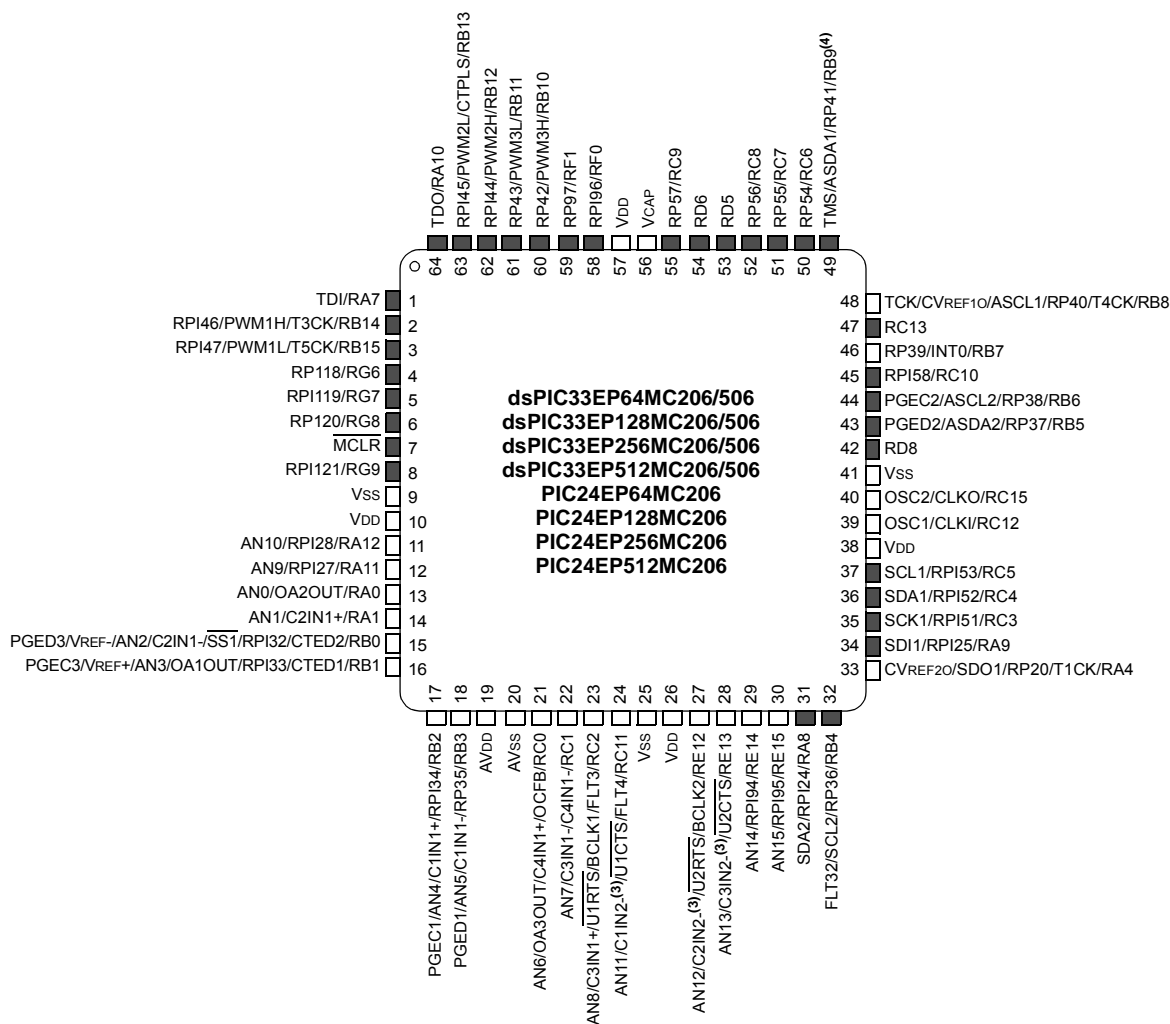**Note 1:** The RPn/RPIn pins can be used by any remappable peripheral with some limitation. See **Section 11.4 "Peripheral Pin Select (PPS)"** for available peripherals and for information on limitations.

2: Every I/O port pin (RAx-RGx) can be used as a Change Notification pin (CNAx-CNGx). See **Section 11.0 "I/O Ports"** for more information.

3: The metal pad at the bottom of the device is not connected to any pins and is recommended to be connected to VSS externally.

4: There is an internal pull-up resistor connected to the TMS pin when the JTAG interface is active. See the JTAGEN bit field in Table 27-2.

Pin Diagrams (Continued)

64-Pin TQFP[1,2,3]

■ = Pins are up to 5V tolerant

Top pins (64 to 49):
64 TDO/RA10
63 RPI45/PWM2L/CTPLS/RB13
62 RPI44/PWM2H/RB12
61 RP43/PWM3L/RB11
60 RP42/PWM3H/RB10
59 RP97/RF1
58 RPI96/RF0
57 VDD
56 VCAP
55 RP57/RC9
54 RD6
53 RD5
52 RP56/RC8
51 RP55/RC7
50 RP54/RC6
49 TMS/ASDA1/RP41/RB9[4]

Left pins (1 to 16):
1 TDI/RA7
2 RPI46/PWM1H/T3CK/RB14
3 RPI47/PWM1L/T5CK/RB15
4 RP118/RG6
5 RPI119/RG7
6 RP120/RG8
7 MCLR
8 RPI121/RG9
9 VSS
10 VDD
11 AN10/RPI28/RA12
12 AN9/RPI27/RA11
13 AN0/OA2OUT/RA0
14 AN1/C2IN1+/RA1
15 PGED3/VREF-/AN2/C2IN1-/SS1/RPI32/CTED2/RB0
16 PGEC3/VREF+/AN3/OA1OUT/RPI33/CTED1/RB1

Device center labels:
dsPIC33EP64MC206/506
dsPIC33EP128MC206/506
dsPIC33EP256MC206/506
dsPIC33EP512MC206/506
PIC24EP64MC206
PIC24EP128MC206
PIC24EP256MC206
PIC24EP512MC206

Right pins (48 to 33):
48 TCK/CVREF1O/ASCL1/RP40/T4CK/RB8
47 RC13
46 RP39/INT0/RB7
45 RPI58/RC10
44 PGEC2/ASCL2/RP38/RB6
43 PGED2/ASDA2/RP37/RB5
42 RD8
41 VSS
40 OSC2/CLKO/RC15
39 OSC1/CLKI/RC12
38 VDD
37 SCL1/RPI53/RC5
36 SDA1/RPI52/RC4
35 SCK1/RPI51/RC3
34 SDI1/RPI25/RA9
33 CVREF2O/SDO1/RP20/T1CK/RA4

Bottom pins (17 to 32):
17 PGEC1/AN4/C1IN1+/RPI34/RB2
18 PGED1/AN5/C1IN1-/RP35/RB3
19 AVDD
20 AVSS
21 AN6/OA3OUT/C4IN1+/OCFB/RC0
22 AN7/C3IN1-/C4IN1-/RC1
23 AN8/C3IN1+/U1RTS/BCLK1/FLT3/RC2
24 AN11/C1IN2-/U1CTS/FLT4/RC11
25 VSS
26 VDD
27 AN12/C2IN2-/U2RTS/BCLK2/RE12
28 AN13/C3IN2-/U2CTS/RE13
29 AN14/RPI94/RE14
30 AN15/RPI95/RE15
31 SDA2/RPI24/RA8
32 FLT32/SCL2/RP36/RB4

Note 1: The RPn/RPIn pins can be used by any remappable peripheral with some limitation. See **Section 11.4 "Peripheral Pin Select (PPS)"** for available peripherals and for information on limitations.

2: Every I/O port pin (RAx-RGx) can be used as a Change Notification pin (CNAx-CNGx). See **Section 11.0 "I/O Ports"** for more information.

3: The metal pad at the bottom of the device is not connected to any pins and is recommended to be connected to Vss externally.

4: There is an internal pull-up resistor connected to the TMS pin when the JTAG interface is active. See the JTAGEN bit field in Table 27-2.
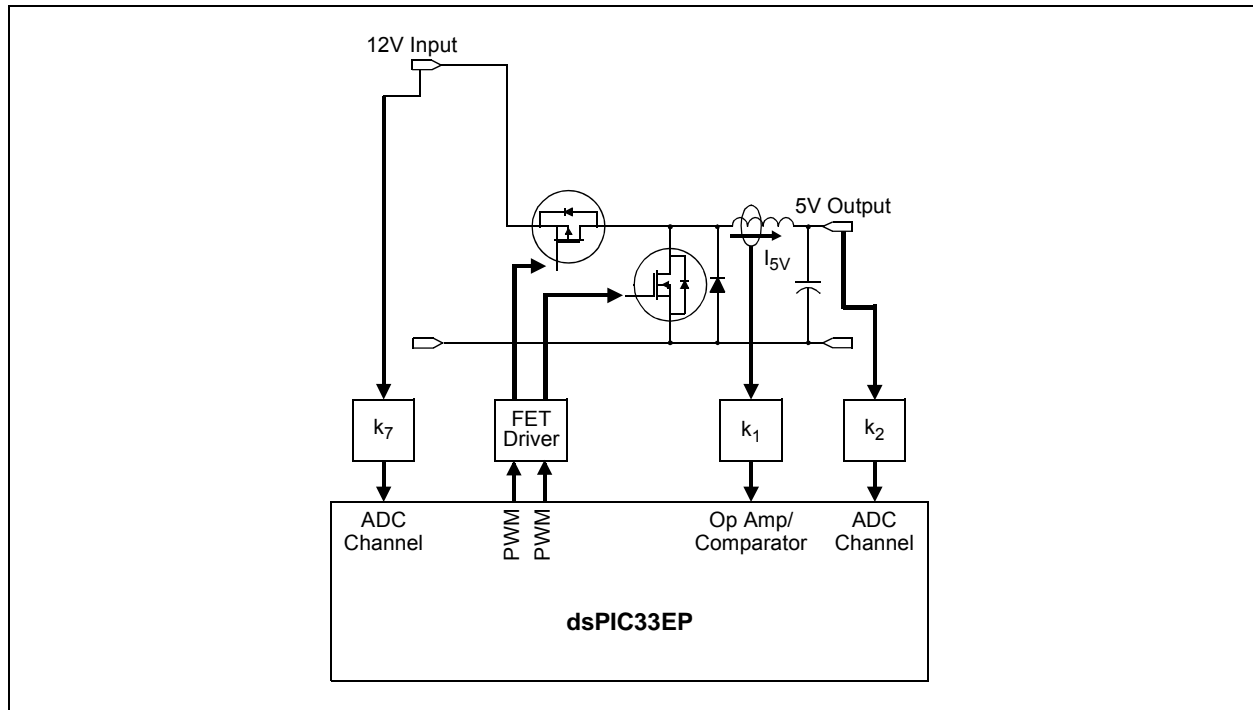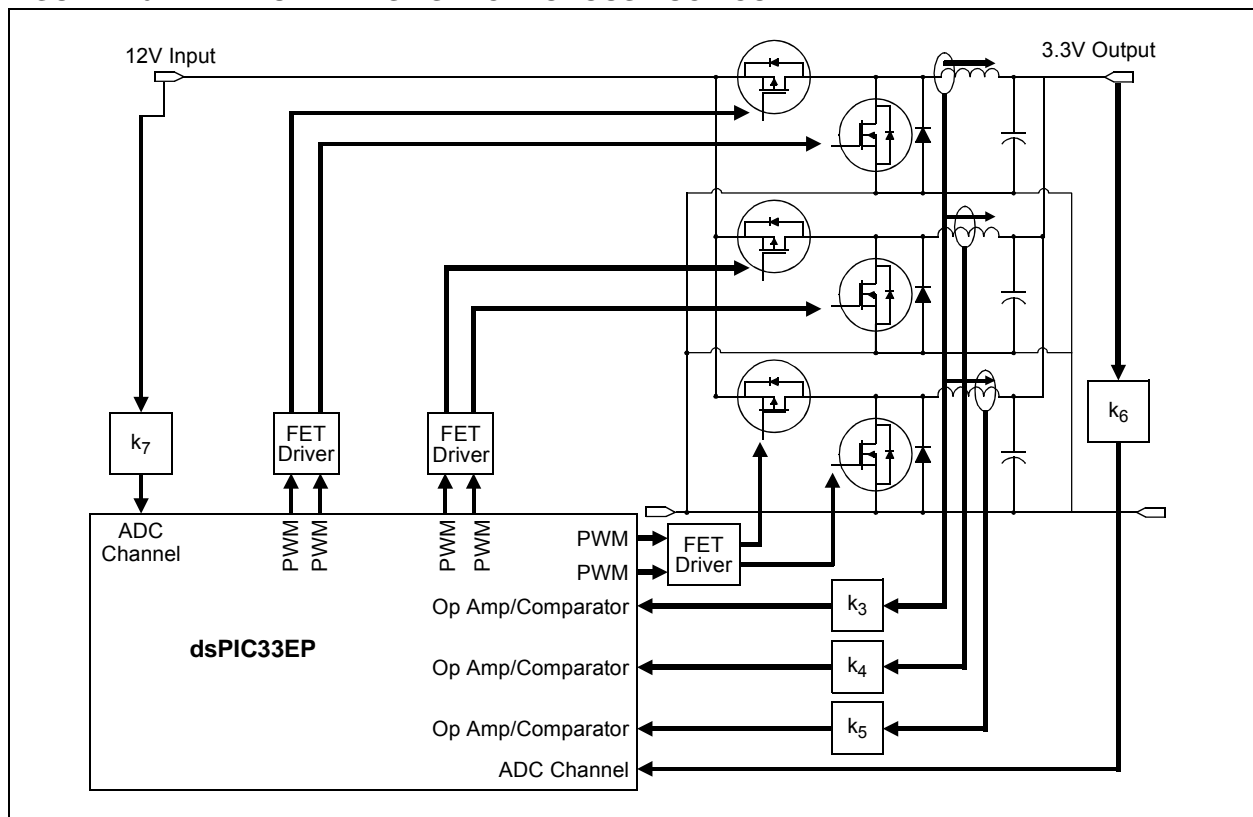
FIGURE 2-5: **SINGLE-PHASE SYNCHRONOUS BUCK CONVERTER**

FIGURE 2-6: **MULTIPHASE SYNCHRONOUS BUCK CONVERTER**

4.0   MEMORY ORGANIZATION

> **Note:** This data sheet summarizes the features of the dsPIC33EPXXXGP50X, dsPIC33EPXXXMC20X/50X and PIC24EPXXXGP/MC20X families of devices. It is not intended to be a comprehensive reference source. To complement the information in this data sheet, refer to **"Program Memory"** (DS70613) in the "*dsPIC33/PIC24 Family Reference Manual*", which is available from the Microchip web site (www.microchip.com).

The dsPIC33EPXXXGP50X, dsPIC33EPXXXMC20X/50X and PIC24EPXXXGP/MC20X architecture features separate program and data memory spaces, and buses. This architecture also allows the direct access of program memory from the Data Space (DS) during code execution.

4.1   Program Address Space

The program address memory space of the dsPIC33EPXXXGP50X, dsPIC33EPXXXMC20X/50X and PIC24EPXXXGP/MC20X devices is 4M instructions. The space is addressable by a 24-bit value derived either from the 23-bit PC during program execution, or from table operation or Data Space remapping, as described in **Section 4.8 "Interfacing Program and Data Memory Spaces"**.

User application access to the program memory space is restricted to the lower half of the address range (0x000000 to 0x7FFFFF). The exception is the use of TBLRD operations, which use TBLPAG<7> to read Device ID sections of the configuration memory space.

The program memory maps, which are presented by device family and memory size, are shown in Figure 4-1 through Figure 4-5.

FIGURE 4-1:   PROGRAM MEMORY MAP FOR dsPIC33EP32GP50X, dsPIC33EP32MC20X/50X AND PIC24EP32GP/MC20X DEVICES
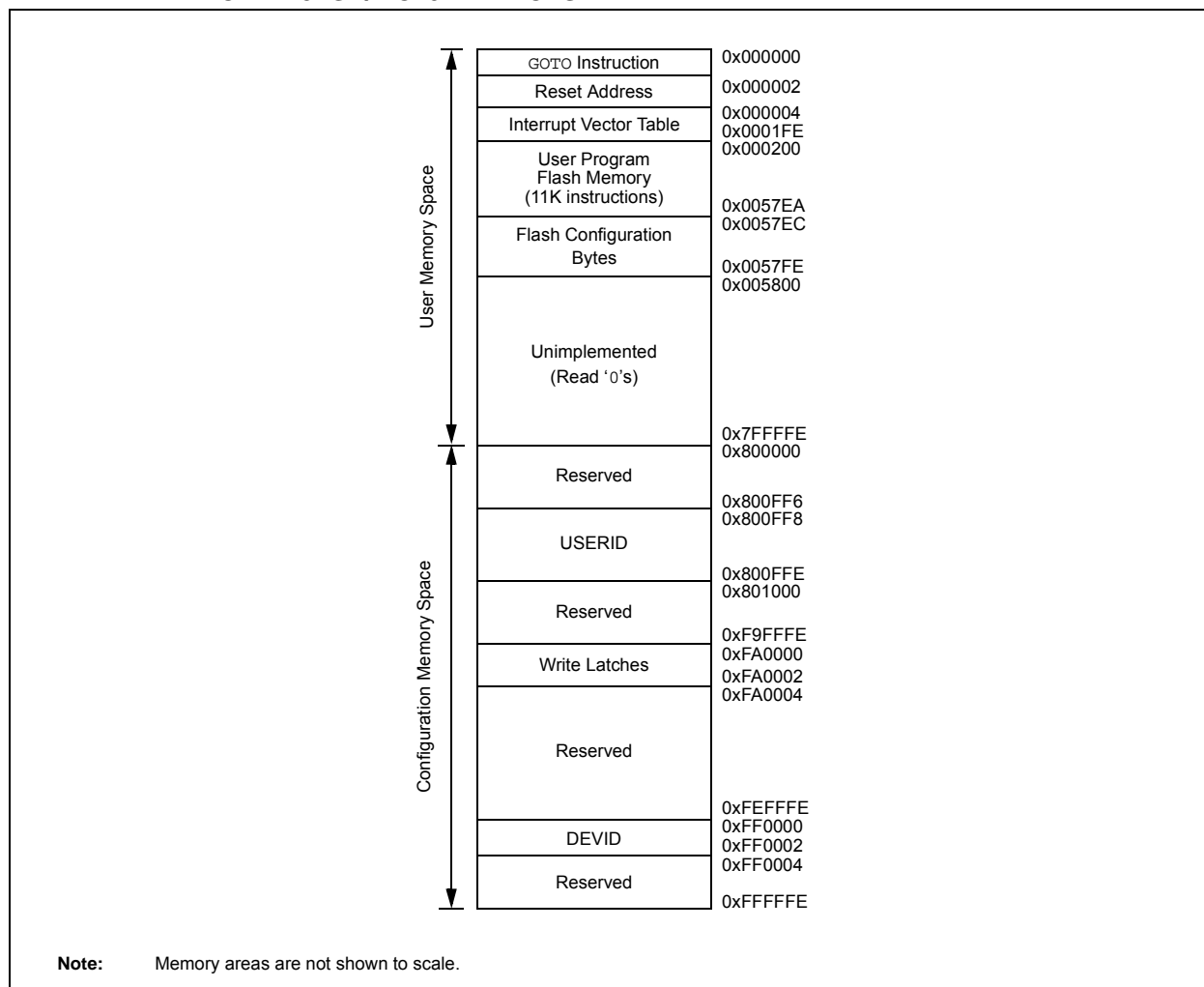

Note: Memory areas are not shown to scale.

TABLE 4-27: PERIPHERAL PIN SELECT OUTPUT REGISTER MAP FOR dsPIC33EPXXXGP/MC204/504 AND PIC24EPXXXGP/MC204 DEVICES ONLY

File Name	Addr.	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	All Resets
RPOR0	0680	—	—			RP35R<5:0>				—	—			RP20R<5:0>				0000
RPOR1	0682	—	—			RP37R<5:0>				—	—			RP36R<5:0>				0000
RPOR2	0684	—	—			RP39R<5:0>				—	—			RP38R<5:0>				0000
RPOR3	0686	—	—			RP41R<5:0>				—	—			RP40R<5:0>				0000
RPOR4	0688	—	—			RP43R<5:0>				—	—			RP42R<5:0>				0000
RPOR5	068A	—	—			RP55R<5:0>				—	—			RP54R<5:0>				0000
RPOR6	068C	—	—			RP57R<5:0>				—	—			RP56R<5:0>				0000

Legend: — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

TABLE 4-28: PERIPHERAL PIN SELECT OUTPUT REGISTER MAP FOR dsPIC33EPXXXGP/MC206/506 AND PIC24EPXXXGP/MC206 DEVICES ONLY

File Name	Addr.	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	All Resets
RPOR0	0680	—	—			RP35R<5:0>				—	—			RP20R<5:0>				0000
RPOR1	0682	—	—			RP37R<5:0>				—	—			RP36R<5:0>				0000
RPOR2	0684	—	—			RP39R<5:0>				—	—			RP38R<5:0>				0000
RPOR3	0686	—	—			RP41R<5:0>				—	—			RP40R<5:0>				0000
RPOR4	0688	—	—			RP43R<5:0>				—	—			RP42R<5:0>				0000
RPOR5	068A	—	—			RP55R<5:0>				—	—			RP54R<5:0>				0000
RPOR6	068C	—	—			RP57R<5:0>				—	—			RP56R<5:0>				0000
RPOR7	068E	—	—			RP97R<5:0>				—	—	—	—	—	—	—	—	0000
RPOR8	0690	—	—			RP118R<5:0>				—	—	—	—	—	—	—	—	0000
RPOR9	0692	—	—	—	—	—	—	—	—	—	—			RP120R<5:0>				0000

Legend: — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

FIGURE 7-1: **dsPIC33EPXXXGP50X, dsPIC33EPXXXMC20X/50X AND PIC24EPXXXGP/MC20X INTERRUPT VECTOR TABLE**

Reset – GOTO Instruction	0x000000
Reset – GOTO Address	0x000002
Oscillator Fail Trap Vector	0x000004
Address Error Trap Vector	0x000006
Generic Hard Trap Vector	0x000008
Stack Error Trap Vector	0x00000A
Math Error Trap Vector	0x00000C
DMAC Error Trap Vector	0x00000E
Generic Soft Trap Vector	0x000010
Reserved	0x000012
Interrupt Vector 0	0x000014
Interrupt Vector 1	0x000016
:	:
:	:
:	:
Interrupt Vector 52	0x00007C
Interrupt Vector 53	0x00007E
Interrupt Vector 54	0x000080
:	:
:	:
:	:
Interrupt Vector 116	0x0000FC
Interrupt Vector 117	0x0000FE
Interrupt Vector 118	0x000100
Interrupt Vector 119	0x000102
Interrupt Vector 120	0x000104
:	:
:	:
:	:
Interrupt Vector 244	0x0001FC
Interrupt Vector 245	0x0001FE
START OF CODE	0x000200

Decreasing Natural Order Priority

IVT

See Table 7-1 for Interrupt Vector Details

REGISTER 11-17: RPINR39: PERIPHERAL PIN SELECT INPUT REGISTER 39 (dsPIC33EPXXXMC20X/50X AND PIC24EPXXXMC20X DEVICES ONLY)

U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
—	DTCMP3R<6:0>						
bit 15							bit 8

U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
—	DTCMP2R<6:0>						
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15 **Unimplemented:** Read as '0'

bit 14-8 **DTCMP3R<6:0>:** Assign PWM Dead-Time Compensation Input 3 to the Corresponding RPn Pin bits (see Table 11-2 for input pin selection numbers)

1111001 = Input tied to RPI121
.
.
.
0000001 = Input tied to CMP1
0000000 = Input tied to Vss

bit 7 **Unimplemented:** Read as '0'

bit 6-0 **DTCMP2R<6:0>:** Assign PWM Dead-Time Compensation Input 2 to the Corresponding RPn Pin bits (see Table 11-2 for input pin selection numbers)

1111001 = Input tied to RPI121
.
.
.
0000001 = Input tied to CMP1
0000000 = Input tied to Vss

14.1   Input Capture Resources

Many useful resources are provided on the main product page of the Microchip web site for the devices listed in this data sheet. This product page, which can be accessed using this link, contains the latest updates and additional information.

Note:	In the event you are not able to access the product page using the link above, enter this URL in your browser: http://www.microchip.com/wwwproducts/Devices.aspx?dDocName=en555464

14.1.1   KEY RESOURCES

• **"Input Capture"** (DS70352) in the *"dsPIC33/PIC24 Family Reference Manual"*
• Code Samples
• Application Notes
• Software Libraries
• Webinars
• All Related *"dsPIC33/PIC24 Family Reference Manual"* Sections
• Development Tools

REGISTER 21-26: CxTRmnCON: ECANx TX/RX BUFFER mn CONTROL REGISTER
(m = 0,2,4,6; n = 1,3,5,7)

R/W-0	R-0	R-0	R-0	R/W-0	R/W-0	R/W-0	R/W-0
TXENn	TXABTn	TXLARBn	TXERRn	TXREQn	RTRENn	TXnPRI1	TXnPRI0
bit 15							bit 8

R/W-0	R-0	R-0	R-0	R/W-0	R/W-0	R/W-0	R/W-0
TXENm	TXABTm[(1)]	TXLARBm[(1)]	TXERRm[(1)]	TXREQm	RTRENm	TXmPRI1	TXmPRI0
bit 7							bit 0

Legend:		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared x = Bit is unknown

bit 15-8   See Definition for bits<7:0>, Controls Buffer n

bit 7   **TXENm:** TX/RX Buffer Selection bit

    1 = Buffer TRBn is a transmit buffer
    0 = Buffer TRBn is a receive buffer

bit 6   **TXABTm:** Message Aborted bit[(1)]

    1 = Message was aborted
    0 = Message completed transmission successfully

bit 5   **TXLARBm:** Message Lost Arbitration bit[(1)]

    1 = Message lost arbitration while being sent
    0 = Message did not lose arbitration while being sent

bit 4   **TXERRm:** Error Detected During Transmission bit[(1)]

    1 = A bus error occurred while the message was being sent
    0 = A bus error did not occur while the message was being sent

bit 3   **TXREQm:** Message Send Request bit

    1 = Requests that a message be sent; the bit automatically clears when the message is successfully sent
    0 = Clearing the bit to '0' while set requests a message abort

bit 2   **RTRENm:** Auto-Remote Transmit Enable bit

    1 = When a remote transmit is received, TXREQ will be set
    0 = When a remote transmit is received, TXREQ will be unaffected

bit 1-0   **TXmPRI<1:0>:** Message Transmission Priority bits

    11 = Highest message priority
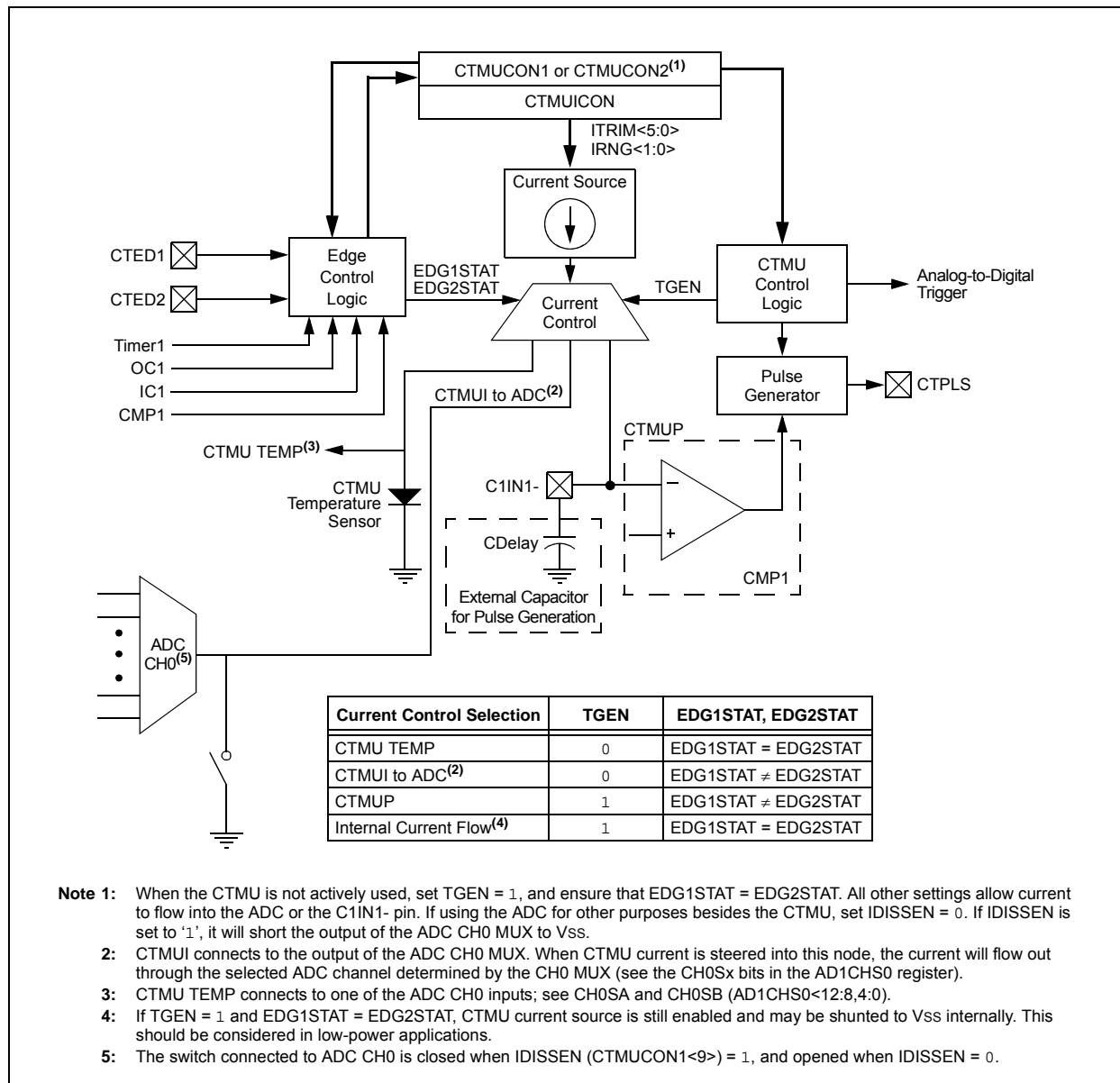   10 = High intermediate message priority
    01 = Low intermediate message priority
    00 = Lowest message priority

Note 1:   This bit is cleared when TXREQ is set.

> **Note:**   The buffers, SID, EID, DLC, Data Field, and Receive Status registers are located in DMA RAM.

FIGURE 22-1: **CTMU BLOCK DIAGRAM**

Current Control Selection	TGEN	EDG1STAT, EDG2STAT
CTMU TEMP	0	EDG1STAT = EDG2STAT
CTMUI to ADC[2]	0	EDG1STAT ≠ EDG2STAT
CTMUP	1	EDG1STAT ≠ EDG2STAT
Internal Current Flow[4]	1	EDG1STAT = EDG2STAT

Note 1: When the CTMU is not actively used, set TGEN = 1, and ensure that EDG1STAT = EDG2STAT. All other settings allow current to flow into the ADC or the C1IN1- pin. If using the ADC for other purposes besides the CTMU, set IDISSEN = 0. If IDISSEN is set to '1', it will short the output of the ADC CH0 MUX to Vss.

2: CTMUI connects to the output of the ADC CH0 MUX. When CTMU current is steered into this node, the current will flow out through the selected ADC channel determined by the CH0 MUX (see the CH0Sx bits in the AD1CHS0 register).

3: CTMU TEMP connects to one of the ADC CH0 inputs; see CH0SA and CH0SB (AD1CHS0<12:8,4:0>).

4: If TGEN = 1 and EDG1STAT = EDG2STAT, CTMU current source is still enabled and may be shunted to Vss internally. This should be considered in low-power applications.

5: The switch connected to ADC CH0 is closed when IDISSEN (CTMUCON1<9>) = 1, and opened when IDISSEN = 0.

22.1 CTMU Resources

Many useful resources are provided on the main product page of the Microchip web site for the devices listed in this data sheet. This product page, which can be accessed using this link, contains the latest updates and additional information.

> **Note:** In the event you are not able to access the product page using the link above, enter this URL in your browser: http://www.microchip.com/wwwproducts/Devices.aspx?dDocName=en555464

22.1.1 KEY RESOURCES

- **"Charge Time Measurement Unit (CTMU)"** (DS70661) in the *"dsPIC33/PIC24 Family Reference Manual"*
- Code Samples
- Application Notes
- Software Libraries
- Webinars
- All Related *"dsPIC33/PIC24 Family Reference Manual"* Sections
- Development Tools

REGISTER 24-8: PTGC1LIM: PTG COUNTER 1 LIMIT REGISTER[1]

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
			PTGC1LIM<15:8>				
bit 15							bit 8

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
			PTGC1LIM<7:0>				
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15-0 **PTGC1LIM<15:0>:** PTG Counter 1 Limit Register bits

May be used to specify the loop count for the PTGJMPC1 Step command or as a limit register for the General Purpose Counter 1.

Note 1: This register is read-only when the PTG module is executing Step commands (PTGEN = 1 and PTGSTRT = 1).

REGISTER 24-9: PTGHOLD: PTG HOLD REGISTER[1]

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
			PTGHOLD<15:8>				
bit 15							bit 8

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
			PTGHOLD<7:0>				
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15-0 **PTGHOLD<15:0>:** PTG General Purpose Hold Register bits

Holds user-supplied data to be copied to the PTGTxLIM, PTGCxLIM, PTGSDLIM or PTGL0 registers with the PTGCOPY command.

Note 1: This register is read-only when the PTG module is executing Step commands (PTGEN = 1 and PTGSTRT = 1).

25.3 Op Amp/Comparator Registers

REGISTER 25-1: CMSTAT: OP AMP/COMPARATOR STATUS REGISTER

R/W-0	U-0	U-0	U-0	R-0	R-0	R-0	R-0
PSIDL	—	—	—	C4EVT[1]	C3EVT[1]	C2EVT[1]	C1EVT[1]
bit 15							bit 8

U-0	U-0	U-0	U-0	R-0	R-0	R-0	R-0
—	—	—	—	C4OUT[2]	C3OUT[2]	C2OUT[2]	C1OUT[2]
bit 7							bit 0

Legend:		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15   **PSIDL:** Comparator Stop in Idle Mode bit

1 = Discontinues operation of all comparators when device enters Idle mode
0 = Continues operation of all comparators in Idle mode

bit 14-12   **Unimplemented:** Read as '0'

bit 11   **C4EVT:** Op Amp/Comparator 4 Event Status bit[1]

1 = Op amp/comparator event occurred
0 = Op amp/comparator event did not occur

bit 10   **C3EVT:** Comparator 3 Event Status bit[1]

1 = Comparator event occurred
0 = Comparator event did not occur

bit 9   **C2EVT:** Comparator 2 Event Status bit[1]

1 = Comparator event occurred
0 = Comparator event did not occur

bit 8   **C1EVT:** Comparator 1 Event Status bit[1]

1 = Comparator event occurred
0 = Comparator event did not occur

bit 7-4   **Unimplemented:** Read as '0'

bit 3   **C4OUT:** Comparator 4 Output Status bit[2]

When CPOL = 0:
1 = $V_{IN+} > V_{IN-}$
0 = $V_{IN+} < V_{IN-}$
When CPOL = 1:
1 = $V_{IN+} < V_{IN-}$
0 = $V_{IN+} > V_{IN-}$

bit 2   **C3OUT:** Comparator 3 Output Status bit[2]

When CPOL = 0:
1 = $V_{IN+} > V_{IN-}$
0 = $V_{IN+} < V_{IN-}$
When CPOL = 1:
1 = $V_{IN+} < V_{IN-}$
0 = $V_{IN+} > V_{IN-}$

Note 1: Reflects the value of the of the CEVT bit in the respective Op Amp/Comparator Control register, CMxCON<9>.

2: Reflects the value of the COUT bit in the respective Op Amp/Comparator Control register, CMxCON<8>.

NOTES:

TABLE 27-2:   CONFIGURATION BITS DESCRIPTION

Bit Field	Description
GCP	General Segment Code-Protect bit `1` = User program memory is not code-protected `0` = Code protection is enabled for the entire program memory space
GWRP	General Segment Write-Protect bit `1` = User program memory is not write-protected `0` = User program memory is write-protected
IESO	Two-Speed Oscillator Start-up Enable bit `1` = Start up device with FRC, then automatically switch to the user-selected oscillator source when ready `0` = Start up device with user-selected oscillator source
PWMLOCK[1]	PWM Lock Enable bit `1` = Certain PWM registers may only be written after a key sequence `0` = PWM registers may be written without a key sequence
FNOSC<2:0>	Oscillator Selection bits `111` = Fast RC Oscillator with Divide-by-N (FRCDIVN) `110` = Fast RC Oscillator with Divide-by-16 (FRCDIV16) `101` = Low-Power RC Oscillator (LPRC) `100` = Reserved; do not use `011` = Primary Oscillator with PLL module (XT + PLL, HS + PLL, EC + PLL) `010` = Primary Oscillator (XT, HS, EC) `001` = Fast RC Oscillator with Divide-by-N with PLL module (FRCPLL) `000` = Fast RC Oscillator (FRC)
FCKSM<1:0>	Clock Switching Mode bits `1x` = Clock switching is disabled, Fail-Safe Clock Monitor is disabled `01` = Clock switching is enabled, Fail-Safe Clock Monitor is disabled `00` = Clock switching is enabled, Fail-Safe Clock Monitor is enabled
IOL1WAY	Peripheral Pin Select Configuration bit `1` = Allow only one reconfiguration `0` = Allow multiple reconfigurations
OSCIOFNC	OSC2 Pin Function bit (except in XT and HS modes) `1` = OSC2 is the clock output `0` = OSC2 is a general purpose digital I/O pin
POSCMD<1:0>	Primary Oscillator Mode Select bits `11` = Primary Oscillator is disabled `10` = HS Crystal Oscillator mode `01` = XT Crystal Oscillator mode `00` = EC (External Clock) mode
FWDTEN	Watchdog Timer Enable bit `1` = Watchdog Timer is always enabled (LPRC oscillator cannot be disabled. Clearing the SWDTEN bit in the RCON register will have no effect.) `0` = Watchdog Timer is enabled/disabled by user software (LPRC can be disabled by clearing the SWDTEN bit in the RCON register)
WINDIS	Watchdog Timer Window Enable bit `1` = Watchdog Timer in Non-Window mode `0` = Watchdog Timer in Window mode
PLLKEN	PLL Lock Enable bit `1` = PLL lock is enabled `0` = PLL lock is disabled

Note 1:   This bit is only available on dsPIC33EPXXXMC20X/50X and PIC24EPXXXMC20X devices.

2:   When JTAGEN = `1`, an internal pull-up resistor is enabled on the TMS pin. Erased devices default to JTAGEN = `1`. Applications requiring I/O pins in a high-impedance state (tri-state) in Reset should use pins other than TMS for this purpose.

27.2 User ID Words

dsPIC33EPXXXGP50X, dsPIC33EPXXXMC20X/50X and PIC24EPXXXGP/MC20X devices contain four User ID Words, located at addresses, 0x800FF8 through 0x800FFE. The User ID Words can be used for storing product information such as serial numbers, system manufacturing dates, manufacturing lot numbers and other application-specific information.

The User ID Words register map is shown in Table 27-3.

TABLE 27-3: USER ID WORDS REGISTER MAP

File Name	Address	Bits 23-16	Bits 15-0
FUID0	0x800FF8	—	UID0
FUID1	0x800FFA	—	UID1
FUID2	0x800FFC	—	UID2
FUID3	0x800FFE	—	UID3

Legend: — = unimplemented, read as '1'.

27.3 On-Chip Voltage Regulator

All of the dsPIC33EPXXXGP50X, dsPIC33EPXXXMC20X/50X and PIC24EPXXXGP/MC20X devices power their core digital logic at a nominal 1.8V. This can create a conflict for designs that are required to operate at a higher typical voltage, such as 3.3V. To simplify system design, all devices in the dsPIC33EPXXXGP50X, dsPIC33EPXXXMC20X/50X and PIC24EPXXXGP/MC20X family incorporate an on-chip regulator that allows the device to run its core logic from V_{DD}.

The regulator provides power to the core from the other V_{DD} pins. A low-ESR (less than 1 Ohm) capacitor (such as tantalum or ceramic) must be connected to the V_{CAP} pin (Figure 27-1). This helps to maintain the stability of the regulator. The recommended value for the filter capacitor is provided in Table 30-5 located in **Section 30.0 "Electrical Characteristics"**.

> **Note:** It is important for the low-ESR capacitor to be placed as close as possible to the V_{CAP} pin.

FIGURE 27-1: CONNECTIONS FOR THE ON-CHIP VOLTAGE REGULATOR[1,2,3]

> **Note 1:** These are typical operating voltages. Refer to Table 30-5 located in **Section 30.1 "DC Characteristics"** for the full operating ranges of V_{DD} and V_{CAP}.
> **2:** It is important for the low-ESR capacitor to be placed as close as possible to the V_{CAP} pin.
> **3:** Typical V_{CAP} pin voltage = 1.8V when $V_{DD} \geq V_{DDMIN}$.
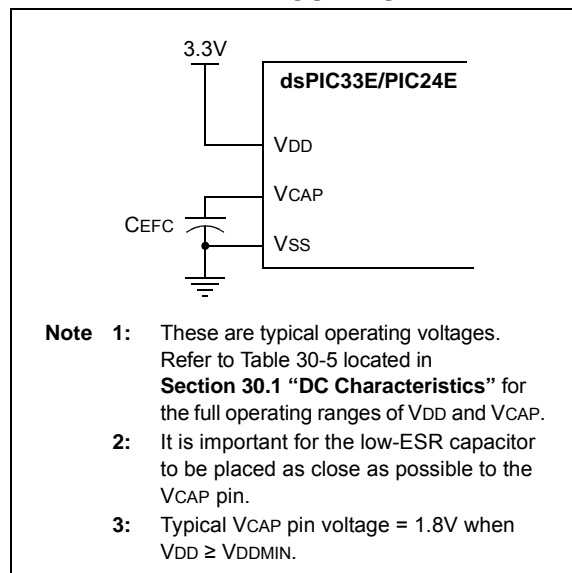
27.4 Brown-out Reset (BOR)

The Brown-out Reset (BOR) module is based on an internal voltage reference circuit that monitors the regulated supply voltage, V_{CAP}. The main purpose of the BOR module is to generate a device Reset when a brown-out condition occurs. Brown-out conditions are generally caused by glitches on the AC mains (for example, missing portions of the AC cycle waveform due to bad power transmission lines or voltage sags due to excessive current draw when a large inductive load is turned on).

A BOR generates a Reset pulse, which resets the device. The BOR selects the clock source, based on the device Configuration bit values (FNOSC<2:0> and POSCMD<1:0>).

If an oscillator mode is selected, the BOR activates the Oscillator Start-up Timer (OST). The system clock is held until OST expires. If the PLL is used, the clock is held until the LOCK bit (OSCCON<5>) is '1'.

Concurrently, the PWRT Time-out (T_{PWRT}) is applied before the internal Reset is released. If T_{PWRT} = 0 and a crystal oscillator is being used, then a nominal delay of T_{FSCM} is applied. The total delay in this case is T_{FSCM}. Refer to Parameter SY35 in Table 30-22 of **Section 30.0 "Electrical Characteristics"** for specific T_{FSCM} values.

The BOR status bit (RCON<1>) is set to indicate that a BOR has occurred. The BOR circuit continues to operate while in Sleep or Idle modes and resets the device should V_{DD} fall below the BOR threshold voltage.
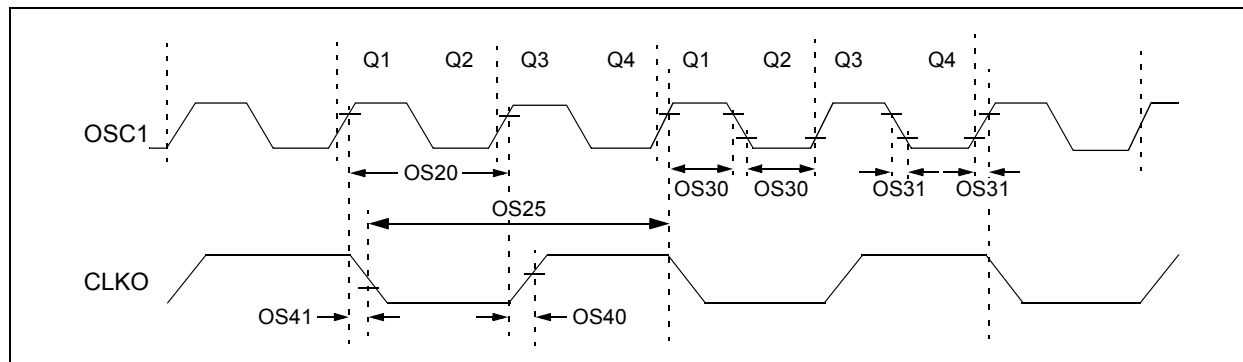
FIGURE 30-2:   EXTERNAL CLOCK TIMING

TABLE 30-17:   EXTERNAL CLOCK TIMING REQUIREMENTS

AC CHARACTERISTICS			Standard Operating Conditions: 3.0V to 3.6V (unless otherwise stated) Operating temperature -40°C ≤ TA ≤ +85°C for Industrial -40°C ≤ TA ≤ +125°C for Extended				
Param No.	Symb	Characteristic	Min.	Typ.[1]	Max.	Units	Conditions
OS10	FIN	External CLKI Frequency (External clocks allowed only in EC and ECPLL modes)	DC	—	60	MHz	EC
		Oscillator Crystal Frequency	3.5 10	— —	10 25	MHz MHz	XT HS
OS20	TOSC	TOSC = 1/FOSC	8.33	—	DC	ns	+125ºC
		TOSC = 1/FOSC	7.14	—	DC	ns	+85ºC
OS25	TCY	Instruction Cycle Time[2]	16.67	—	DC	ns	+125ºC
		Instruction Cycle Time[2]	14.28	—	DC	ns	+85ºC
OS30	TosL, TosH	External Clock in (OSC1) High or Low Time	0.45 x TOSC	—	0.55 x TOSC	ns	EC
OS31	TosR, TosF	External Clock in (OSC1) Rise or Fall Time	—	—	20	ns	EC
OS40	TckR	CLKO Rise Time[3,4]	—	5.2	—	ns	
OS41	TckF	CLKO Fall Time[3,4]	—	5.2	—	ns	
OS42	GM	External Oscillator Transconductance[4]	—	12	—	mA/V	HS, VDD = 3.3V, TA = +25ºC
			—	6	—	mA/V	XT, VDD = 3.3V, TA = +25ºC

Note 1:   Data in "Typical" column is at 3.3V, +25°C unless otherwise stated.

2:   Instruction cycle period (TCY) equals two times the input oscillator time base period. All specified values are based on characterization data for that particular oscillator type under standard operating conditions with the device executing code. Exceeding these specified limits may result in an unstable oscillator operation and/or higher than expected current consumption. All devices are tested to operate at "Minimum" values with an external clock applied to the OSC1 pin. When an external clock input is used, the "Maximum" cycle time limit is "DC" (no clock) for all devices.

3:   Measurements are taken in EC mode. The CLKO signal is measured on the OSC2 pin.

4:   This parameter is characterized, but not tested in manufacturing.

TABLE 30-18: PLL CLOCK TIMING SPECIFICATIONS

AC CHARACTERISTICS			Standard Operating Conditions: 3.0V to 3.6V (unless otherwise stated) Operating temperature -40°C ≤ TA ≤ +85°C for Industrial -40°C ≤ TA ≤ +125°C for Extended				
Param No.	Symbol	Characteristic	Min.	Typ.[1]	Max.	Units	Conditions
OS50	F_{PLLI}	PLL Voltage Controlled Oscillator (VCO) Input Frequency Range	0.8	—	8.0	MHz	ECPLL, XTPLL modes
OS51	F_{VCO}	On-Chip VCO System Frequency	120	—	340	MHz	
OS52	T_{LOCK}	PLL Start-up Time (Lock Time)	0.9	1.5	3.1	ms	
OS53	D_{CLK}	CLKO Stability (Jitter)[2]	-3	0.5	3	%	

Note 1: Data in "Typical" column is at 3.3V, +25°C unless otherwise stated. Parameters are for design guidance only and are not tested.

2: This jitter specification is based on clock cycle-by-clock cycle measurements. To get the effective jitter for individual time bases, or communication clocks used by the application, use the following formula:

$$Effective\ Jitter = \frac{D_{CLK}}{\sqrt{\frac{F_{OSC}}{Time\ Base\ or\ Communication\ Clock}}}$$

For example, if F_{OSC} = 120 MHz and the SPIx bit rate = 10 MHz, the effective jitter is as follows:

$$Effective\ Jitter = \frac{D_{CLK}}{\sqrt{\frac{120}{10}}} = \frac{D_{CLK}}{\sqrt{12}} = \frac{D_{CLK}}{3.464}$$

TABLE 30-19: INTERNAL FRC ACCURACY

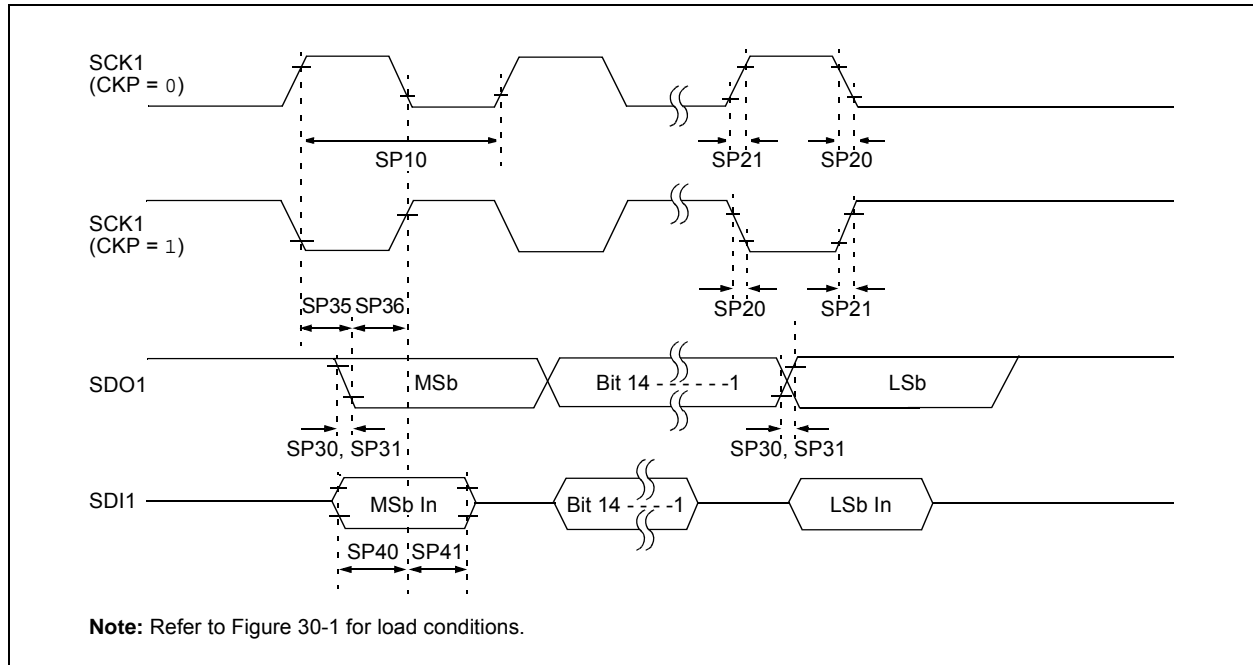| AC CHARACTERISTICS		Standard Operating Conditions: 3.0V to 3.6V (unless otherwise stated) Operating temperature -40°C ≤ TA ≤ +85°C for Industrial -40°C ≤ TA ≤ +125°C for Extended				
Param No.	Characteristic	Min.	Typ.	Max.	Units	Conditions
Internal FRC Accuracy @ FRC Frequency = 7.37 MHz[1]						
F20a	FRC	-1.5	0.5	+1.5	%	-40°C ≤ TA ≤ -10°C VDD = 3.0-3.6V
		-1	0.5	+1	%	-10°C ≤ TA ≤ +85°C VDD = 3.0-3.6V
F20b	FRC	-2	1	+2	%	+85°C ≤ TA ≤ +125°C VDD = 3.0-3.6V

Note 1: Frequency is calibrated at +25°C and 3.3V. TUNx bits can be used to compensate for temperature drift.

TABLE 30-20: INTERNAL LPRC ACCURACY

AC CHARACTERISTICS		Standard Operating Conditions: 3.0V to 3.6V (unless otherwise stated) Operating temperature -40°C ≤ TA ≤ +85°C for Industrial -40°C ≤ TA ≤ +125°C for Extended				
Param No.	Characteristic	Min.	Typ.	Max.	Units	Conditions
LPRC @ 32.768 kHz[1]						
F21a	LPRC	-30	—	+30	%	-40°C ≤ TA ≤ -10°C VDD = 3.0-3.6V
		-20	—	+20	%	-10°C ≤ TA ≤ +85°C VDD = 3.0-3.6V
F21b	LPRC	-30	—	+30	%	+85°C ≤ TA ≤ +125°C VDD = 3.0-3.6V

Note 1: The change of LPRC frequency as VDD changes.

FIGURE 30-25: SPI1 MASTER MODE (FULL-DUPLEX, CKE = 0, CKP = x, SMP = 1)
TIMING CHARACTERISTICS

Note: Refer to Figure 30-1 for load conditions.

TABLE 30-44: SPI1 MASTER MODE (FULL-DUPLEX, CKE = 0, CKP = x, SMP = 1)
TIMING REQUIREMENTS

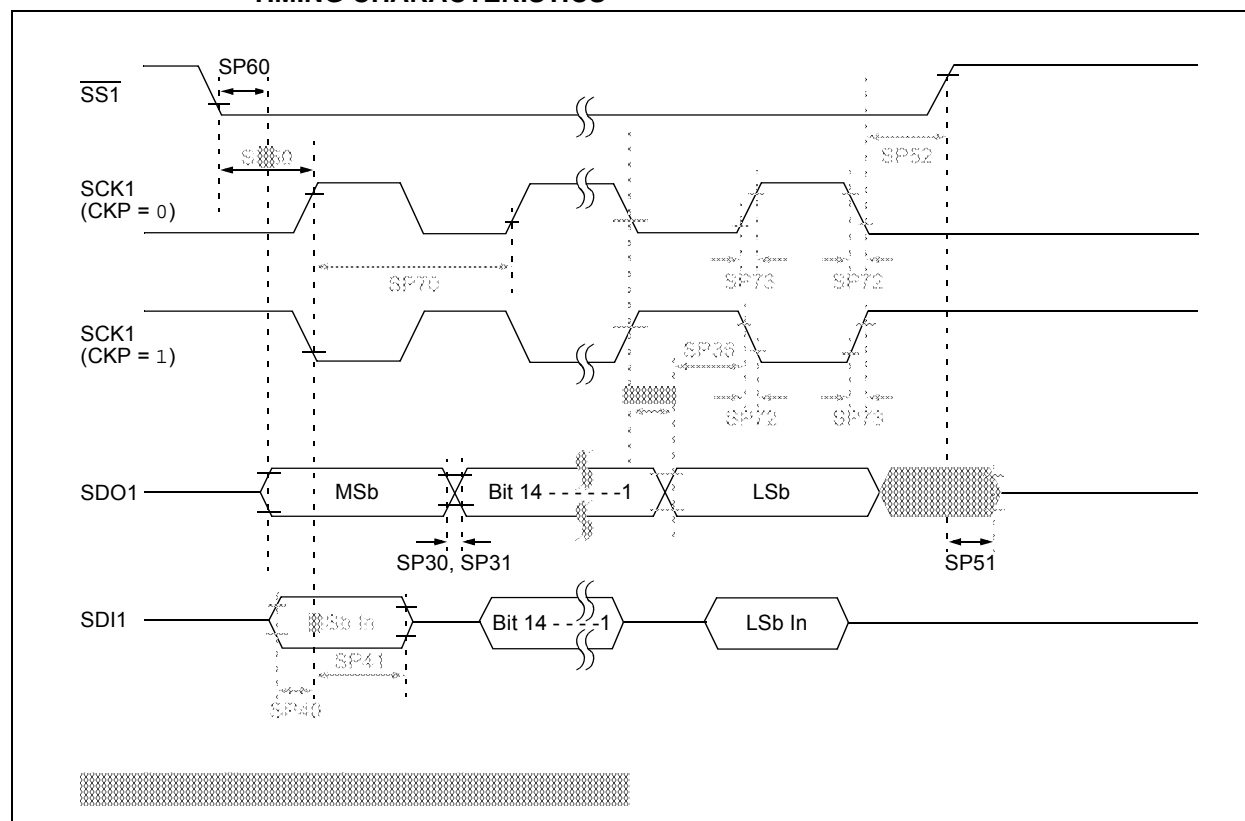| AC CHARACTERISTICS			Standard Operating Conditions: 3.0V to 3.6V (unless otherwise stated) Operating temperature -40°C ≤ TA ≤ +85°C for Industrial -40°C ≤ TA ≤ +125°C for Extended				
Param.	Symbol	Characteristic[1]	Min.	Typ.[2]	Max.	Units	Conditions
SP10	FscP	Maximum SCK1 Frequency	—	—	10	MHz	-40ºC to +125ºC **(Note 3)**
SP20	TscF	SCK1 Output Fall Time	—	—	—	ns	See Parameter DO32 **(Note 4)**
SP21	TscR	SCK1 Output Rise Time	—	—	—	ns	See Parameter DO31 **(Note 4)**
SP30	TdoF	SDO1 Data Output Fall Time	—	—	—	ns	See Parameter DO32 **(Note 4)**
SP31	TdoR	SDO1 Data Output Rise Time	—	—	—	ns	See Parameter DO31 **(Note 4)**
SP35	TscH2doV, TscL2doV	SDO1 Data Output Valid after SCK1 Edge	—	6	20	ns	
SP36	TdoV2scH, TdoV2scL	SDO1 Data Output Setup to First SCK1 Edge	30	—	—	ns	
SP40	TdiV2scH, TdiV2scL	Setup Time of SDI1 Data Input to SCK1 Edge	30	—	—	ns	
SP41	TscH2diL, TscL2diL	Hold Time of SDI1 Data Input to SCK1 Edge	30	—	—	ns	

Note 1: These parameters are characterized, but are not tested in manufacturing.

2: Data in "Typical" column is at 3.3V, +25°C unless otherwise stated.

3: The minimum clock period for SCK1 is 100 ns. The clock generated in Master mode must not violate this specification.

4: Assumes 50 pF load on all SPI1 pins.

FIGURE 30-27: **SPI1 SLAVE MODE (FULL-DUPLEX, CKE = 1, CKP = 1, SMP = 0) TIMING CHARACTERISTICS**

NOTES: