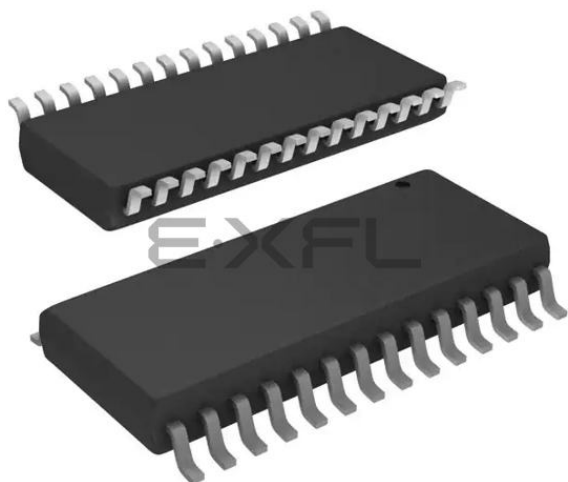




Welcome to E-XFL.COM

What is "[Embedded - Microcontrollers](#)"?

"[Embedded - Microcontrollers](#)" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "[Embedded - Microcontrollers](#)"

Details

Product Status	Active
Core Processor	PIC
Core Size	16-Bit
Speed	60 MIPs
Connectivity	I ² C, IrDA, LINbus, QEI, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, DMA, Motor Control PWM, POR, PWM, WDT
Number of I/O	21
Program Memory Size	32KB (10.7K x 24)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	2K x 16
Voltage - Supply (Vcc/Vdd)	3V ~ 3.6V
Data Converters	A/D 6x10b/12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 125°C (TA)
Mounting Type	Surface Mount
Package / Case	28-SOIC (0.295", 7.50mm Width)
Supplier Device Package	28-SOIC
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/pic24ep32mc202-e-so

Referenced Sources

This device data sheet is based on the following individual chapters of the “*dsPIC33/PIC24 Family Reference Manual*”. These documents should be considered as the general reference for the operation of a particular module or device feature.

Note 1: To access the documents listed below, browse to the documentation section of the dsPIC33EP64MC506 product page of the Microchip web site (www.microchip.com) or select a family reference manual section from the following list.

In addition to parameters, features and other documentation, the resulting page provides links to the related family reference manual sections.

- “**Introduction**” (DS70573)
- “**CPU**” (DS70359)
- “**Data Memory**” (DS70595)
- “**Program Memory**” (DS70613)
- “**Flash Programming**” (DS70609)
- “**Interrupts**” (DS70600)
- “**Oscillator**” (DS70580)
- “**Reset**” (DS70602)
- “**Watchdog Timer and Power-Saving Modes**” (DS70615)
- “**I/O Ports**” (DS70598)
- “**Timers**” (DS70362)
- “**Input Capture**” (DS70352)
- “**Output Compare**” (DS70358)
- “**High-Speed PWM**” (DS70645)
- “**Quadrature Encoder Interface (QEI)**” (DS70601)
- “**Analog-to-Digital Converter (ADC)**” (DS70621)
- “**UART**” (DS70582)
- “**Serial Peripheral Interface (SPI)**” (DS70569)
- “**Inter-Integrated Circuit (I²C™)**” (DS70330)
- “**Enhanced Controller Area Network (ECAN™)**” (DS70353)
- “**Direct Memory Access (DMA)**” (DS70348)
- “**CodeGuard™ Security**” (DS70634)
- “**Programming and Diagnostics**” (DS70608)
- “**Op Amp/Comparator**” (DS70357)
- “**Programmable Cyclic Redundancy Check (CRC)**” (DS70346)
- “**Device Configuration**” (DS70618)
- “**Peripheral Trigger Generator (PTG)**” (DS70669)
- “**Charge Time Measurement Unit (CTMU)**” (DS70661)

TABLE 4-2: CPU CORE REGISTER MAP FOR PIC24EPXXXGP/MC20X DEVICES ONLY

File Name	Addr.	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	All Resets	
W0	0000	W0 (WREG)																XXXX	
W1	0002	W1																XXXX	
W2	0004	W2																XXXX	
W3	0006	W3																XXXX	
W4	0008	W4																XXXX	
W5	000A	W5																XXXX	
W6	000C	W6																XXXX	
W7	000E	W7																XXXX	
W8	0010	W8																XXXX	
W9	0012	W9																XXXX	
W10	0014	W10																XXXX	
W11	0016	W11																XXXX	
W12	0018	W12																XXXX	
W13	001A	W13																XXXX	
W14	001C	W14																XXXX	
W15	001E	W15																XXXX	
SPLIM	0020	SPLIM<15:0>																0000	
PCL	002E	PCL<15:1>																—	0000
PCH	0030	—	—	—	—	—	—	—	—	—	PCH<6:0>							0000	
DSRPAG	0032	—	—	—	—	—	—	DSRPAG<9:0>										0001	
DSWPAG	0034	—	—	—	—	—	—	—	DSWPAG<8:0>										0001
RCOUNT	0036	RCOUNT<15:0>																0000	
SR	0042	—	—	—	—	—	—	—	DC	IPL2	IPL1	IPL0	RA	N	OV	Z	C	0000	
CORCON	0044	VAR	—	—	—	—	—	—	—	—	—	—	—	IPL3	SFA	—	—	0020	
DISICNT	0052	—	—	DISICNT<13:0>														0000	
TBLPAG	0054	—	—	—	—	—	—	—	—	TBLPAG<7:0>									0000
MSTRPR	0058	MSTRPR<15:0>																0000	

Legend: x = unknown value on Reset, — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

TABLE 4-46: PORTA REGISTER MAP FOR PIC24EPXXXGP/MC206 AND dsPIC33EPXXXGP/MC206/506 DEVICES ONLY

File Name	Addr.	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	All Resets
TRISA	0E00	—	—	—	TRISA12	TRISA11	TRISA10	TRISA9	TRISA8	TRISA7	—	—	TRISA4	—	—	TRISA1	TRISA0	1F93
PORTA	0E02	—	—	—	RA12	RA11	RA10	RA9	RA8	RA7	—	—	RA4	—	—	RA1	RA0	0000
LATA	0E04	—	—	—	LATA12	LATA11	LATA10	LATA9	LATA8	LATA7	—	—	LATA4	—	—	LA1TA1	LA0TA0	0000
ODCA	0E06	—	—	—	ODCA12	ODCA11	ODCA10	ODCA9	ODCA8	ODCA7	—	—	ODCA4	—	—	ODCA1	ODCA0	0000
CNENA	0E08	—	—	—	CNIEA12	CNIEA11	CNIEA10	CNIEA9	CNIEA8	CNIEA7	—	—	CNIEA4	—	—	CNIEA1	CNIEA0	0000
CNPUA	0E0A	—	—	—	CNPUA12	CNPUA11	CNPUA10	CNPUA9	CNPUA8	CNPUA7	—	—	CNPUA4	—	—	CNPUA1	CNPUA0	0000
CNPDA	0E0C	—	—	—	CNPDA12	CNPDA11	CNPDA10	CNPDA9	CNPDA8	CNPDA7	—	—	CNPDA4	—	—	CNPDA1	CNPDA0	0000
ANSELA	0E0E	—	—	—	ANSA12	ANSA11	—	—	—	—	—	—	ANSA4	—	—	ANSA1	ANSA0	1813

Legend: — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

TABLE 4-47: PORTB REGISTER MAP FOR PIC24EPXXXGP/MC206 AND dsPIC33EPXXXGP/MC206/506 DEVICES ONLY

File Name	Addr.	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	All Resets
TRISB	0E10	TRISB15	TRISB14	TRISB13	TRISB12	TRISB11	TRISB10	TRISB9	TRISB8	TRISB7	TRISB6	TRISB5	TRISB4	TRISB3	TRISB2	TRISB1	TRISB0	FFFF
PORTB	0E12	RB15	RB14	RB13	RB12	RB11	RB10	RB9	RB8	RB7	RB6	RB5	RB4	RB3	RB2	RB1	RB0	xxxx
LATB	0E14	LATB15	LATB14	LATB13	LATB12	LATB11	LATB10	LATB9	LATB8	LATB7	LATB6	LATB5	LATB4	LATB3	LATB2	LATB1	LATB0	xxxx
ODCB	0E16	ODCB15	ODCB14	ODCB13	ODCB12	ODCB11	ODCB10	ODCB9	ODCB8	ODCB7	ODCB6	ODCB5	ODCB4	ODCB3	ODCB2	ODCB1	ODCB0	0000
CNENB	0E18	CNIEB15	CNIEB14	CNIEB13	CNIEB12	CNIEB11	CNIEB10	CNIEB9	CNIEB8	CNIEB7	CNIEB6	CNIEB5	CNIEB4	CNIEB3	CNIEB2	CNIEB1	CNIEB0	0000
CNPUB	0E1A	CNPUB15	CNPUB14	CNPUB13	CNPUB12	CNPUB11	CNPUB10	CNPUB9	CNPUB8	CNPUB7	CNPUB6	CNPUB5	CNPUB4	CNPUB3	CNPUB2	CNPUB1	CNPUB0	0000
CNPDB	0E1C	CNPDB15	CNPDB14	CNPDB13	CNPDB12	CNPDB11	CNPDB10	CNPDB9	CNPDB8	CNPDB7	CNPDB6	CNPDB5	CNPDB4	CNPDB3	CNPDB2	CNPDB1	CNPDB0	0000
ANSELB	0E1E	—	—	—	—	—	—	—	ANSB8	—	—	—	—	ANSB3	ANSB2	ANSB1	ANSB0	010F

Legend: x = unknown value on Reset, — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

TABLE 4-48: PORTC REGISTER MAP FOR PIC24EPXXXGP/MC206 AND dsPIC33EPXXXGP/MC206/506 DEVICES ONLY

File Name	Addr.	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	All Resets
TRISC	0E20	TRISC15	—	TRISC13	TRISC12	TRISC11	TRISC10	TRISC9	TRISC8	TRISC7	TRISC6	TRISC5	TRISC4	TRISC3	TRISC2	TRISC1	TRISC0	BFFF
PORTC	0E22	RC15	—	RC13	RC12	RC11	RC10	RC9	RC8	RC7	RC6	RC5	RC4	RC3	RC2	RC1	RC0	xxxx
LATC	0E24	LATC15	—	LATC13	LATC12	LATC11	LATC10	LATC9	LATC8	LATC7	LATC6	LATC5	LATC4	LATC3	LATC2	LATC1	LATC0	xxxx
ODCC	0E26	ODCC15	—	ODCC13	ODCC12	ODCC11	ODCC10	ODCC9	ODCC8	ODCC7	ODCC6	ODCC5	ODCC4	ODCC3	ODCC2	ODCC1	ODCC0	0000
CNENC	0E28	CNIEC15	—	CNIEC13	CNIEC12	CNIEC11	CNIEC10	CNIEC9	CNIEC8	CNIEC7	CNIEC6	CNIEC5	CNIEC4	CNIEC3	CNIEC2	CNIEC1	CNIEC0	0000
CNPUC	0E2A	CNPUC15	—	CNPUC13	CNPUC12	CNPUC11	CNPUC10	CNPUC9	CNPUC8	CNPUC7	CNPUC6	CNPUC5	CNPUC4	CNPUC3	CNPUC2	CNPUC1	CNPUC0	0000
CNPDC	0E2C	CNPDC15	—	CNPDC13	CNPDC12	CNPDC11	CNPDC10	CNPDC9	CNPDC8	CNPDC7	CNPDC6	CNPDC5	CNPDC4	CNPDC3	CNPDC2	CNPDC1	CNPDC0	0000
ANSELC	0E2E	—	—	—	—	ANSC11	—	—	—	—	—	—	—	—	ANSC2	ANSC1	ANSC0	0807

Legend: x = unknown value on Reset, — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

REGISTER 8-3: DMAxSTAH: DMA CHANNEL x START ADDRESS REGISTER A (HIGH)

U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
—	—	—	—	—	—	—	—
bit 15				bit 8			

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
STA<23:16>							
bit 7				bit 0			

Legend:

R = Readable bit W = Writable bit U = Unimplemented bit, read as '0'
-n = Value at POR '1' = Bit is set '0' = Bit is cleared x = Bit is unknown

bit 15-8 **Unimplemented:** Read as '0'
bit 7-0 **STA<23:16>:** Primary Start Address bits (source or destination)

REGISTER 8-4: DMAxSTAL: DMA CHANNEL x START ADDRESS REGISTER A (LOW)

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
STA<15:8>							
bit 15				bit 8			

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
STA<7:0>							
bit 7				bit 0			

Legend:

R = Readable bit W = Writable bit U = Unimplemented bit, read as '0'
-n = Value at POR '1' = Bit is set '0' = Bit is cleared x = Bit is unknown

bit 15-0 **STA<15:0>:** Primary Start Address bits (source or destination)

REGISTER 9-1: OSCCON: OSCILLATOR CONTROL REGISTER⁽¹⁾ (CONTINUED)

bit 4	Unimplemented: Read as '0'
bit 3	CF: Clock Fail Detect bit ⁽³⁾ 1 = FSCM has detected clock failure 0 = FSCM has not detected clock failure
bit 2-1	Unimplemented: Read as '0'
bit 0	OSWEN: Oscillator Switch Enable bit 1 = Requests oscillator switch to selection specified by the NOSC<2:0> bits 0 = Oscillator switch is complete

- Note 1:** Writes to this register require an unlock sequence. Refer to “**Oscillator**” (DS70580) in the “*dsPIC33/PIC24 Family Reference Manual*” (available from the Microchip web site) for details.
- 2:** Direct clock switches between any primary oscillator mode with PLL and FRCPLL mode are not permitted. This applies to clock switches in either direction. In these instances, the application must switch to FRC mode as a transitional clock source between the two PLL modes.
- 3:** This bit should only be cleared in software. Setting the bit in software (= 1) will have the same effect as an actual oscillator failure and trigger an oscillator failure trap.

REGISTER 9-4: OSCTUN: FRC OSCILLATOR TUNING REGISTER

U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
—	—	—	—	—	—	—	—
bit 15							bit 8

U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
—	—	TUN5	TUN4	TUN3	TUN2	TUN1	TUN0
bit 7							bit 0

Legend:

R = Readable bit

W = Writable bit

U = Unimplemented bit, read as '0'

-n = Value at POR

'1' = Bit is set

'0' = Bit is cleared

x = Bit is unknown

bit 15-6

Unimplemented: Read as '0'

bit 5-0

TUN<5:0>: FRC Oscillator Tuning bits

011111 = Maximum frequency deviation of 1.453% (7.477 MHz)

011110 = Center frequency + 1.406% (7.474 MHz)

• • •

000001 = Center frequency + 0.047% (7.373 MHz)

000000 = Center frequency (7.37 MHz nominal)

111111 = Center frequency – 0.047% (7.367 MHz)

• • •

100001 = Center frequency – 1.453% (7.263 MHz)

100000 = Minimum frequency deviation of -1.5% (7.259 MHz)

REGISTER 11-5: RPINR8: PERIPHERAL PIN SELECT INPUT REGISTER 8

U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
—	IC4R<6:0>						
bit 15							bit 8

U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
—	IC3R<6:0>						
bit 7							bit 0

Legend:

R = Readable bit W = Writable bit U = Unimplemented bit, read as '0'
-n = Value at POR '1' = Bit is set '0' = Bit is cleared x = Bit is unknown

bit 15 **Unimplemented:** Read as '0'

bit 14-8 **IC4R<6:0>:** Assign Input Capture 4 (IC4) to the Corresponding RPn Pin bits
(see Table 11-2 for input pin selection numbers)

1111001 = Input tied to RPI121

.

.

.

0000001 = Input tied to CMP1

0000000 = Input tied to Vss

bit 7 **Unimplemented:** Read as '0'

bit 6-0 **IC3R<6:0>:** Assign Input Capture 3 (IC3) to the Corresponding RPn Pin bits
(see Table 11-2 for input pin selection numbers)

1111001 = Input tied to RPI121

.

.

.

0000001 = Input tied to CMP1

0000000 = Input tied to Vss

REGISTER 11-20: RPOR2: PERIPHERAL PIN SELECT OUTPUT REGISTER 2

U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
—	—	RP39R<5:0>					
bit 15							bit 8

U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
—	—	RP38R<5:0>					
bit 7							bit 0

Legend:

R = Readable bit W = Writable bit U = Unimplemented bit, read as '0'
-n = Value at POR '1' = Bit is set '0' = Bit is cleared x = Bit is unknown

- bit 15-14 **Unimplemented:** Read as '0'
- bit 13-8 **RP39R<5:0>:** Peripheral Output Function is Assigned to RP39 Output Pin bits
(see Table 11-3 for peripheral function numbers)
- bit 7-6 **Unimplemented:** Read as '0'
- bit 5-0 **RP38R<5:0>:** Peripheral Output Function is Assigned to RP38 Output Pin bits
(see Table 11-3 for peripheral function numbers)

REGISTER 11-21: RPOR3: PERIPHERAL PIN SELECT OUTPUT REGISTER 3

U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
—	—	RP41R<5:0>					
bit 15							bit 8

U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
—	—	RP40R<5:0>					
bit 7							bit 0

Legend:

R = Readable bit W = Writable bit U = Unimplemented bit, read as '0'
-n = Value at POR '1' = Bit is set '0' = Bit is cleared x = Bit is unknown

- bit 15-14 **Unimplemented:** Read as '0'
- bit 13-8 **RP41R<5:0>:** Peripheral Output Function is Assigned to RP41 Output Pin bits
(see Table 11-3 for peripheral function numbers)
- bit 7-6 **Unimplemented:** Read as '0'
- bit 5-0 **RP40R<5:0>:** Peripheral Output Function is Assigned to RP40 Output Pin bits
(see Table 11-3 for peripheral function numbers)

REGISTER 24-12: PTGQPTR: PTG STEP QUEUE POINTER REGISTER⁽¹⁾

U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
—	—	—	—	—	—	—	—
bit 15							bit 8

U-0	U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
—	—	—	PTGQPTR<4:0>				
bit 7							bit 0

Legend:

R = Readable bit

W = Writable bit

U = Unimplemented bit, read as '0'

-n = Value at POR

'1' = Bit is set

'0' = Bit is cleared

x = Bit is unknown

bit 15-5 **Unimplemented:** Read as '0'bit 4-0 **PTGQPTR<4:0>:** PTG Step Queue Pointer Register bits

This register points to the currently active Step command in the Step queue.

Note 1: This register is read-only when the PTG module is executing Step commands (PTGEN = 1 and PTGSTRT = 1).

REGISTER 24-13: PTGQUEX: PTG STEP QUEUE REGISTER x (x = 0-7)^(1,3)

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
STEP(2x + 1)<7:0> ⁽²⁾							
bit 15							bit 8

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
STEP(2x)<7:0> ⁽²⁾							
bit 7							bit 0

Legend:

R = Readable bit

W = Writable bit

U = Unimplemented bit, read as '0'

-n = Value at POR

'1' = Bit is set

'0' = Bit is cleared

x = Bit is unknown

bit 15-8 **STEP(2x + 1)<7:0>:** PTG Step Queue Pointer Register bits⁽²⁾

A queue location for storage of the STEP(2x + 1) command byte.

bit 7-0 **STEP(2x)<7:0>:** PTG Step Queue Pointer Register bits⁽²⁾

A queue location for storage of the STEP(2x) command byte.

Note 1: This register is read-only when the PTG module is executing Step commands (PTGEN = 1 and PTGSTRT = 1).

2: Refer to Table 24-1 for the Step command encoding.

3: The Step registers maintain their values on any type of Reset.

27.0 SPECIAL FEATURES

Note: This data sheet summarizes the features of the dsPIC33EPXXXGP50X, dsPIC33EPXXXMC20X/50X and PIC24EPXXXGP/MC20X families of devices. It is not intended to be a comprehensive reference source. To complement the information in this data sheet, refer to the related section of the “dsPIC33/PIC24 Family Reference Manual”, which is available from the Microchip web site (www.microchip.com).

dsPIC33EPXXXGP50X, dsPIC33EPXXXMC20X/50X and PIC24EPXXXGP/MC20X devices include several features intended to maximize application flexibility and reliability, and minimize cost through elimination of external components. These are:

- Flexible Configuration
- Watchdog Timer (WDT)
- Code Protection and CodeGuard™ Security
- JTAG Boundary Scan Interface
- In-Circuit Serial Programming™ (ICSP™)
- In-Circuit Emulation

27.1 Configuration Bits

In dsPIC33EPXXXGP50X, dsPIC33EPXXXMC20X/50X and PIC24EPXXXGP/MC20X devices, the Configuration bytes are implemented as volatile memory. This means that configuration data must be programmed each time the device is powered up. Configuration data is stored in at the top of the on-chip program memory space, known as the Flash Configuration bytes. Their specific locations are shown in Table 27-1. The configuration data is automatically loaded from the Flash Configuration bytes to the proper Configuration Shadow registers during device Resets.

Note: Configuration data is reloaded on all types of device Resets.

When creating applications for these devices, users should always specifically allocate the location of the Flash Configuration bytes for configuration data in their code for the compiler. This is to make certain that program code is not stored in this address when the code is compiled.

The upper 2 bytes of all Flash Configuration Words in program memory should always be ‘1111 1111 1111 1111’. This makes them appear to be NOP instructions in the remote event that their locations are ever executed by accident. Since Configuration bits are not implemented in the corresponding locations, writing ‘1’s to these locations has no effect on device operation.

Note: Performing a page erase operation on the last page of program memory clears the Flash Configuration bytes, enabling code protection as a result. Therefore, users should avoid performing page erase operations on the last page of program memory.

The Configuration Flash bytes map is shown in Table 27-1.

30.0 ELECTRICAL CHARACTERISTICS

This section provides an overview of dsPIC33EPXXXGP50X, dsPIC33EPXXXMC20X/50X and PIC24EPXXXGP/MC20X electrical characteristics. Additional information will be provided in future revisions of this document as it becomes available.

Absolute maximum ratings for the dsPIC33EPXXXGP50X, dsPIC33EPXXXMC20X/50X and PIC24EPXXXGP/MC20X family are listed below. Exposure to these maximum rating conditions for extended periods may affect device reliability. Functional operation of the device at these or any other conditions above the parameters indicated in the operation listings of this specification is not implied.

Absolute Maximum Ratings⁽¹⁾

Ambient temperature under bias	-40°C to +125°C
Storage temperature	-65°C to +150°C
Voltage on VDD with respect to VSS	-0.3V to +4.0V
Voltage on any pin that is not 5V tolerant, with respect to VSS ⁽³⁾	-0.3V to (VDD + 0.3V)
Voltage on any 5V tolerant pin with respect to VSS when VDD ≥ 3.0V ⁽³⁾	-0.3V to +5.5V
Voltage on any 5V tolerant pin with respect to VSS when VDD < 3.0V ⁽³⁾	-0.3V to +3.6V
Maximum current out of VSS pin	300 mA
Maximum current into VDD pin ⁽²⁾	300 mA
Maximum current sunk/sourced by any 4x I/O pin	15 mA
Maximum current sunk/sourced by any 8x I/O pin	25 mA
Maximum current sunk by all ports ^(2,4)	200 mA

Note 1: Stresses above those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only, and functional operation of the device at those or any other conditions above those indicated in the operation listings of this specification is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

2: Maximum allowable current is a function of device maximum power dissipation (see Table 30-2).

3: See the “Pin Diagrams” section for the 5V tolerant pins.

4: Exceptions are: dsPIC33EPXXXGP502, dsPIC33EPXXXMC202/502 and PIC24EPXXXGP/MC202 devices, which have a maximum sink/source capability of 130 mA.

TABLE 30-11: DC CHARACTERISTICS: I/O PIN INPUT SPECIFICATIONS (CONTINUED)

DC CHARACTERISTICS			Standard Operating Conditions: 3.0V to 3.6V (unless otherwise stated) Operating temperature $-40^{\circ}\text{C} \leq T_A \leq +85^{\circ}\text{C}$ for Industrial $-40^{\circ}\text{C} \leq T_A \leq +125^{\circ}\text{C}$ for Extended				
Param No.	Symbol	Characteristic	Min.	Typ.	Max.	Units	Conditions
DI60a	I _{ICL}	Input Low Injection Current	0	—	-5 ^(4,7)	mA	All pins except V _{DD} , V _{SS} , AV _{DD} , AV _{SS} , MCLR, VCAP and RB7
DI60b	I _{ICH}	Input High Injection Current	0	—	+5 ^(5,6,7)	mA	All pins except V _{DD} , V _{SS} , AV _{DD} , AV _{SS} , MCLR, VCAP, RB7 and all 5V tolerant pins ⁽⁶⁾
DI60c	ΣI_{ICT}	Total Input Injection Current (sum of all I/O and control pins)	-20 ⁽⁸⁾	—	+20 ⁽⁸⁾	mA	Absolute instantaneous sum of all $\pm$ input injection currents from all I/O pins ($ I_{ICL} + I_{ICH} $) $\leq \Sigma I_{ICT}$

- Note 1:** The leakage current on the MCLR pin is strongly dependent on the applied voltage level. The specified levels represent normal operating conditions. Higher leakage current can be measured at different input voltages.
- 2:** Negative current is defined as current sourced by the pin.
- 3:** See the “Pin Diagrams” section for the 5V tolerant I/O pins.
- 4:** V_{IL} source < (V_{SS} – 0.3). Characterized but not tested.
- 5:** Non-5V tolerant pins V_{IH} source > (V_{DD} + 0.3), 5V tolerant pins V_{IH} source > 5.5V. Characterized but not tested.
- 6:** Digital 5V tolerant pins cannot tolerate any “positive” input injection current from input sources > 5.5V.
- 7:** Non-zero injection currents can affect the ADC results by approximately 4-6 counts.
- 8:** Any number and/or combination of I/O pins not excluded under I_{ICL} or I_{ICH} conditions are permitted provided the mathematical “absolute instantaneous” sum of the input injection currents from all pins do not exceed the specified limit. Characterized but not tested.

FIGURE 30-29: SPI1 SLAVE MODE (FULL-DUPLEX, CKE = 0, CKP = 0, SMP = 0)
TIMING CHARACTERISTICS

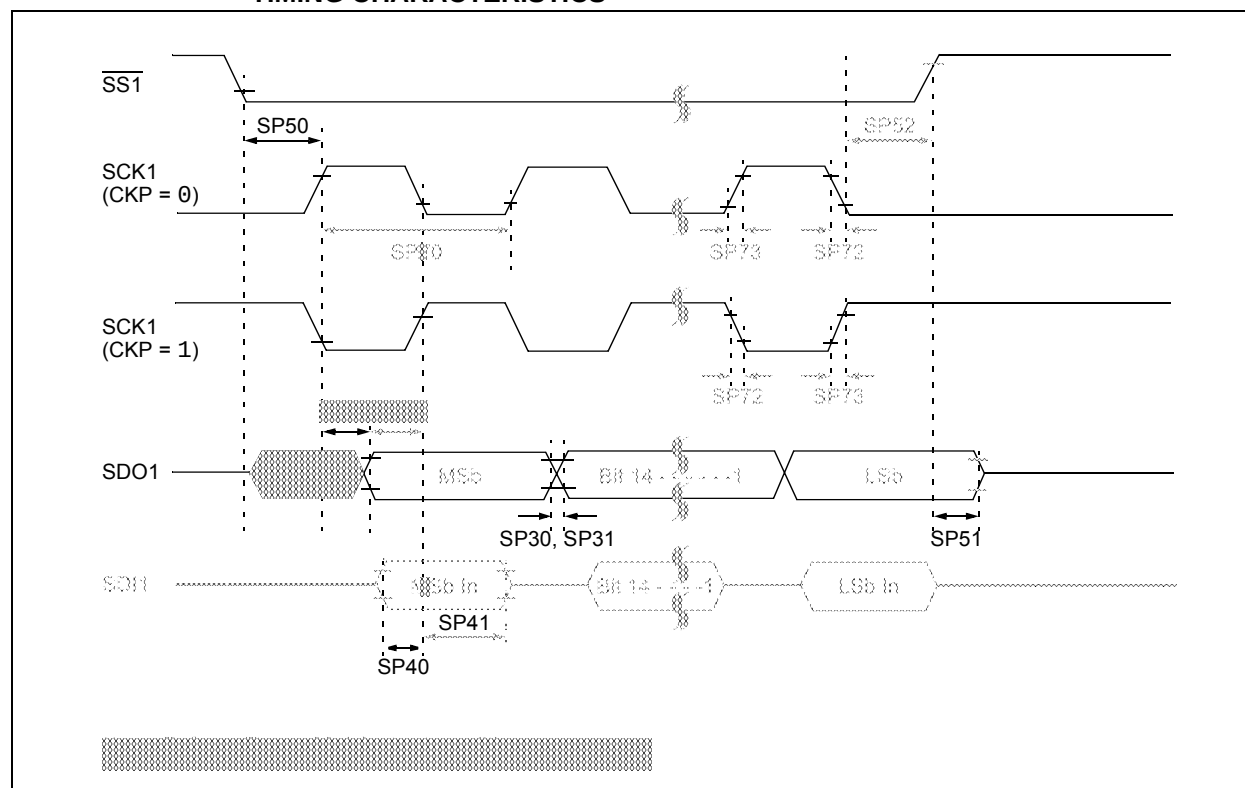


TABLE 30-49: I2Cx BUS DATA TIMING REQUIREMENTS (MASTER MODE)

AC CHARACTERISTICS				Standard Operating Conditions: 3.0V to 3.6V (unless otherwise stated) Operating temperature $-40^{\circ}\text{C} \leq T_A \leq +85^{\circ}\text{C}$ for Industrial $-40^{\circ}\text{C} \leq T_A \leq +125^{\circ}\text{C}$ for Extended			
Param No.	Symbol	Characteristic ⁽⁴⁾		Min. ⁽¹⁾	Max.	Units	Conditions
IM10	TLO:SCL	Clock Low Time	100 kHz mode	$T_{CY}/2$ (BRG + 2)	—	μs	
			400 kHz mode	$T_{CY}/2$ (BRG + 2)	—	μs	
			1 MHz mode ⁽²⁾	$T_{CY}/2$ (BRG + 2)	—	μs	
IM11	THI:SCL	Clock High Time	100 kHz mode	$T_{CY}/2$ (BRG + 2)	—	μs	
			400 kHz mode	$T_{CY}/2$ (BRG + 2)	—	μs	
			1 MHz mode ⁽²⁾	$T_{CY}/2$ (BRG + 2)	—	μs	
IM20	TF:SCL	SDAx and SCLx Fall Time	100 kHz mode	—	300	ns	Cb is specified to be from 10 to 400 pF
			400 kHz mode	$20 + 0.1 C_b$	300	ns	
			1 MHz mode ⁽²⁾	—	100	ns	
IM21	TR:SCL	SDAx and SCLx Rise Time	100 kHz mode	—	1000	ns	Cb is specified to be from 10 to 400 pF
			400 kHz mode	$20 + 0.1 C_b$	300	ns	
			1 MHz mode ⁽²⁾	—	300	ns	
IM25	TSU:DAT	Data Input Setup Time	100 kHz mode	250	—	ns	
			400 kHz mode	100	—	ns	
			1 MHz mode ⁽²⁾	40	—	ns	
IM26	THD:DAT	Data Input Hold Time	100 kHz mode	0	—	μs	
			400 kHz mode	0	0.9	μs	
			1 MHz mode ⁽²⁾	0.2	—	μs	
IM30	TSU:STA	Start Condition Setup Time	100 kHz mode	$T_{CY}/2$ (BRG + 2)	—	μs	Only relevant for Repeated Start condition
			400 kHz mode	$T_{CY}/2$ (BRG + 2)	—	μs	
			1 MHz mode ⁽²⁾	$T_{CY}/2$ (BRG + 2)	—	μs	
IM31	THD:STA	Start Condition Hold Time	100 kHz mode	$T_{CY}/2$ (BRG + 2)	—	μs	After this period, the first clock pulse is generated
			400 kHz mode	$T_{CY}/2$ (BRG + 2)	—	μs	
			1 MHz mode ⁽²⁾	$T_{CY}/2$ (BRG + 2)	—	μs	
IM33	TSU:STO	Stop Condition Setup Time	100 kHz mode	$T_{CY}/2$ (BRG + 2)	—	μs	
			400 kHz mode	$T_{CY}/2$ (BRG + 2)	—	μs	
			1 MHz mode ⁽²⁾	$T_{CY}/2$ (BRG + 2)	—	μs	
IM34	THD:STO	Stop Condition Hold Time	100 kHz mode	$T_{CY}/2$ (BRG + 2)	—	μs	
			400 kHz mode	$T_{CY}/2$ (BRG + 2)	—	μs	
			1 MHz mode ⁽²⁾	$T_{CY}/2$ (BRG + 2)	—	μs	
IM40	TAA:SCL	Output Valid From Clock	100 kHz mode	—	3500	ns	
			400 kHz mode	—	1000	ns	
			1 MHz mode ⁽²⁾	—	400	ns	
IM45	TBF:SDA	Bus Free Time	100 kHz mode	4.7	—	μs	Time the bus must be free before a new transmission can start
			400 kHz mode	1.3	—	μs	
			1 MHz mode ⁽²⁾	0.5	—	μs	
IM50	CB	Bus Capacitive Loading		—	400	pF	
IM51	TPGD	Pulse Gobbler Delay		65	390	ns	(Note 3)

Note 1: BRG is the value of the I²C™ Baud Rate Generator. Refer to “Inter-Integrated Circuit (I²C™)” (DS70330) in the “dsPIC33/PIC24 Family Reference Manual”. Please see the Microchip web site for the latest family reference manual sections.

2: Maximum pin capacitance = 10 pF for all I2Cx pins (for 1 MHz mode only).

3: Typical value for this parameter is 130 ns.

4: These parameters are characterized, but not tested in manufacturing.

31.2 AC Characteristics and Timing Parameters

The information contained in this section defines dsPIC33EPXXXGP50X, dsPIC33EPXXXMC20X/50X and PIC24EPXXXGP/MC20X AC characteristics and timing parameters for high-temperature devices. However, all AC timing specifications in this section are the same as those in **Section 30.2 “AC Characteristics and Timing Parameters”**, with the exception of the parameters listed in this section.

Parameters in this section begin with an H, which denotes High temperature. For example, Parameter OS53 in **Section 30.2 “AC Characteristics and Timing Parameters”** is the Industrial and Extended temperature equivalent of HOS53.

TABLE 31-9: TEMPERATURE AND VOLTAGE SPECIFICATIONS – AC

AC CHARACTERISTICS	Standard Operating Conditions: 3.0V to 3.6V (unless otherwise stated) Operating temperature $-40^{\circ}\text{C} \leq T_A \leq +150^{\circ}\text{C}$ Operating voltage VDD range as described in Table 31-1.
--------------------	---

FIGURE 31-1: LOAD CONDITIONS FOR DEVICE TIMING SPECIFICATIONS

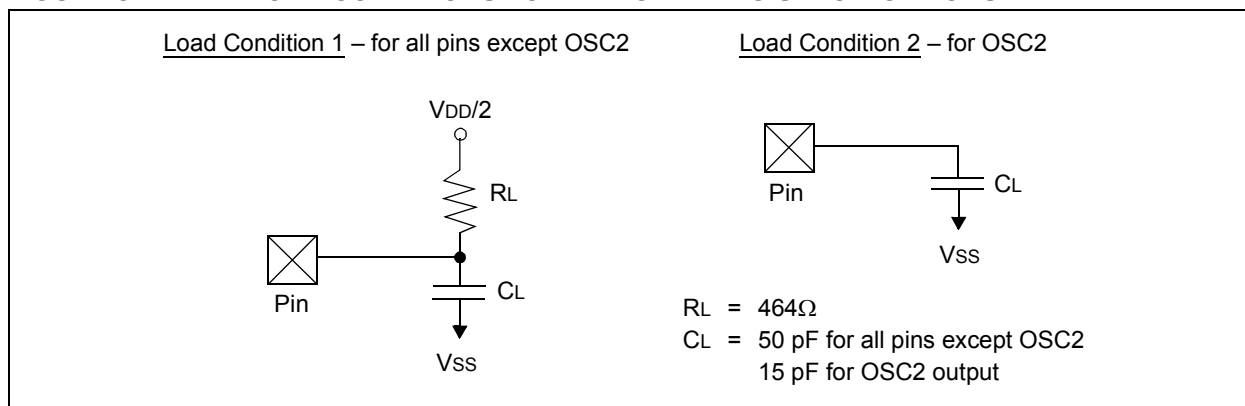


TABLE 31-10: PLL CLOCK TIMING SPECIFICATIONS

AC CHARACTERISTICS			Standard Operating Conditions: 3.0V to 3.6V (unless otherwise stated) Operating temperature $-40^{\circ}\text{C} \leq T_A \leq +150^{\circ}\text{C}$				
Param No.	Symbol	Characteristic	Min	Typ	Max	Units	Conditions
HOS53	DCLK	CLKO Stability (Jitter) ⁽¹⁾	-5	0.5	5	%	Measured over 100 ms period

Note 1: These parameters are characterized by similarity, but are not tested in manufacturing. This specification is based on clock cycle by clock cycle measurements. To calculate the effective jitter for individual time bases or communication clocks use this formula:

$$\text{Peripheral Clock Jitter} = \frac{DCLK}{\sqrt{\left(\frac{FOSC}{\text{Peripheral Bit Rate Clock}}\right)}}$$

For example: FOSC = 32 MHz, DCLK = 5%, SPIx bit rate clock (i.e., SCKx) is 2 MHz.

$$\text{SPI SCK Jitter} = \left[\frac{DCLK}{\sqrt{\left(\frac{32 \text{ MHz}}{2 \text{ MHz}}\right)}} \right] = \left[\frac{5\%}{\sqrt{16}} \right] = \left[\frac{5\%}{4} \right] = 1.25\%$$

NOTES:

Revision H (August 2013)

This revision includes minor typographical and formatting changes throughout the text.

Other major changes are referenced by their respective section in Table A-6.

TABLE A-6: MAJOR SECTION UPDATES

Section Name	Update Description
Cover Section	- Adds Peripheral Pin Select (PPS) to allow Digital Function Remapping and Change Notification Interrupts to Input/Output section - Adds heading information to 64-Pin TQFP
Section 4.0 “Memory Organization”	- Corrects Reset values for ANSELE, TRISF, TRISC, ANSELC and TRISA - Corrects address range from 0x2FFF to 0x7FFF - Corrects DSRPAG and DSWPAG (now 3 hex digits) - Changes Call Stack Frame from <15:1> to PC<15:0> - Word length in Figure 4-20 is changed to 50 words for clarity
Section 5.0 “Flash Program Memory”	Corrects descriptions of NVM registers
Section 9.0 “Oscillator Configuration”	- Removes resistor from Figure 9-1 - Adds Fast RC Oscillator with Divide-by-16 (FRCDIV16) row to Table 9-1 - Removes incorrect information from ROI bit in Register 9-2
Section 14.0 “Input Capture”	- Changes 31 user-selectable Trigger/Sync interrupts to 19 user-selectable Trigger/Sync interrupts - Corrects ICTSEL<12:10> bits (now ICTSEL<2:0>)
Section 17.0 “Quadrature Encoder Interface (QEI) Module (dsPIC33EPXXXMC20X/50X and PIC24EPXXXMC20X Devices Only)”	Corrects QCAPEN bit description
Section 19.0 “Inter-Integrated Circuit™ (I²C™)”	Adds note to clarify that 100kbit/sec operation of I²C is not possible at high processor speeds
Section 22.0 “Charge Time Measurement Unit (CTMU)”	Clarifies Figure 22-1 to accurately reflect peripheral behavior
Section 23.0 “10-Bit/12-Bit Analog-to-Digital Converter (ADC)”	Correct Figure 23-1 (changes CH123x to CH123Sx)
Section 24.0 “Peripheral Trigger Generator (PTG) Module”	Adds footnote to Register 24-1 (In order to operate with CVRSS=1, at least one of the comparator modules must be enabled).
Section 25.0 “Op Amp/Comparator Module”	- Adds note to Figure 25-3 (In order to operate with CVRSS=1, at least one of the comparator modules must be enabled) - Adds footnote to Register 25-2 (COE is not available when OPMODE (CMxCON<10>) = 1)
Section 27.0 “Special Features”	Corrects the bit description for FNOSC<2:0>
Section 30.0 “Electrical Characteristics”	- Corrects 512K part power-down currents based on test data - Corrects WDT timing limits based on LPRC oscillator tolerance
Section 31.0 “High-Temperature Electrical Characteristics”	Adds Table 31-5 (DC Characteristics: Idle Current (I_{IDLE}))

ECAN Module	
Control Registers	290
Modes of Operation	289
Overview	287
Resources	289
Electrical Characteristics	401
AC	413, 471
Enhanced CAN (ECAN) Module	287
Equations	
Device Operating Frequency	154
FPLLO Calculation	154
FVCO Calculation	154
Errata	23
F	
Filter Capacitor (CEFC) Specifications	403
Flash Program Memory	119
Control Registers	120
Programming Operations	120
Resources	120
RTSP Operation	120
Table Instructions	119
Flexible Configuration	379
G	
Guidelines for Getting Started	29
Application Examples	32
Basic Connection Requirements	29
CPU Logic Filter Capacitor Connection (VCAP)	30
Decoupling Capacitors	29
External Oscillator Pins	31
ICSP Pins	31
Master Clear (MCLR) Pin	30
Oscillator Value Conditions on Start-up	32
Unused I/Os	32
H	
High-Speed PWM	225
Control Registers	230
Faults	225
Resources	229
High-Temperature Electrical Characteristics	467
Absolute Maximum Ratings	467
I	
I/O Ports	173
Helpful Tips	181
Parallel I/O (PIO)	173
Resources	182
Write/Read Timing	174
In-Circuit Debugger	386
In-Circuit Emulation	379
In-Circuit Serial Programming (ICSP)	379, 386
Input Capture	213
Control Registers	215
Resources	214
Input Change Notification (ICN)	174
Instruction Addressing Modes	112
File Register Instructions	112
Fundamental Modes Supported	112
MAC Instructions	113
MCU Instructions	112
Move and Accumulator Instructions	113
Other Instructions	113

Instruction Set	
Overview	390
Summary	387
Symbols Used in Opcode Descriptions	388
Inter-Integrated Circuit (I ² C)	273
Control Registers	276
Resources	275
Internal RC Oscillator	
Use with WDT	385
Internet Address	524
Interrupt Controller	
Control and Status Registers	131
INTCON1	131
INTCON2	131
INTCON3	131
INTCON4	131
INTTREG	131
Interrupt Vector Details	129
Interrupt Vector Table (IVT)	127
Reset Sequence	127
Resources	131
J	
JTAG Boundary Scan Interface	379
JTAG Interface	386
M	
Memory Maps	
Extended Data Space	109
Memory Organization	45
Resources	62
Microchip Internet Web Site	524
Modulo Addressing	114
Applicability	115
Operation Example	114
Start and End Address	114
W Address Register Selection	114
MPLAB Assembler, Linker, Librarian	398
MPLAB ICD 3 In-Circuit Debugger	399
MPLAB PM3 Device Programmer	399
MPLAB REAL ICE In-Circuit Emulator System	399
MPLAB X Integrated Development	
Environment Software	397
MPLAB X SIM Software Simulator	399
MPLIB Object Librarian	398
MPLINK Object Linker	398
O	
Op Amp	
Application Considerations	358
Configuration A	358
Configuration B	359
Op Amp/Comparator	355
Control Registers	360
Resources	359
Open-Drain Configuration	174
Oscillator	
Control Registers	156
Resources	155
Output Compare	219
Control Registers	221
Resources	220

DMAxSTAH (DMA Channel x Start Address A, High)	144	PTGCST (PTG Control/Status).....	340
DMAxSTAL (DMA Channel x Start Address A, Low)	144	PTGHOLD (PTG Hold)	347
DMAxSTBH (DMA Channel x Start Address B, High)	145	PTGL0 (PTG Literal 0).....	348
DMAxSTBL (DMA Channel x Start Address B, Low)	145	PTGQPTR (PTG Step Queue Pointer)	349
DSADRH (DMA Most Recent RAM High Address)	147	PTGQUEX (PTG Step Queue x)	349
DSADRL (DMA Most Recent RAM Low Address)	147	PTGSDLIM (PTG Step Delay Limit)	346
DTRx (PWMx Dead-Time)	238	PTGT0LIM (PTG Timer0 Limit).....	345
FCLCONx (PWMx Fault Current-Limit Control)	243	PTGT1LIM (PTG Timer1 Limit).....	345
I2CxCON (I2Cx Control)	276	PTPER (PWMx Primary Master Time Base Period).....	233
I2CxMSK (I2Cx Slave Mode Address Mask)	280	PWMCONx (PWMx Control).....	235
I2CxSTAT (I2Cx Status)	278	QE1CON (QE1 Control)	252
ICxCON1 (Input Capture x Control 1)	215	QE1GECH (QE1 Greater Than or Equal Compare High Word).....	262
ICxCON2 (Input Capture x Control 2)	216	QE1GECL (QE1 Greater Than or Equal Compare Low Word)	262
INDX1CNTH (Index Counter 1 High Word)	259	QE1ICH (QE1 Initialization/Capture High Word)	260
INDX1CNTL (Index Counter 1 Low Word)	259	QE1ICL (QE1 Initialization/Capture Low Word)	260
INDX1HLD (Index Counter 1 Hold)	260	QE1IIOC (QE1 I/O Control)	254
INT1HLDH (Interval 1 Timer Hold High Word).....	264	QE1LECH (QE1 Less Than or Equal Compare High Word).....	261
INT1HLDL (Interval 1 Timer Hold Low Word)	264	QE1LECL (QE1 Less Than or Equal Compare Low Word)	261
INT1TMRH (Interval 1 Timer High Word).....	263	QE1STAT (QE1 Status).....	256
INT1TMRL (Interval 1 Timer Low Word).....	263	RCON (Reset Control).....	125
INTCON1 (Interrupt Control 1)	134	REFOCON (Reference Oscillator Control)	162
INTCON2 (Interrupt Control 2)	136	RPINR0 (Peripheral Pin Select Input 0).....	183
INTCON2 (Interrupt Control 3).....	137	RPINR1 (Peripheral Pin Select Input 1).....	184
INTCON4 (Interrupt Control 4).....	137	RPINR11 (Peripheral Pin Select Input 11).....	187
INTTREG (Interrupt Control and Status).....	138	RPINR12 (Peripheral Pin Select Input 12).....	188
IOCONx (PWMx I/O Control)	240	RPINR14 (Peripheral Pin Select Input 14).....	189
LEBCONx (PWMx Leading-Edge Blanking Control)	245	RPINR15 (Peripheral Pin Select Input 15).....	190
LEBDLYx (PWMx Leading-Edge Blanking Delay)	246	RPINR18 (Peripheral Pin Select Input 18).....	191
MDC (PWMx Master Duty Cycle).....	234	RPINR19 (Peripheral Pin Select Input 19).....	191
NVMADRH (Nonvolatile Memory Address High)	122	RPINR22 (Peripheral Pin Select Input 22).....	192
NVMADRL (Nonvolatile Memory Address Low).....	122	RPINR23 (Peripheral Pin Select Input 23).....	193
NVMCON (Nonvolatile Memory (NVM) Control)	121	RPINR26 (Peripheral Pin Select Input 26).....	193
NVMKEY (Nonvolatile Memory Key)	122	RPINR3 (Peripheral Pin Select Input 3).....	184
OCxCON1 (Output Compare x Control 1)	221	RPINR37 (Peripheral Pin Select Input 37).....	194
OCxCON2 (Output Compare x Control 2)	223	RPINR38 (Peripheral Pin Select Input 38).....	195
OSCCON (Oscillator Control)	156	RPINR39 (Peripheral Pin Select Input 39).....	196
OSCTUN (FRC Oscillator Tuning)	161	RPINR7 (Peripheral Pin Select Input 7).....	185
PDCx (PWMx Generator Duty Cycle)	237	RPINR8 (Peripheral Pin Select Input 8).....	186
PHASEx (PWMx Primary Phase-Shift)	237	RPOR0 (Peripheral Pin Select Output 0).....	197
PLLFBF (PLL Feedback Divisor)	160	RPOR1 (Peripheral Pin Select Output 1).....	197
PMD1 (Peripheral Module Disable Control 1)	166	RPOR2 (Peripheral Pin Select Output 2).....	198
PMD2 (Peripheral Module Disable Control 2).....	168	RPOR3 (Peripheral Pin Select Output 3).....	198
PMD3 (Peripheral Module Disable Control 3).....	169	RPOR4 (Peripheral Pin Select Output 4).....	199
PMD4 (Peripheral Module Disable Control 4).....	169	RPOR5 (Peripheral Pin Select Output 5).....	199
PMD6 (Peripheral Module Disable Control 6).....	170	RPOR6 (Peripheral Pin Select Output 6).....	200
PMD7 (Peripheral Module Disable Control 7).....	171	RPOR7 (Peripheral Pin Select Output 7).....	200
POS1CNTH (Position Counter 1 High Word)	258	RPOR8 (Peripheral Pin Select Output 8).....	201
POS1CNTL (Position Counter1 Low Word)	258	RPOR9 (Peripheral Pin Select Output 9).....	201
POS1HLD (Position Counter 1 Hold)	258	SEVTCMP (PWMx Primary Special Event Compare)	233
PTCON (PWMx Time Base Control)	230	SPIxCON1 (SPIx Control 1).....	270
PTCON2 (PWMx Primary Master Clock Divider Select 2).....	232	SPIxCON2 (SPIx Control 2).....	272
PTGADJ (PTG Adjust)	348	SPIxSTAT (SPIx Status and Control)	268
PTGBTE (PTG Broadcast Trigger Enable)	343	SR (CPU STATUS).....	40, 132
PTGC0LIM (PTG Counter 0 Limit)	346	T1CON (Timer1 Control)	205
PTGC1LIM (PTG Counter 1 Limit)	347	TRGCONx (PWMx Trigger Control)	239
PTGCON (PTG Control)	342	TRIGx (PWMx Primary Trigger Compare Value).....	242
		TxCON (Timer2 and Timer4 Control)	210

Note the following details of the code protection feature on Microchip devices:

- Microchip products meet the specification contained in their particular Microchip Data Sheet.
- Microchip believes that its family of products is one of the most secure families of its kind on the market today, when used in the intended manner and under normal conditions.
- There are dishonest and possibly illegal methods used to breach the code protection feature. All of these methods, to our knowledge, require using the Microchip products in a manner outside the operating specifications contained in Microchip's Data Sheets. Most likely, the person doing so is engaged in theft of intellectual property.
- Microchip is willing to work with the customer who is concerned about the integrity of their code.
- Neither Microchip nor any other semiconductor manufacturer can guarantee the security of their code. Code protection does not mean that we are guaranteeing the product as "unbreakable."

Code protection is constantly evolving. We at Microchip are committed to continuously improving the code protection features of our products. Attempts to break Microchip's code protection feature may be a violation of the Digital Millennium Copyright Act. If such acts allow unauthorized access to your software or other copyrighted work, you may have a right to sue for relief under that Act.

Information contained in this publication regarding device applications and the like is provided only for your convenience and may be superseded by updates. It is your responsibility to ensure that your application meets with your specifications. MICROCHIP MAKES NO REPRESENTATIONS OR WARRANTIES OF ANY KIND WHETHER EXPRESS OR IMPLIED, WRITTEN OR ORAL, STATUTORY OR OTHERWISE, RELATED TO THE INFORMATION, INCLUDING BUT NOT LIMITED TO ITS CONDITION, QUALITY, PERFORMANCE, MERCHANTABILITY OR FITNESS FOR PURPOSE. Microchip disclaims all liability arising from this information and its use. Use of Microchip devices in life support and/or safety applications is entirely at the buyer's risk, and the buyer agrees to defend, indemnify and hold harmless Microchip from any and all damages, claims, suits, or expenses resulting from such use. No licenses are conveyed, implicitly or otherwise, under any Microchip intellectual property rights.

Trademarks

The Microchip name and logo, the Microchip logo, dsPIC, FlashFlex, KEELoQ, KEELoQ logo, MPLAB, PIC, PICmicro, PICSTART, PIC³² logo, rPIC, SST, SST Logo, SuperFlash and UNI/O are registered trademarks of Microchip Technology Incorporated in the U.S.A. and other countries.

FilterLab, Hampshire, HI-TECH C, Linear Active Thermistor, MTP, SEEVAL and The Embedded Control Solutions Company are registered trademarks of Microchip Technology Incorporated in the U.S.A.

Silicon Storage Technology is a registered trademark of Microchip Technology Inc. in other countries.

Analog-for-the-Digital Age, Application Maestro, BodyCom, chipKIT, chipKIT logo, CodeGuard, dsPICDEM, dsPICDEM.net, dsPICworks, dsSPEAK, ECAN, ECONOMONITOR, FanSense, HI-TIDE, In-Circuit Serial Programming, ICSP, Mindi, MiWi, MPASM, MPF, MPLAB Certified logo, MPLIB, MPLINK, mTouch, Omniclient Code Generation, PICC, PICC-18, PICDEM, PICDEM.net, PICkit, PICtail, REAL ICE, rLAB, Select Mode, SQL, Serial Quad I/O, Total Endurance, TSHARC, UniWinDriver, WiperLock, ZENA and Z-Scale are trademarks of Microchip Technology Incorporated in the U.S.A. and other countries.

SQTP is a service mark of Microchip Technology Incorporated in the U.S.A.

GestIC and ULPP are registered trademarks of Microchip Technology Germany II GmbH & Co. KG, a subsidiary of Microchip Technology Inc., in other countries.

All other trademarks mentioned herein are property of their respective companies.

© 2011-2013, Microchip Technology Incorporated, Printed in the U.S.A., All Rights Reserved.

Printed on recycled paper.

ISBN: 9781620773949

QUALITY MANAGEMENT SYSTEM
CERTIFIED BY DNV
== ISO/TS 16949 ==

Microchip received ISO/TS-16949:2009 certification for its worldwide headquarters, design and wafer fabrication facilities in Chandler and Tempe, Arizona; Gresham, Oregon and design centers in California and India. The Company's quality system processes and procedures are for its PIC® MCUs and dsPIC® DSCs, KEELoQ® code hopping devices, Serial EEPROMs, microperipherals, nonvolatile memory and analog products. In addition, Microchip's quality system for the design and manufacture of development systems is ISO 9001:2000 certified.