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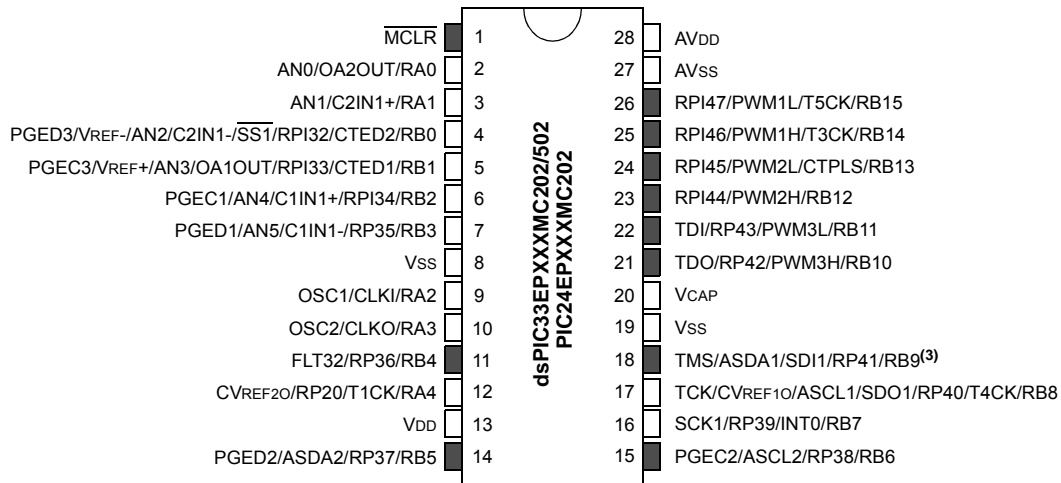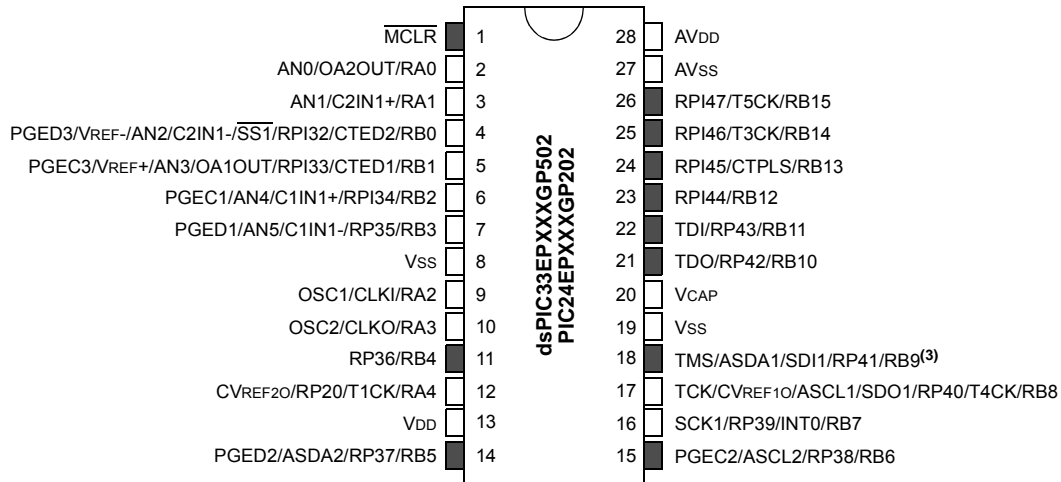
Applications of "<u>Embedded - Microcontrollers</u>"

Details	
Product Status	Active
Core Processor	PIC
Core Size	16-Bit
Speed	60 MIPs
Connectivity	I²C, IrDA, LINbus, QEI, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, DMA, Motor Control PWM, POR, PWM, WDT
Number of I/O	21
Program Memory Size	32KB (10.7K x 24)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	2K x 16
Voltage - Supply (Vcc/Vdd)	3V ~ 3.6V
Data Converters	A/D 6x10b/12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 125°C (TA)
Mounting Type	Through Hole
Package / Case	28-DIP (0.300", 7.62mm)
Supplier Device Package	28-SPDIP
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/pic24ep32mc202-e-sp

Pin Diagrams

28-Pin SPDIP/SOIC/SSOP[1,2]

■ = Pins are up to 5V tolerant

dsPIC33EPXXXGP502
PIC24EPXXXGP202

MCLR	1	28	AVDD
AN0/OA2OUT/RA0	2	27	AVSS
AN1/C2IN1+/RA1	3	26	RPI47/T5CK/RB15
PGED3/VREF-/AN2/C2IN1-/SS1/RPI32/CTED2/RB0	4	25	RPI46/T3CK/RB14
PGEC3/VREF+/AN3/OA1OUT/RPI33/CTED1/RB1	5	24	RPI45/CTPLS/RB13
PGEC1/AN4/C1IN1+/RPI34/RB2	6	23	RPI44/RB12
PGED1/AN5/C1IN1-/RP35/RB3	7	22	TDI/RP43/RB11
VSS	8	21	TDO/RP42/RB10
OSC1/CLKI/RA2	9	20	VCAP
OSC2/CLKO/RA3	10	19	VSS
RP36/RB4	11	18	TMS/ASDA1/SDI1/RP41/RB9[3]
CVREF2O/RP20/T1CK/RA4	12	17	TCK/CVREF1O/ASCL1/SDO1/RP40/T4CK/RB8
VDD	13	16	SCK1/RP39/INT0/RB7
PGED2/ASDA2/RP37/RB5	14	15	PGEC2/ASCL2/RP38/RB6

dsPIC33EPXXXMC202/502
PIC24EPXXXMC202

MCLR	1	28	AVDD
AN0/OA2OUT/RA0	2	27	AVSS
AN1/C2IN1+/RA1	3	26	RPI47/PWM1L/T5CK/RB15
PGED3/VREF-/AN2/C2IN1-/SS1/RPI32/CTED2/RB0	4	25	RPI46/PWM1H/T3CK/RB14
PGEC3/VREF+/AN3/OA1OUT/RPI33/CTED1/RB1	5	24	RPI45/PWM2L/CTPLS/RB13
PGEC1/AN4/C1IN1+/RPI34/RB2	6	23	RPI44/PWM2H/RB12
PGED1/AN5/C1IN1-/RP35/RB3	7	22	TDI/RP43/PWM3L/RB11
VSS	8	21	TDO/RP42/PWM3H/RB10
OSC1/CLKI/RA2	9	20	VCAP
OSC2/CLKO/RA3	10	19	VSS
FLT32/RP36/RB4	11	18	TMS/ASDA1/SDI1/RP41/RB9[3]
CVREF2O/RP20/T1CK/RA4	12	17	TCK/CVREF1O/ASCL1/SDO1/RP40/T4CK/RB8
VDD	13	16	SCK1/RP39/INT0/RB7
PGED2/ASDA2/RP37/RB5	14	15	PGEC2/ASCL2/RP38/RB6

Note 1: The RPn/RPIn pins can be used by any remappable peripheral with some limitation. See **Section 11.4 "Peripheral Pin Select (PPS)"** for available peripherals and for information on limitations.

2: Every I/O port pin (RAx-RGx) can be used as a Change Notification pin (CNAx-CNGx). See **Section 11.0 "I/O Ports"** for more information.

3: There is an internal pull-up resistor connected to the TMS pin when the JTAG interface is active. See the JTAGEN bit field in Table 27-2.

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**TABLE 4-2:** **CPU CORE REGISTER MAP FOR PIC24EPXXXGP/MC20X DEVICES ONLY**

File Name	Addr.	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	All Resets
W0	0000								W0 (WREG)									xxxx
W1	0002								W1									xxxx
W2	0004								W2									xxxx
W3	0006								W3									xxxx
W4	0008								W4									xxxx
W5	000A								W5									xxxx
W6	000C								W6									xxxx
W7	000E								W7									xxxx
W8	0010								W8									xxxx
W9	0012								W9									xxxx
W10	0014								W10									xxxx
W11	0016								W11									xxxx
W12	0018								W12									xxxx
W13	001A								W13									xxxx
W14	001C								W14									xxxx
W15	001E								W15									xxxx
SPLIM	0020								SPLIM<15:0>									0000
PCL	002E								PCL<15:1>								—	0000
PCH	0030	—	—	—	—	—	—	—	—	—			PCH<6:0>					0000
DSRPAG	0032	—	—	—	—	—	—					DSRPAG<9:0>						0001
DSWPAG	0034	—	—	—	—	—	—	—				DSWPAG<8:0>						0001
RCOUNT	0036								RCOUNT<15:0>									0000
SR	0042	—	—	—	—	—	—	DC	IPL2	IPL1	IPL0	RA	N	OV	Z	C		0000
CORCON	0044	VAR	—	—	—	—	—	—	—	—	—	—	—	IPL3	SFA	—	—	0020
DISICNT	0052	—	—						DISICNT<13:0>									0000
TBLPAG	0054	—	—	—	—	—	—	—	—				TBLPAG<7:0>					0000
MSTRPR	0058								MSTRPR<15:0>									0000

Legend: x = unknown value on Reset, — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

TABLE 4-7: INTERRUPT CONTROLLER REGISTER MAP FOR dsPIC33EPXXXMC50X DEVICES ONLY

File Name	Addr.	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	All Resets
IFS0	0800	—	DMA1IF	AD1IF	U1TXIF	U1RXIF	SPI1IF	SPI1EIF	T3IF	T2IF	OC2IF	IC2IF	DMA0IF	T1IF	OC1IF	IC1IF	INT0IF	0000
IFS1	0802	U2TXIF	U2RXIF	INT2IF	T5IF	T4IF	OC4IF	OC3IF	DMA2IF	—	—	—	INT1IF	CNIF	CMIF	MI2C1IF	SI2C1IF	0000
IFS2	0804	—	—	—	—	—	—	—	—	—	IC4IF	IC3IF	DMA3IF	C1IF	C1RXIF	SPI2IF	SPI2EIF	0000
IFS3	0806	—	—	—	—	—	QEI1IF	PSEMIF	—	—	—	—	—	—	MI2C2IF	SI2C2IF	—	0000
IFS4	0808	—	—	CTMUIF	—	—	—	—	—	—	C1TXIF	—	—	CRCIF	U2EIF	U1EIF	—	0000
IFS5	080A	PWM2IF	PWM1IF	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
IFS6	080C	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	PWM3IF	0000
IFS8	0810	JTAGIF	ICDIF	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
IFS9	0812	—	—	—	—	—	—	—	—	—	PTG3IF	PTG2IF	PTG1IF	PTG0IF	PTGWDTIF	PTGSTEPIF	—	0000
IEC0	0820	—	DMA1IE	AD1IE	U1TXIE	U1RXIE	SPI1IE	SPI1EIE	T3IE	T2IE	OC2IE	IC2IE	DMA0IE	T1IE	OC1IE	IC1IE	INT0IE	0000
IEC1	0822	U2TXIE	U2RXIE	INT2IE	T5IE	T4IE	OC4IE	OC3IE	DMA2IE	—	—	—	INT1IE	CNIE	CMIE	MI2C1IE	SI2C1IE	0000
IEC2	0824	—	—	—	—	—	—	—	—	—	IC4IE	IC3IE	DMA3IE	C1IE	C1RXIE	SPI2IE	SPI2EIE	0000
IEC3	0826	—	—	—	—	—	QEI1IE	PSEMIE	—	—	—	—	—	—	MI2C2IE	SI2C2IE	—	0000
IEC4	0828	—	—	CTMUIE	—	—	—	—	—	—	C1TXIE	—	—	CRCIE	U2EIE	U1EIE	—	0000
IEC5	082A	PWM2IE	PWM1IE	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
IEC6	082C	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	PWM3IE	0000
IEC7	082E	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
IEC8	0830	JTAGIE	ICDIE	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
IEC9	0832	—	—	—	—	—	—	—	—	—	PTG3IE	PTG2IE	PTG1IE	PTG0IE	PTGWDTIE	PTGSTEPIE	—	0000
IPC0	0840	—		T1IP<2:0>		—		OC1IP<2:0>		—		IC1IP<2:0>		—		INT0IP<2:0>		4444
IPC1	0842	—		T2IP<2:0>		—		OC2IP<2:0>		—		IC2IP<2:0>		—		DMA0IP<2:0>		4444
IPC2	0844	—		U1RXIP<2:0>		—		SPI1IP<2:0>		—		SPI1EIP<2:0>		—		T3IP<2:0>		4444
IPC3	0846	—	—	—	—	—		DMA1IP<2:0>		—		AD1IP<2:0>		—		U1TXIP<2:0>		0444
IPC4	0848	—		CNIP<2:0>		—		CMIP<2:0>		—		MI2C1IP<2:0>		—		SI2C1IP<2:0>		4444
IPC5	084A	—	—	—	—	—	—	—	—	—	—	—	—	—		INT1IP<2:0>		0004
IPC6	084C	—		T4IP<2:0>		—		OC4IP<2:0>		—		OC3IP<2:0>		—		DMA2IP<2:0>		4444
IPC7	084E	—		U2TXIP<2:0>		—		U2RXIP<2:0>		—		INT2IP<2:0>		—		T5IP<2:0>		4444
IPC8	0850	—		C1IP<2:0>		—		C1RXIP<2:0>		—		SPI2IP<2:0>		—		SPI2EIP<2:0>		4444
IPC9	0852	—	—	—	—	—		IC4IP<2:0>		—		IC3IP<2:0>		—		DMA3IP<2:0>		0444
IPC12	0858	—	—	—	—	—		MI2C2IP<2:0>		—		SI2C2IP<2:0>		—	—	—	—	0440
IPC14	085C	—	—	—	—	—		QEI1IP<2:0>		—		PSEMIP<2:0>		—	—	—	—	0440
IPC16	0860	—		CRCIP<2:0>		—		U2EIP<2:0>		—		U1EIP<2:0>		—	—	—	—	4440
IPC17	0862	—	—	—	—	—		C1TXIP<2:0>		—	—	—	—	—	—	—	—	0400
IPC19	0866	—	—	—	—	—	—	—	—	—		CTMUIP<2:0>		—	—	—	—	0040

Legend: — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

EXAMPLE 4-2: **EXTENDED DATA SPACE (EDS) WRITE ADDRESS GENERATION**

Note: DS read access when DSRPAG = 0x000 will force an address error trap.
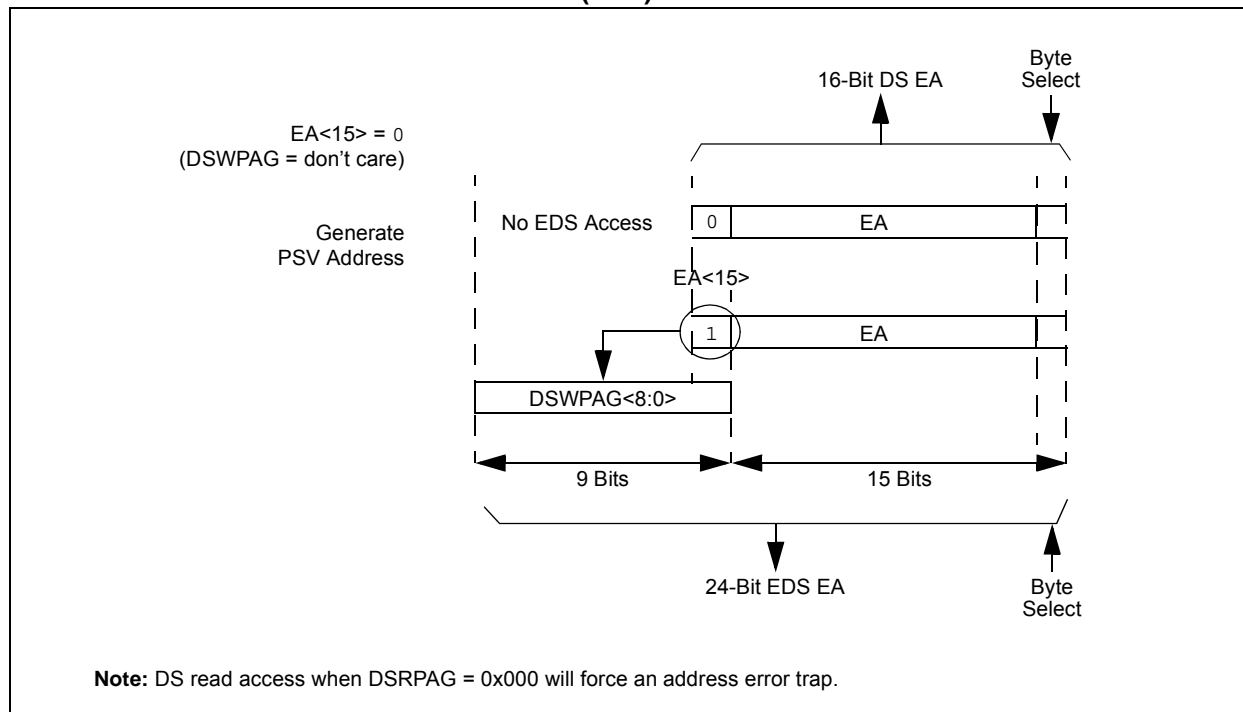
The paged memory scheme provides access to multiple 32-Kbyte windows in the EDS and PSV memory. The Data Space Page registers, DSxPAG, in combination with the upper half of the Data Space address, can provide up to 16 Mbytes of additional address space in the EDS and 8 Mbytes (DSRPAG only) of PSV address space. The paged data memory space is shown in Example 4-3.

The Program Space (PS) can be accessed with a DSRPAG of 0x200 or greater. Only reads from PS are supported using the DSRPAG. Writes to PS are not supported, so DSWPAG is dedicated to DS, including EDS only. The Data Space and EDS can be read from, and written to, using DSRPAG and DSWPAG, respectively.

5.2   RTSP Operation

RTSP allows the user application to erase a single page of memory and to program two instruction words at a time. See the General Purpose and Motor Control Family tables (Table 1 and Table 2, respectively) for the page sizes of each device.

For more information on erasing and programming Flash memory, refer to **"Flash Programming"** (DS70609) in the *"dsPIC33/PIC24 Family Reference Manual"*.

5.3   Programming Operations

A complete programming sequence is necessary for programming or erasing the internal Flash in RTSP mode. The processor stalls (waits) until the programming operation is finished.

For erase and program times, refer to Parameters D137a and D137b (Page Erase Time), and D138a and D138b (Word Write Cycle Time) in Table 30-14 in **Section 30.0 "Electrical Characteristics"**.

Setting the WR bit (NVMCON<15>) starts the operation and the WR bit is automatically cleared when the operation is finished.

5.3.1   PROGRAMMING ALGORITHM FOR FLASH PROGRAM MEMORY

Programmers can program two adjacent words (24 bits x 2) of program Flash memory at a time on every other word address boundary (0x000002, 0x000006, 0x00000A, etc.). To do this, it is necessary to erase the page that contains the desired address of the location the user wants to change.

For protection against accidental operations, the write initiate sequence for NVMKEY must be used to allow any erase or program operation to proceed. After the programming command has been executed, the user application must wait for the programming time until programming is complete. The two instructions following the start of the programming sequence should be NOPs.

Refer to Flash Programming" (DS70609) in the "*dsPIC33/PIC24 Family Reference Manual*" for details and codes examples on programming using RTSP.

5.4   Flash Memory Resources

Many useful resources are provided on the main product page of the Microchip web site for the devices listed in this data sheet. This product page, which can be accessed using this link, contains the latest updates and additional information.

> **Note:**   In the event you are not able to access the product page using the link above, enter this URL in your browser: http://www.microchip.com/wwwproducts/Devices.aspx?dDocName=en555464

5.4.1   KEY RESOURCES

- **"Flash Programming"** (DS70609) in the *"dsPIC33/PIC24 Family Reference Manual"*
- Code Samples
- Application Notes
- Software Libraries
- Webinars
- All Related *"dsPIC33/PIC24 Family Reference Manual"* Sections
- Development Tools

5.5   Control Registers

Four SFRs are used to erase and write the program Flash memory: NVMCON, NVMKEY, NVMADRH and NVMADRL.

The NVMCON register (Register 5-1) enables and initiates Flash memory erase and write operations.

NVMKEY (Register 5-4) is a write-only register that is used for write protection. To start a programming or erase sequence, the user application must consecutively write 0x55 and 0xAA to the NVMKEY register.

There are two NVM Address registers: NVMADRH and NVMADRL. These two registers, when concatenated, form the 24-bit Effective Address (EA) of the selected word for programming operations or the selected page for erase operations.

The NVMADRH register is used to hold the upper 8 bits of the EA, while the NVMADRL register is used to hold the lower 16 bits of the EA.

9.1 CPU Clocking System

The dsPIC33EPXXXGP50X, dsPIC33EPXXXMC20X/50X and PIC24EPXXXGP/MC20X family of devices provides six system clock options:

- Fast RC (FRC) Oscillator
- FRC Oscillator with Phase Locked Loop (PLL)
- FRC Oscillator with Postscaler
- Primary (XT, HS or EC) Oscillator
- Primary Oscillator with PLL
- Low-Power RC (LPRC) Oscillator

Instruction execution speed or device operating frequency, F_{CY}, is given by Equation 9-1.

EQUATION 9-1: DEVICE OPERATING FREQUENCY

$$F_{CY} = F_{OSC}/2$$

Figure 9-2 is a block diagram of the PLL module.

Equation 9-2 provides the relationship between input frequency (F_{IN}) and output frequency (F_{PLLO}). In clock modes S1 and S3, when the PLL output is selected, $F_{OSC} = F_{PLLO}$.

Equation 9-3 provides the relationship between input frequency (F_{IN}) and VCO frequency (F_{VCO}).

FIGURE 9-2: PLL BLOCK DIAGRAM
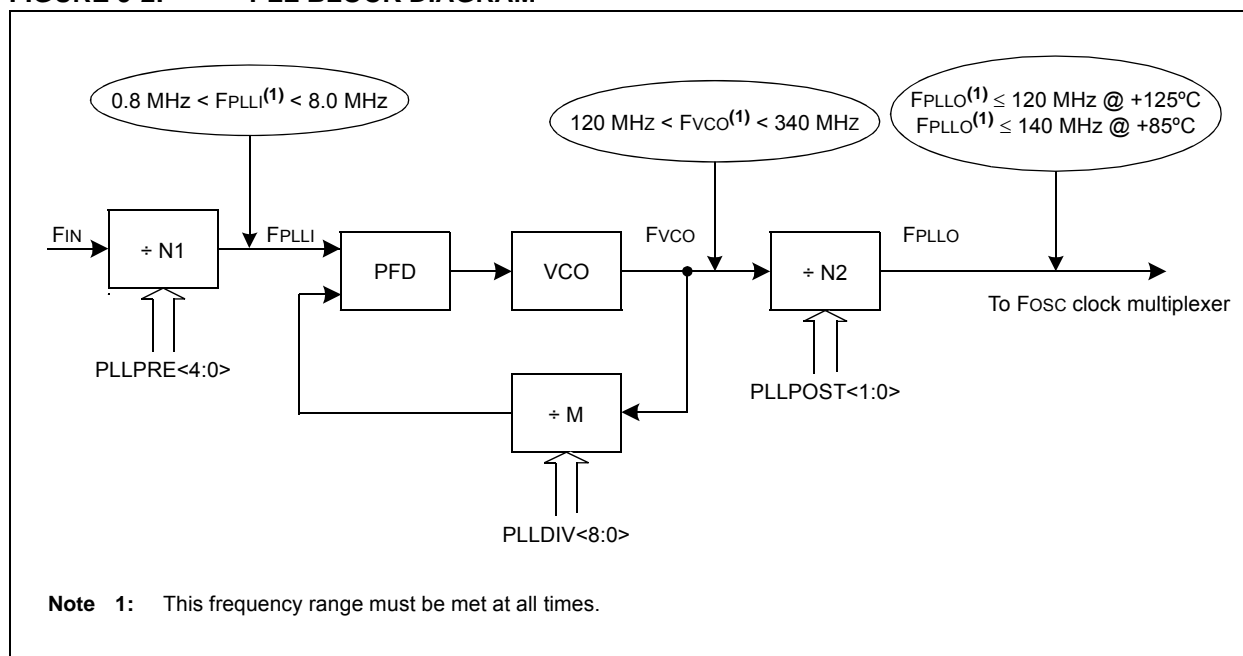
EQUATION 9-2: F_{PLLO} CALCULATION

$$F_{PLLO} = F_{IN} \times \left(\frac{M}{N1 \times N2}\right) = F_{IN} \times \left(\frac{(PLLDIV + 2)}{(PLLPRE + 2) \times 2(PLLPOST + 1)}\right)$$

Where:

$N1 = PLLPRE + 2$

$N2 = 2 \times (PLLPOST + 1)$

$M = PLLDIV + 2$

EQUATION 9-3: F_{VCO} CALCULATION

$$F_{VCO} = F_{IN} \times \left(\frac{M}{N1}\right) = F_{IN} \times \left(\frac{(PLLDIV + 2)}{(PLLPRE + 2)}\right)$$

REGISTER 15-2: **OCxCON2: OUTPUT COMPARE x CONTROL REGISTER 2**

R/W-0	R/W-0	R/W-0	R/W-0	U-0	U-0	U-0	R/W-0
FLTMD	FLTOUT	FLTTRIEN	OCINV	—	—	—	OC32
bit 15							bit 8

R/W-0	R/W-0, HS	R/W-0	R/W-0	R/W-1	R/W-1	R/W-0	R/W-0
OCTRIG	TRIGSTAT	OCTRIS	SYNCSEL4	SYNCSEL3	SYNCSEL2	SYNCSEL1	SYNCSEL0
bit 7							bit 0

Legend:		HS = Hardware Settable bit	
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15 **FLTMD:** Fault Mode Select bit

1 = Fault mode is maintained until the Fault source is removed; the corresponding OCFLTx bit is cleared in software and a new PWM period starts
0 = Fault mode is maintained until the Fault source is removed and a new PWM period starts

bit 14 **FLTOUT:** Fault Out bit

1 = PWM output is driven high on a Fault
0 = PWM output is driven low on a Fault

bit 13 **FLTTRIEN:** Fault Output State Select bit

1 = OCx pin is tri-stated on a Fault condition
0 = OCx pin I/O state is defined by the FLTOUT bit on a Fault condition

bit 12 **OCINV:** Output Compare x Invert bit

1 = OCx output is inverted
0 = OCx output is not inverted

bit 11-9 **Unimplemented:** Read as '0'

bit 8 **OC32:** Cascade Two OCx Modules Enable bit (32-bit operation)

1 = Cascade module operation is enabled
0 = Cascade module operation is disabled

bit 7 **OCTRIG:** Output Compare x Trigger/Sync Select bit

1 = Triggers OCx from the source designated by the SYNCSELx bits
0 = Synchronizes OCx with the source designated by the SYNCSELx bits

bit 6 **TRIGSTAT:** Timer Trigger Status bit

1 = Timer source has been triggered and is running
0 = Timer source has not been triggered and is being held clear

bit 5 **OCTRIS:** Output Compare x Output Pin Direction Select bit

1 = OCx is tri-stated
0 = Output Compare x module drives the OCx pin

Note 1: Do not use the OCx module as its own Synchronization or Trigger source.

    2: When the OCy module is turned OFF, it sends a trigger out signal. If the OCx module uses the OCy module as a Trigger source, the OCy module must be unselected as a Trigger source prior to disabling it.

    3: Each Output Compare x module (OCx) has one PTG Trigger/Synchronization source. See **Section 24.0 "Peripheral Trigger Generator (PTG) Module"** for more information.
PTGO0 = OC1
PTGO1 = OC2
PTGO2 = OC3
PTGO3 = OC4

REGISTER 16-12:   TRGCONx: PWMx TRIGGER CONTROL REGISTER

R/W-0	R/W-0	R/W-0	R/W-0	U-0	U-0	U-0	U-0
TRGDIV\<3:0\>				—	—	—	—
bit 15							bit 8

U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
—	—	TRGSTRT\<5:0\>[1]					
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15-12 **TRGDIV\<3:0\>:** Trigger # Output Divider bits

1111 = Trigger output for every 16th trigger event
1110 = Trigger output for every 15th trigger event
1101 = Trigger output for every 14th trigger event
1100 = Trigger output for every 13th trigger event
1011 = Trigger output for every 12th trigger event
1010 = Trigger output for every 11th trigger event
1001 = Trigger output for every 10th trigger event
1000 = Trigger output for every 9th trigger event
0111 = Trigger output for every 8th trigger event
0110 = Trigger output for every 7th trigger event
0101 = Trigger output for every 6th trigger event
0100 = Trigger output for every 5th trigger event
0011 = Trigger output for every 4th trigger event
0010 = Trigger output for every 3rd trigger event
0001 = Trigger output for every 2nd trigger event
0000 = Trigger output for every trigger event

bit 11-6 **Unimplemented:** Read as '0'

bit 5-0 **TRGSTRT\<5:0\>:** Trigger Postscaler Start Enable Select bits[1]

111111 = Waits 63 PWM cycles before generating the first trigger event after the module is enabled
•
•
•
000010 = Waits 2 PWM cycles before generating the first trigger event after the module is enabled
000001 = Waits 1 PWM cycle before generating the first trigger event after the module is enabled
000000 = Waits 0 PWM cycles before generating the first trigger event after the module is enabled

Note 1: The secondary PWM generator cannot generate PWMx trigger interrupts.

REGISTER 17-3:   QEI1STAT: QEI1 STATUS REGISTER (CONTINUED)

bit 2   **HOMIEN:** Home Input Event Interrupt Enable bit

1 = Interrupt is enabled
0 = Interrupt is disabled

bit 1   **IDXIRQ:** Status Flag for Index Event Status bit

1 = Index event has occurred
0 = No Index event has occurred

bit 0   **IDXIEN:** Index Input Event Interrupt Enable bit

1 = Interrupt is enabled
0 = Interrupt is disabled

Note 1:   This status bit is only applicable to PIMOD<2:0> modes, '011' and '100'.

18.0 SERIAL PERIPHERAL INTERFACE (SPI)

> **Note 1:** This data sheet summarizes the features of the dsPIC33EPXXXGP50X, dsPIC33EPXXXMC20X/50X and PIC24EPXXXGP/MC20X families of devices. It is not intended to be a comprehensive reference source. To complement the information in this data sheet, refer to **"Serial Peripheral Interface (SPI)"** (DS70569) in the "*dsPIC33/PIC24 Family Reference Manual*", which is available from the Microchip web site (www.microchip.com).
>
> **2:** Some registers and associated bits described in this section may not be available on all devices. Refer to **Section 4.0 "Memory Organization"** in this data sheet for device-specific register and bit information.

The SPI module is a synchronous serial interface, useful for communicating with other peripheral or microcontroller devices. These peripheral devices can be serial EEPROMs, shift registers, display drivers, ADC Converters, etc. The SPI module is compatible with Motorola® SPI and SIOP interfaces.

The dsPIC33EPXXXGP50X, dsPIC33EPXXXMC20X/50X and PIC24EPXXXGP/MC20X device family offers two SPI modules on a single device. These modules, which are designated as SPI1 and SPI2, are functionally identical. Each SPI module includes an eight-word FIFO buffer and allows DMA bus connections. When using the SPI module with DMA, FIFO operation can be disabled.

> **Note:** In this section, the SPI modules are referred to together as SPIx, or separately as SPI1 and SPI2. Special Function Registers follow a similar notation. For example, SPIxCON refers to the control register for the SPI1 and SPI2 modules.

The SPI1 module uses dedicated pins which allow for a higher speed when using SPI1. The SPI2 module takes advantage of the Peripheral Pin Select (PPS) feature to allow for greater flexibility in pin configuration of the SPI2 module, but results in a lower maximum speed for SPI2. See **Section 30.0 "Electrical Characteristics"** for more information.

The SPIx serial interface consists of four pins, as follows:

- SDIx: Serial Data Input
- SDOx: Serial Data Output
- SCKx: Shift Clock Input or Output
- SSx/FSYNCx: Active-Low Slave Select or Frame Synchronization I/O Pulse

The SPIx module can be configured to operate with two, three or four pins. In 3-pin mode, $\overline{SSx}$ is not used. In 2-pin mode, neither SDOx nor $\overline{SSx}$ is used.

Figure 18-1 illustrates the block diagram of the SPIx module in Standard and Enhanced modes.

FIGURE 19-1: **I2Cx BLOCK DIAGRAM   (x = 1 OR 2)**
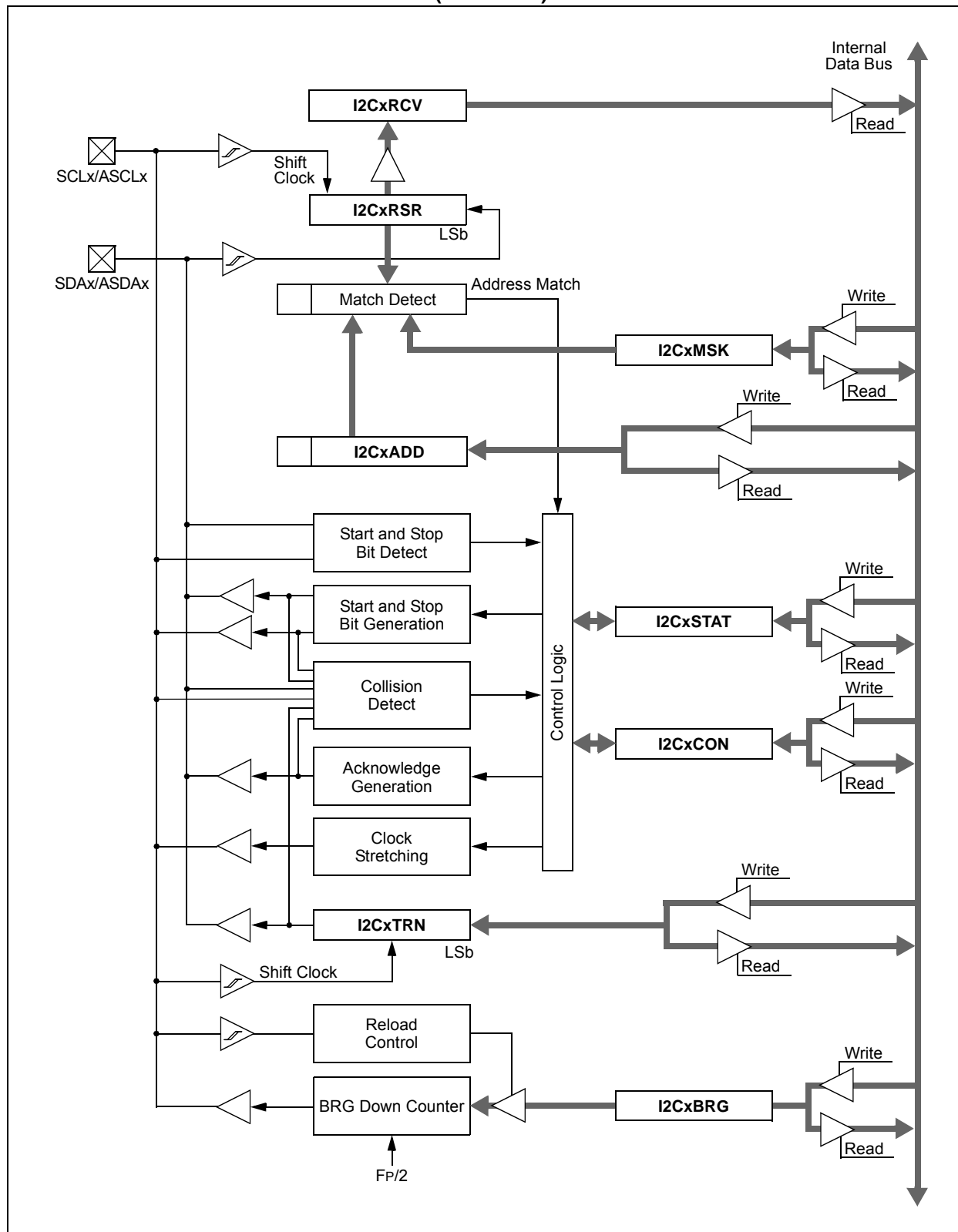
REGISTER 23-6: **AD1CHS0: ADC1 INPUT CHANNEL 0 SELECT REGISTER (CONTINUED)**

bit 4-0 **CH0SA<4:0>:** Channel 0 Positive Input Select for Sample MUXA bits[1]

11111 = Open; use this selection with CTMU capacitive and time measurement
11110 = Channel 0 positive input is connected to the CTMU temperature measurement diode (CTMU TEMP)
11101 = Reserved
11100 = Reserved
11011 = Reserved
11010 = Channel 0 positive input is the output of OA3/AN6[2,3]
11001 = Channel 0 positive input is the output of OA2/AN0[2]
11000 = Channel 0 positive input is the output of OA1/AN3[2]
10110 = Reserved
•
•
•
10000 = Reserved
01111 = Channel 0 positive input is AN15[1,3]
01110 = Channel 0 positive input is AN14[1,3]
01101 = Channel 0 positive input is AN13[1,3]
•
•
•
00010 = Channel 0 positive input is AN2[1,3]
00001 = Channel 0 positive input is AN1[1,3]
00000 = Channel 0 positive input is AN0[1,3]

Note 1: AN0 through AN7 are repurposed when comparator and op amp functionality is enabled. See Figure 23-1 to determine how enabling a particular op amp or comparator affects selection choices for Channels 1, 2 and 3.

2: The OAx input is used if the corresponding op amp is selected (OPMODE (CMxCON<10>) = 1); otherwise, the ANx input is used.

3: See the **"Pin Diagrams"** section for the available analog channels for each device.

REGISTER 27-1:   DEVID: DEVICE ID REGISTER

R	R	R	R	R	R	R	R
DEVID<23:16>[1]							
bit 23							bit 16

R	R	R	R	R	R	R	R
DEVID<15:8>[1]							
bit 15							bit 8

R	R	R	R	R	R	R	R
DEVID<7:0>[1]							
bit 7							bit 0

Legend:	R = Read-Only bit	U = Unimplemented bit

bit 23-0   **DEVID<23:0>:** Device Identifier bits[1]

Note 1:   Refer to the *"dsPIC33E/PIC24E Flash Programming Specification for Devices with Volatile Configuration Bits"* (DS70663) for the list of device ID values.

REGISTER 27-2:   DEVREV: DEVICE REVISION REGISTER

R	R	R	R	R	R	R	R
DEVREV<23:16>[1]							
bit 23							bit 16

R	R	R	R	R	R	R	R
DEVREV<15:8>[1]							
bit 15							bit 8

R	R	R	R	R	R	R	R
DEVREV<7:0>[1]							
bit 7							bit 0

Legend:	R = Read-only bit	U = Unimplemented bit

bit 23-0   **DEVREV<23:0>:** Device Revision bits[1]

Note 1:   Refer to the *"dsPIC33E/PIC24E Flash Programming Specification for Devices with Volatile Configuration Bits"* (DS70663) for the list of device revision values.

TABLE 30-11: DC CHARACTERISTICS: I/O PIN INPUT SPECIFICATIONS (CONTINUED)

DC CHARACTERISTICS							Standard Operating Conditions: 3.0V to 3.6V (unless otherwise stated) Operating temperature -40°C ≤ TA ≤ +85°C for Industrial -40°C ≤ TA ≤ +125°C for Extended
Param No.	Symbol	Characteristic	Min.	Typ.	Max.	Units	Conditions
	I_{IL}	**Input Leakage Current[1,2]**					
DI50		I/O Pins 5V Tolerant[3]	-1	—	+1	μA	$V_{SS} \leq V_{PIN} \leq V_{DD}$, Pin at high-impedance
DI51		I/O Pins Not 5V Tolerant[3]	-1	—	+1	μA	$V_{SS} \leq V_{PIN} \leq V_{DD}$, Pin at high-impedance, -40°C ≤ TA ≤ +85°C
DI51a		I/O Pins Not 5V Tolerant[3]	-1	—	+1	μA	Analog pins shared with external reference pins, -40°C ≤ TA ≤ +85°C
DI51b		I/O Pins Not 5V Tolerant[3]	-1	—	+1	μA	$V_{SS} \leq V_{PIN} \leq V_{DD}$, Pin at high-impedance, -40°C ≤ TA ≤ +125°C
DI51c		I/O Pins Not 5V Tolerant[3]	-1	—	+1	μA	Analog pins shared with external reference pins, -40°C ≤ TA ≤ +125°C
DI55		$\overline{MCLR}$	-5	—	+5	μA	$V_{SS} \leq V_{PIN} \leq V_{DD}$
DI56		OSC1	-5	—	+5	μA	$V_{SS} \leq V_{PIN} \leq V_{DD}$, XT and HS modes

Note 1: The leakage current on the $\overline{MCLR}$ pin is strongly dependent on the applied voltage level. The specified levels represent normal operating conditions. Higher leakage current can be measured at different input voltages.

   2: Negative current is defined as current sourced by the pin.

   3: See the **"Pin Diagrams"** section for the 5V tolerant I/O pins.

   4: V_{IL} source < (V_{SS} – 0.3). Characterized but not tested.

   5: Non-5V tolerant pins V_{IH} source > (V_{DD} + 0.3), 5V tolerant pins V_{IH} source > 5.5V. Characterized but not tested.

   6: Digital 5V tolerant pins cannot tolerate any "positive" input injection current from input sources > 5.5V.

   7: Non-zero injection currents can affect the ADC results by approximately 4-6 counts.

   8: Any number and/or combination of I/O pins not excluded under I_{ICL} or I_{ICH} conditions are permitted provided the mathematical "absolute instantaneous" sum of the input injection currents from all pins do not exceed the specified limit. Characterized but not tested.

48-Lead Plastic Ultra Thin Quad Flat, No Lead Package (MV) – 6x6x0.5 mm Body [UQFN]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging
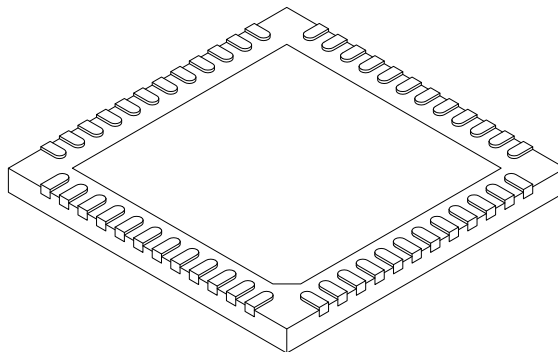
	Units		MILLIMETERS	
Dimension Limits		MIN	NOM	MAX
Number of Pins	N		48	
Pitch	e		0.40 BSC	
Overall Height	A	0.45	0.50	0.55
Standoff	A1	0.00	0.02	0.05
Contact Thickness	A3		0.127 REF	
Overall Width	E		6.00 BSC	
Exposed Pad Width	E2	4.45	4.60	4.75
Overall Length	D		6.00 BSC	
Exposed Pad Length	D2	4.45	4.60	4.75
Contact Width	b	0.15	0.20	0.25
Contact Length	L	0.30	0.40	0.50
Contact-to-Exposed Pad	K	0.20	-	-

Notes:
1. Pin 1 visual index feature may vary, but must be located within the hatched area.
2. Package is saw singulated.
3. Dimensioning and tolerancing per ASME Y14.5M.
    BSC: Basic Dimension. Theoretically exact value shown without tolerances.
    REF: Reference Dimension, usually without tolerance, for information purposes only.

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64-Lead Plastic Quad Flat, No Lead Package (MR) – 9x9x0.9 mm Body
with 5.40 x 5.40 Exposed Pad [QFN]

> **Note:** For the most current package drawings, please see the Microchip Packaging Specification located at
> http://www.microchip.com/packaging

TOP VIEW

SEATING PLANE

BOTTOM VIEW

Microchip Technology Drawing C04-154A Sheet 1 of 2

APPENDIX A: REVISION HISTORY

Revision A (April 2011)

This is the initial released version of the document.

Revision B (July 2011)

This revision includes minor typographical and formatting changes throughout the data sheet text.

All other major changes are referenced by their respective section in Table A-1.

TABLE A-1: MAJOR SECTION UPDATES

Section Name	Update Description
"High-Performance, 16-bit Digital Signal Controllers and Microcontrollers"	Changed all pin diagrams references of VLAP to TLA.
Section 4.0 "Memory Organization"	Updated the All Resets values for CLKDIV and PLLFBD in the System Control Register Map (see Table 4-35).
Section 5.0 "Flash Program Memory"	Updated "one word" to "two words" in the first paragraph of **Section 5.2 "RTSP Operation"**.
Section 9.0 "Oscillator Configuration"	Updated the PLL Block Diagram (see Figure 9-2).
	Updated the Oscillator Mode, Fast RC Oscillator (FRC) with divide-by-N and PLL (FRCPLL), by changing (FRCDIVN + PLL) to (FRCPLL).
	Changed (FRCDIVN + PLL) to (FRCPLL) for COSC<2:0> = `001` and NOSC<2:0> = `001` in the Oscillator Control Register (see Register 9-1).
	Changed the POR value from 0 to 1 for the DOZE<1:0> bits, from 1 to 0 for the FRCDIV<0> bit, and from 0 to 1 for the PLLPOST<0> bit; Updated the default definitions for the DOZE<2:0> and FRCDIV<2:0> bits and updated all bit definitions for the PLLPOST<1:0> bits in the Clock Divisor Register (see Register 9-2).
	Changed the POR value from 0 to 1 for the PLLDIV<5:4> bits and updated the default definitions for all PLLDIV<8:0> bits in the PLL Feedback Division Register (see Register 9-2).
Section 22.0 "Charge Time Measurement Unit (CTMU)"	Updated the bit definitions for the IRNG<1:0> bits in the CTMU Current Control Register (see Register 22-3).
Section 25.0 "Op amp/ Comparator Module"	Updated the voltage reference block diagrams (see Figure 25-1 and Figure 25-2).

Revision H (August 2013)

This revision includes minor typographical and formatting changes throughout the text.

Other major changes are referenced by their respective section in Table A-6.

TABLE A-6:   MAJOR SECTION UPDATES

Section Name	Update Description
Cover Section	• Adds Peripheral Pin Select (PPS) to allow Digital Function Remapping and Change Notification Interrupts to Input/Output section • Adds heading information to 64-Pin TQFP
Section 4.0 "Memory Organization"	• Corrects Reset values for ANSELE, TRISF, TRISC, ANSELC and TRISA • Corrects address range from 0x2FFF to 0x7FFF • Corrects DSRPAG and DSWPAG (now 3 hex digits) • Changes Call Stack Frame from <15:1> to PC<15:0> • Word length in Figure 4-20 is changed to 50 words for clarity
Section 5.0 "Flash Program Memory"	• Corrects descriptions of NVM registers
Section 9.0 "Oscillator Configuration"	• Removes resistor from Figure 9-1 • Adds Fast RC Oscillator with Divide-by-16 (FRCDIV16) row to Table 9-1 • Removes incorrect information from ROI bit in Register 9-2
Section 14.0 "Input Capture"	• Changes 31 user-selectable Trigger/Sync interrupts to 19 user-selectable Trigger/Sync interrupts • Corrects ICTSEL<12:10> bits (now ICTSEL<2:0>)
Section 17.0 "Quadrature Encoder Interface (QEI) Module (dsPIC33EPXXXMC20X/50X and PIC24EPXXXMC20X Devices Only)"	• Corrects QCAPEN bit description
Section 19.0 "Inter-Integrated Circuit™ (I²C™)"	• Adds note to clarify that 100kbit/sec operation of I²C is not possible at high processor speeds
Section 22.0 "Charge Time Measurement Unit (CTMU)"	• Clarifies Figure 22-1 to accurately reflect peripheral behavior
Section 23.0 "10-Bit/12-Bit Analog-to-Digital Converter (ADC)"	• Correct Figure 23-1 (changes CH123x to CH123Sx)
Section 24.0 "Peripheral Trigger Generator (PTG) Module"	• Adds footnote to Register 24-1 (In order to operate with CVRSS=1, at least one of the comparator modules must be enabled.
Section 25.0 "Op Amp/ Comparator Module"	• Adds note to Figure 25-3 (In order to operate with CVRSS=1, at least one of the comparator modules must be enabled) • Adds footnote to Register 25-2 (COE is not available when OPMODE (CMxCON<10>) = 1)
Section 27.0 "Special Features"	• Corrects the bit description for FNOSC<2:0>
Section 30.0 "Electrical Characteristics"	• Corrects 512K part power-down currents based on test data • Corrects WDT timing limits based on LPRC oscillator tolerance
Section 31.0 "High-Temperature Electrical Characteristics"	• Adds Table 31-5 (DC Characteristics: Idle Current (IIDLE)