

Welcome to E-XFL.COM

What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "<u>Embedded -</u> <u>Microcontrollers</u>"

Details

⊡XFI

Product Status	Active
Core Processor	PIC
Core Size	16-Bit
Speed	70 MIPs
Connectivity	I ² C, IrDA, LINbus, QEI, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, DMA, Motor Control PWM, POR, PWM, WDT
Number of I/O	21
Program Memory Size	32KB (10.7K x 24)
Program Memory Type	FLASH
EEPROM Size	•
RAM Size	2K x 16
Voltage - Supply (Vcc/Vdd)	3V ~ 3.6V
Data Converters	A/D 6x10b/12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	28-VQFN Exposed Pad
Supplier Device Package	28-QFN-S (6x6)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/pic24ep32mc202-i-mm

Email: info@E-XFL.COM

Address: Room A, 16/F, Full Win Commercial Centre, 573 Nathan Road, Mongkok, Hong Kong

4.2 Data Address Space

The dsPIC33EPXXXGP50X, dsPIC33EPXXXMC20X/ 50X and PIC24EPXXXGP/MC20X CPU has a separate 16-bit-wide data memory space. The Data Space is accessed using separate Address Generation Units (AGUs) for read and write operations. The data memory maps, which are presented by device family and memory size, are shown in Figure 4-7 through Figure 4-16.

All Effective Addresses (EAs) in the data memory space are 16 bits wide and point to bytes within the Data Space. This arrangement gives a base Data Space address range of 64 Kbytes (32K words).

The base Data Space address is used in conjunction with a Read or Write Page register (DSRPAG or DSWPAG) to form an Extended Data Space, which has a total address range of 16 Mbytes.

dsPIC33EPXXXGP50X, dsPIC33EPXXXMC20X/50X and PIC24EPXXXGP/MC20X devices implement up to 52 Kbytes of data memory (4 Kbytes of data memory for Special Function Registers and up to 48 Kbytes of data memory for RAM). If an EA points to a location outside of this area, an all-zero word or byte is returned.

4.2.1 DATA SPACE WIDTH

The data memory space is organized in byteaddressable, 16-bit-wide blocks. Data is aligned in data memory and registers as 16-bit words, but all Data Space EAs resolve to bytes. The Least Significant Bytes (LSBs) of each word have even addresses, while the Most Significant Bytes (MSBs) have odd addresses.

4.2.2 DATA MEMORY ORGANIZATION AND ALIGNMENT

To maintain backward compatibility with PIC[®] MCU devices and improve Data Space memory usage efficiency, the dsPIC33EPXXXGP50X, dsPIC33EPXXXMC20X/50X and PIC24EPXXXGP/ MC20X instruction set supports both word and byte operations. As a consequence of byte accessibility, all Effective Address calculations are internally scaled to step through word-aligned memory. For example, the core recognizes that Post-Modified Register Indirect Addressing mode [Ws++] results in a value of Ws + 1 for byte operations and Ws + 2 for word operations.

A data byte read, reads the complete word that contains the byte, using the LSb of any EA to determine which byte to select. The selected byte is placed onto the LSB of the data path. That is, data memory and registers are organized as two parallel, byte-wide entities with shared (word) address decode but separate write lines. Data byte writes only write to the corresponding side of the array or register that matches the byte address. All word accesses must be aligned to an even address. Misaligned word data fetches are not supported, so care must be taken when mixing byte and word operations, or translating from 8-bit MCU code. If a misaligned read or write is attempted, an address error trap is generated. If the error occurred on a read, the instruction underway is completed. If the error occurred on a write, the instruction is executed but the write does not occur. In either case, a trap is then executed, allowing the system and/or user application to examine the machine state prior to execution of the address Fault.

All byte loads into any W register are loaded into the LSB. The MSB is not modified.

A Sign-Extend (SE) instruction is provided to allow user applications to translate 8-bit signed data to 16-bit signed values. Alternatively, for 16-bit unsigned data, user applications can clear the MSB of any W register by executing a Zero-Extend (ZE) instruction on the appropriate address.

4.2.3 SFR SPACE

The first 4 Kbytes of the Near Data Space, from 0x0000 to 0x0FFF, is primarily occupied by Special Function Registers (SFRs). These are used by the dsPIC33EPXXXGP50X, dsPIC33EPXXXMC20X/50X and PIC24EPXXXGP/MC20X core and peripheral modules for controlling the operation of the device.

SFRs are distributed among the modules that they control and are generally grouped together by module. Much of the SFR space contains unused addresses; these are read as '0'.

Note: The actual set of peripheral features and interrupts varies by the device. Refer to the corresponding device tables and pinout diagrams for device-specific information.

4.2.4 NEAR DATA SPACE

The 8-Kbyte area, between 0x0000 and 0x1FFF, is referred to as the Near Data Space. Locations in this space are directly addressable through a 13-bit absolute address field within all memory direct instructions. Additionally, the whole Data Space is addressable using MOV instructions, which support Memory Direct Addressing mode with a 16-bit address field, or by using Indirect Addressing mode using a working register as an Address Pointer.

4.4 Special Function Register Maps

TABLE 4-1: CPU CORE REGISTER MAP FOR dsPIC33EPXXXMC20X/50X AND dsPIC33EPXXXGP50X DEVICES ONLY

File Name	Addr.	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	All Resets
W0	0000								W0 (WR	EG)								xxxx
W1	0002								W1									xxxx
W2	0004								W2									xxxx
W3	0006								W3									xxxx
W4	8000								W4									xxxx
W5	000A								W5									xxxx
W6	000C								W6									xxxx
W7	000E								W7									xxxx
W8	0010								W8									xxxx
W9	0012								W9									xxxx
W10	0014								W10									xxxx
W11	0016								W11									xxxx
W12	0018								W12									xxxx
W13	001A								W13									xxxx
W14	001C								W14									xxxx
W15	001E								W15									xxxx
SPLIM	0020								SPLI	Л								0000
ACCAL	0022								ACCA	L								0000
ACCAH	0024								ACCA	н								0000
ACCAU	0026			Się	gn Extensio	n of ACCA<	39>						AC	CAU				0000
ACCBL	0028								ACCB	L								0000
ACCBH	002A								ACCB	н								0000
ACCBU	002C			Się	gn Extensio	n of ACCB<	39>						AC	CBU				0000
PCL	002E							P	CL<15:0>								—	0000
PCH	0030	_	—	—	—	_	-	—	—	—				PCH<6:0>				0000
DSRPAG	0032	_	—	—	—	_	-					DSRPAC	G<9:0>					0001
DSWPAG	0034	_	—	—	—	_	-	—				DS	WPAG<8:	0>				0001
RCOUNT	0036								RCOUNT<	:15:0>								0000
DCOUNT	0038								DCOUNT<	:15:0>								0000
DOSTARTL	003A							DOS	TARTL<15:1	>							—	0000
DOSTARTH	003C	_	_	—	_	—	_	_	_	_	—			DOSTAF	RTH<5:0>			0000
DOENDL	003E							DO	ENDL<15:1>	>							_	0000
DOENDH	0040	_	_	—	—	_	_	_	—	_	_			DOEND)H<5:0>			0000

Legend: x = unknown value on Reset, — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

TABLE 4-3: INTERRUPT CONTROLLER REGISTER MAP FOR PIC24EPXXXGP20X DEVICES ONLY

File Name	Addr.	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	All Resets
IFS0	0800	—	DMA1IF	AD1IF	U1TXIF	U1RXIF	SPI1IF	SPI1EIF	T3IF	T2IF	OC2IF	IC2IF	DMA0IF	T1IF	OC1IF	IC1IF	INT0IF	0000
IFS1	0802	U2TXIF	U2RXIF	INT2IF	T5IF	T4IF	OC4IF	OC3IF	DMA2IF	-	—	_	INT1IF	CNIF	CMIF	MI2C1IF	SI2C1IF	0000
IFS2	0804	—	—	—		—	_	_	_		IC4IF	IC3IF	DMA3IF	_	—	SPI2IF	SPI2EIF	0000
IFS3	0806	—	—	—		—	—	_	_		—	—	_	—	MI2C2IF	SI2C2IF	—	0000
IFS4	0808	_	_	CTMUIF		_	_	_	_		_	_	—	CRCIF	U2EIF	U1EIF	_	0000
IFS8	0810	JTAGIF	ICDIF	—	_	—	—	—	—	_	—	—	—	—	—	—	—	0000
IFS9	0812	—	—	—	_	—	—	—	—	_	PTG3IF	PTG2IF	PTG1IF	PTG0IF	PTGWDTIF	PTGSTEPIF	—	0000
IEC0	0820	—	DMA1IE	AD1IE	U1TXIE	U1RXIE	SPI1IE	SPI1EIE	T3IE	T2IE	OC2IE	IC2IE	DMA0IE	T1IE	OC1IE	IC1IE	INT0IE	0000
IEC1	0822	U2TXIE	U2RXIE	INT2IE	T5IE	T4IE	OC4IE	OC3IE	DMA2IE	_	—	—	INT1IE	CNIE	CMIE	MI2C1IE	SI2C1IE	0000
IEC2	0824	—	—	—	_	—	—	—	—	_	IC4IE	IC3IE	DMA3IE	—	—	SPI2IE	SPI2EIE	0000
IEC3	0826	—	—	—	_	—	—	—	—		—	_	—	—	MI2C2IE	SI2C2IE	—	0000
IEC4	0828	—	—	CTMUIE	_	—	—	—	—	_	—	—	—	CRCIE	U2EIE	U1EIE	—	0000
IEC8	0830	JTAGIE	ICDIE	—	_	—	—	—	—		—	_	—	—	—	—	—	0000
IEC9	0832	—	—	—	_	—	—	—	_	_	PTG3IE	PTG2IE	PTG1IE	PTG0IE	PTGWDTIE	PTGSTEPIE	—	0000
IPC0	0840	—		T1IP<2:0>		—		OC1IP<2:0)>	_		IC1IP<2:0>		—		INT0IP<2:0>		4444
IPC1	0842	—		T2IP<2:0>		—		OC2IP<2:0)>			IC2IP<2:0>		—	0	0MA0IP<2:0>		4444
IPC2	0844	—	ι	J1RXIP<2:0	>	—	:	SPI1IP<2:0)>	_		SPI1EIP<2:0	>	—		T3IP<2:0>		4444
IPC3	0846	—	—	—	—	—	0)ma1ip<2:	0>			AD1IP<2:0>	•	—	ι	J1TXIP<2:0>		0444
IPC4	0848	—		CNIP<2:0>		—		CMIP<2:0	>	_		MI2C1IP<2:0	>	—	5	SI2C1IP<2:0>		4444
IPC5	084A	—	—	—	_	—	—	—	—	_	—	—	—	—		INT1IP<2:0>		0004
IPC6	084C	—		T4IP<2:0>		—		OC4IP<2:0)>	_		OC3IP<2:0>	•	—	0	0MA2IP<2:0>		4444
IPC7	084E	—	I	J2TXIP<2:0	>	—	ι	J2RXIP<2:	0>	_		INT2IP<2:0>	>	—		T5IP<2:0>		4444
IPC8	0850	—	—	—	_	—	—	—	—	_		SPI2IP<2:0>	>	—	S	SPI2EIP<2:0>		0044
IPC9	0852	—	—	—	_	—		IC4IP<2:0	>	_		IC3IP<2:0>		—	0	0MA3IP<2:0>		0444
IPC12	0858	—	—	—	_	—	N	112C2IP<2:	0>	_		SI2C2IP<2:0	>	—	—	—	—	0440
IPC16	0860	—		CRCIP<2:0	>	—		U2EIP<2:0	>	_		U1EIP<2:0>		—	—	—	—	4440
IPC19	0866	—	—	—	_	—	—	—	—	_		CTMUIP<2:0	>	—	—	—	—	0040
IPC35	0886	—		JTAGIP<2:0	>	—		ICDIP<2:0	>	_	—	—	—	—	—	—	—	4400
IPC36	0888	—	F	PTG0IP<2:0	>	—	PT	GWDTIP<	2:0>	_	P	TGSTEPIP<2	2:0>	—	—	—	—	4440
IPC37	088A	—	—	—		—	F	PTG3IP<2:	0>			PTG2IP<2:0	>	—	F	PTG1IP<2:0>		0444
INTCON1	08C0	NSTDIS	OVAERR	OVBERR	_	—	—	—	—	_	DIV0ERR	DMACERR	MATHERR	ADDRERR	STKERR	OSCFAIL	—	0000
INTCON2	08C2	GIE	DISI	SWTRAP	_	—	_	—	—	_	—	_	_	—	INT2EP	INT1EP	INT0EP	8000
INTCON3	08C4	_	—	—	_	—	_	—	—	_	—	DAE	DOOVR	—	_	—	—	0000
INTCON4	08C6	—	—	—	—	—	—	—	—	_	—	—	—	—	—	—	SGHT	0000
INTTREG	08C8	_	_	_	—		ILR<	3:0>					VECN	JM<7:0>				0000

- = unimplemented, read as '0'. Reset values are shown in hexadecimal. Legend:

TADLL 4-2		LUANT	NL GIG I				ICINE	1<02) -	· • • • • .	I I OK US			IC/GFJ					
File Name	Addr.	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	All Resets
C1CTRL1	0400	_	—	CSIDL	ABAT	CANCKS	R	EQOP<2:0)>	OPN	NODE<2:0	>	_	CANCAP	_	_	WIN	0480
C1CTRL2	0402	_	—	_	—	—	—	_	_	_	—	_		D	NCNT<4:0	>		0000
C1VEC	0404	_	_	_		F	ILHIT<4:0>			_				ICODE<6:0	>			0040
C1FCTRL	0406	[DMABS<2:0	>	—	—		—	_	_	—	—			FSA<4:0>			0000
C1FIFO	0408	_	_			FBP<	5:0>			_	_			FNRB	<5:0>			0000
C1INTF	040A	_	_	ТХВО	TXBP	RXBP	TXWAR	RXWAR	EWARN	IVRIF	WAKIF	ERRIF	_	FIFOIF	RBOVIF	RBIF	TBIF	0000
C1INTE	040C	_	_	_	—	—	_	_	_	IVRIE	WAKIE	ERRIE	_	FIFOIE	RBOVIE	RBIE	TBIE	0000
C1EC	040E				TERRCN	T<7:0>							RERRCM	NT<7:0>				0000
C1CFG1	0410	_	_	_	—	—	_	_	_	SJW<	1:0>			BRP	<5:0>			0000
C1CFG2	0412	_	WAKFIL	_	—	—	SI	EG2PH<2:(0>	SEG2PHTS	SAM	S	EG1PH<2	::0>	P	RSEG<2:0	>	0000
C1FEN1	0414	FLTEN15	FLTEN14	FLTEN13	FLTEN12	FLTEN11	FLTEN10	FLTEN9	FLTEN8	FLTEN7	FLTEN6	FLTEN5	FLTEN4	FLTEN3	FLTEN2	FLTEN1	FLTEN0	FFFF
C1FMSKSEL1	0418	F7MS	K<1:0>	F6MS	K<1:0>	F5MS	K<1:0>	F4MS	K<1:0>	F3MSK	<1:0>	F2MS	K<1:0>	F1MSł	<<1:0>	F0MS	<<1:0>	0000
C1FMSKSEL2	041A	F15MS	SK<1:0>	F14MS	K<1:0>	F13MS	SK<1:0>	F12MS	SK<1:0>	F11MSK	<1:0>	F10MS	K<1:0>	F9MSł	<<1:0>	F8MS	< <1:0>	0000

TABLE 4-21: ECAN1 REGISTER MAP WHEN WIN (C1CTRL1<0>) = 0 OR 1 FOR dsPIC33EPXXXMC/GP50X DEVICES ONLY

Legend: — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

TABLE 4-22: ECAN1 REGISTER MAP WHEN WIN (C1CTRL1<0>) = 0 FOR dsPIC33EPXXXMC/GP50X DEVICES ONLY

File Name	Addr	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	All Resets
	0400- 041E							S	ee definition	when WIN	= x							
C1RXFUL1	0420	RXFUL15	RXFUL14	RXFUL13	RXFUL12	RXFUL11	RXFUL10	RXFUL9	RXFUL8	RXFUL7	RXFUL6	RXFUL5	RXFUL4	RXFUL3	RXFUL2	RXFUL1	RXFUL0	0000
C1RXFUL2	0422	RXFUL31	RXFUL30	RXFUL29	RXFUL28	RXFUL27	RXFUL26	RXFUL25	RXFUL24	RXFUL23	RXFUL22	RXFUL21	RXFUL20	RXFUL19	RXFUL18	RXFUL17	RXFUL16	0000
C1RXOVF1	0428	RXOVF15	RXOVF14	RXOVF13	RXOVF12	RXOVF11	RXOVF10	RXOVF9	RXOVF8	RXOVF7	RXOVF6	RXOVF5	RXOVF4	RXOVF3	RXOVF2	RXOVF1	RXOVF0	0000
C1RXOVF2	042A	RXOVF31	RXOVF30	RXOVF29	RXOVF28	RXOVF27	RXOVF26	RXOVF25	RXOVF24	RXOVF23	RXOVF22	RXOVF21	RXOVF20	RXOVF19	RXOVF18	RXOVF17	RXOVF16	0000
C1TR01CON	0430	TXEN1	TXABT1	TXLARB1	TXERR1	TXREQ1	RTREN1	TX1PF	RI<1:0>	TXEN0	TXABAT0	TXLARB0	TXERR0	TXREQ0	RTREN0	TX0PF	RI<1:0>	0000
C1TR23CON	0432	TXEN3	TXABT3	TXLARB3	TXERR3	TXREQ3	RTREN3	TX3PF	RI<1:0>	TXEN2	TXABAT2	TXLARB2	TXERR2	TXREQ2	RTREN2	TX2PF	RI<1:0>	0000
C1TR45CON	0434	TXEN5	TXABT5	TXLARB5	TXERR5	TXREQ5	RTREN5	TX5PF	RI<1:0>	TXEN4	TXABAT4	TXLARB4	TXERR4	TXREQ4	RTREN4	TX4PF	RI<1:0>	0000
C1TR67CON	0436	TXEN7	TXABT7	TXLARB7	TXERR7	TXREQ7	RTREN7	TX7PF	RI<1:0>	TXEN6	TXABAT6	TXLARB6	TXERR6	TXREQ6	RTREN6	TX6PF	RI<1:0>	xxxx
C1RXD	0440							E	CAN1 Rece	eive Data Wo	ord							xxxx
C1TXD	0442		ECAN1 Transmit Data Word xxxx															

Legend: x = unknown value on Reset, — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

R/S-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
FORCE ⁽¹⁾	—	—	_	_	—	—	—
bit 15		·			·		bit 8
R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
IRQSEL7	IRQSEL6	IRQSEL5	IRQSEL4	IRQSEL3	IRQSEL2	IRQSEL1	IRQSEL0
bit 7		•			·		bit 0
Legend:		S = Settable b	oit				
R = Readable	bit	W = Writable	bit	U = Unimpler	mented bit, read	as '0'	
-n = Value at P	OR	'1' = Bit is set		'0' = Bit is cle	ared	x = Bit is unkr	Iown
bit 15	FORCE: Forc	e DMA Transfe	er bit ⁽¹⁾				
	1 = Forces a	single DMA tra	insfer (Manua	l mode)			
	0 = Automati	c DMA transfer	initiation by D	MA request			
bit 14-8	Unimplemen	ted: Read as '	י)				
bit 7-0	IRQSEL<7:0>	-: DMA Periphe	eral IRQ Numl	ber Select bits			
	01000110 =	ECAN1 – TX D	ata Request ⁽²	2)			
	00100110 =	IC4 – Input Caj	oture 4				
	00100101 =	IC3 – Input Ca	oture 3				
	00100010 =	ECAN1 – RX D	ata Ready ⁽²⁾				
	00100001 = 3	SPIZ Transfer I	Jone NDT2 Transmi	ittor			
	00011111 =	UART2RX - U	ART2 Receive	ar			
	0001110 = 00011100 = 000011100 = 000011000 = 00000000	TMR5 – Timer	5				
	00011011 =	TMR4 – Timer4	1				
	00011010 =	OC4 – Output	Compare 4				
	00011001 =	OC3 – Output (Compare 3				
	00001101 =	ADC1 – ADC1	Convert done	•			
	00001100 =	UART1TX – U/	ART1 Transm	itter			
	00001011 =	UART1RX – U	ART1 Receive	er			
	00001010 =	SPI1 – Transfe	r Done				
	00001000 =	TMR3 – Timera	3				
	00000111 =	100RZ - 100RZ	<u>Compore 2</u>				
	00000110 = 0	IC2 – Duipui (oture 2				
	00000101 = 0	OC1 = Outout 0	Compare 1				
	00000001 =	IC1 – Input Ca	oture 1				
	00000000 =	INT0 – Externa	I Interrupt 0				

REGISTER 8-2: DMAXREQ: DMA CHANNEL x IRQ SELECT REGISTER

- **Note 1:** The FORCE bit cannot be cleared by user software. The FORCE bit is cleared by hardware when the forced DMA transfer is complete or the channel is disabled (CHEN = 0).
 - 2: This selection is available in dsPIC33EPXXXGP/MC50X devices only.

11.4.4 INPUT MAPPING

The inputs of the Peripheral Pin Select options are mapped on the basis of the peripheral. That is, a control register associated with a peripheral dictates the pin it will be mapped to. The RPINRx registers are used to configure peripheral input mapping (see Register 11-1 through Register 11-17). Each register contains sets of 7-bit fields, with each set associated with one of the remappable peripherals. Programming a given peripheral's bit field with an appropriate 7-bit value maps the RPn pin with the corresponding value to that peripheral. For any given device, the valid range of values for any bit field corresponds to the maximum number of Peripheral Pin Selections supported by the device.

For example, Figure 11-2 illustrates remappable pin selection for the U1RX input.

FIGURE 11-2: REMAPPABLE INPUT FOR U1RX



11.4.4.1 Virtual Connections

dsPIC33EPXXXGP50X, dsPIC33EPXXXMC20X/50X and PIC24EPXXXGP/MC20X devices support virtual (internal) connections to the output of the op amp/ comparator module (see Figure 25-1 in Section 25.0 "Op Amp/Comparator Module"), and the PTG module (see Section 24.0 "Peripheral Trigger Generator (PTG) Module").

In addition, dsPIC33EPXXXMC20X/50X and PIC24EPXXXMC20X devices support virtual connections to the filtered QEI module inputs: FINDX1, FHOME1, FINDX2 and FHOME2 (see Figure 17-1 in Section 17.0 "Quadrature Encoder Interface (QEI) Module (dsPIC33EPXXXMC20X/50X and PIC24EPXXXMC20X Devices Only)".

Virtual connections provide a simple way of interperipheral connection without utilizing a physical pin. For example, by setting the FLT1R<6:0> bits of the RPINR12 register to the value of `b0000001, the output of the analog comparator, C1OUT, will be connected to the PWM Fault 1 input, which allows the analog comparator to trigger PWM Faults without the use of an actual physical pin on the device.

Virtual connection to the QEI module allows peripherals to be connected to the QEI digital filter input. To utilize this filter, the QEI module must be enabled and its inputs must be connected to a physical RPn pin. Example 11-2 illustrates how the input capture module can be connected to the QEI digital filter.

EXAMPLE 11-2: CONNECTING IC1 TO THE HOME1 QEI1 DIGITAL FILTER INPUT ON PIN 43 OF THE dsPIC33EPXXXMC206 DEVICE

RPINR15 = 0x2500;	/* Connect the QEI1 HOME1 input to RP37 (pin 43) */
RPINR7 = 0x009;	/* Connect the IC1 input to the digital filter on the FHOME1 input */
QEI1IOC = 0x4000;	/* Enable the QEI digital filter */
QEI1CON = 0x8000;	/* Enable the QEI module */

R/W-0	U-0	U-0	U-0	U-0	U-0	R/W-0	R/W-0
CHPCLKEN	—	—	—	_	—	CHOPC	LK<9:8>
bit 15							bit 8
R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
			CHOPC	LK<7:0>			
bit 7							bit 0
Legend:							
R = Readable I	oit	W = Writable	bit	U = Unimple	mented bit, read	as '0'	
-n = Value at P	OR	'1' = Bit is set		'0' = Bit is cle	eared	x = Bit is unki	nown
bit 15 bit 14-10 bit 9-0	CHPCLKEN: 1 = Chop cloc 0 = Chop cloc Unimplemen CHOPCLK<9 The frequenc Chop Frequen	Enable Chop ck generator is ck generator is ited: Read as 9:0>: Chop Clo cy of the chop c ncy = (FP/PCL	Clock Genera enabled disabled o' ock Divider bits clock signal is KDIV<2:0)/(Cl	tor bit given by the fc HOPCLK<9:0>	llowing expressi + 1)	on:	

REGISTER 16-5: CHOP: PWMx CHOP CLOCK GENERATOR REGISTER

REGISTER 16-6: MDC: PWMx MASTER DUTY CYCLE REGISTER

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
			MDC	<15:8>			
bit 15							bit 8
R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
			MDO	C<7:0>			
bit 7							bit 0
Legend:							
R = Readable	bit	W = Writable	bit	U = Unimpler	mented bit, rea	ad as '0'	
-n = Value at F	POR	'1' = Bit is set		'0' = Bit is cle	ared	x = Bit is unki	nown

bit 15-0 MDC<15:0>: PWMx Master Duty Cycle Value bits

U-0	U-0	U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0
—	—	—	_		LEB	<11:8>	
bit 15							bit 8
R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
			LEE	3<7:0>			
bit 7							bit 0
Legend:							
R = Readable	bit	W = Writable	bit	U = Unimpler	nented bit, rea	d as '0'	
-n = Value at F	POR	'1' = Bit is set		'0' = Bit is cle	ared	x = Bit is unkr	nown

REGISTER 16-17: LEBDLYx: PWMx LEADING-EDGE BLANKING DELAY REGISTER

bit 15-12 Unimplemented: Read as '0'

bit 11-0 LEB<11:0>: Leading-Edge Blanking Delay for Current-Limit and Fault Inputs bits

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
			QEIGE	EC<31:24>			
bit 15							bit 8
R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
			QEIGE	EC<23:16>			
bit 7							bit 0
Legend:							
R = Readable	bit	W = Writable	bit	U = Unimplen	nented bit, read	d as '0'	
-n = Value at	POR	'1' = Bit is set		'0' = Bit is clea	ared	x = Bit is unkr	iown

REGISTER 17-15: QEI1GECH: QEI1 GREATER THAN OR EQUAL COMPARE HIGH WORD REGISTER

bit 15-0 QEIGEC<31:16>: High Word Used to Form 32-Bit Greater Than or Equal Compare Register (QEI1GEC) bits

REGISTER 17-16: QEI1GECL: QEI1 GREATER THAN OR EQUAL COMPARE LOW WORD REGISTER

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
			QEIGE	C<15:8>			
bit 15							bit 8
R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
			QEIG	EC<7:0>			
bit 7							bit 0
Legend:							
R = Readable	bit	W = Writable	bit	U = Unimplei	mented bit, rea	id as '0'	
-n = Value at F	POR	'1' = Bit is set		'0' = Bit is cle	eared	x = Bit is unkr	nown

bit 15-0 QEIGEC<15:0>: Low Word Used to Form 32-Bit Greater Than or Equal Compare Register (QEI1GEC) bits

REGISTER 19-1: I2CxCON: I2Cx CONTROL REGISTER (CONTINUED)

bit 6	STREN: SCLx Clock Stretch Enable bit (when operating as I ² C slave) Used in conjunction with the SCLREL bit. 1 = Enables software or receives clock stretching 0 = Disables software or receives clock stretching
bit 5	ACKDT: Acknowledge Data bit (when operating as I ² C master, applicable during master receive)
	Value that is transmitted when the software initiates an Acknowledge sequence. 1 = Sends NACK during Acknowledge 0 = Sends ACK during Acknowledge
bit 4	ACKEN: Acknowledge Sequence Enable bit (when operating as I ² C master, applicable during master receive)
	 1 = Initiates Acknowledge sequence on SDAx and SCLx pins and transmits ACKDT data bit. Hardware is clear at the end of the master Acknowledge sequence. 0 = Acknowledge sequence is not in progress
bit 3	RCEN: Receive Enable bit (when operating as I ² C master)
	 1 = Enables Receive mode for I²C. Hardware is clear at the end of the eighth bit of the master receive data byte. a Receive acquirement in program.
hit 2	0 = Receive sequence is not in progress
511 2	 1 = Initiates Stop condition on SDAx and SCLx pins. Hardware is clear at the end of the master Stop sequence. a Stop condition is not in processor.
h :+ 4	0 = Stop condition is not in progress
DIT	RSEN: Repeated Start Condition Enable bit (when operating as I-C master)
	 Initiates Repeated Start condition on SDAx and SCLX pins. Hardware is clear at the end of the master Repeated Start sequence. 0 = Repeated Start condition is not in progress
bit 0	SEN: Start Condition Enable bit (when operating as l^2C master)
	 1 = Initiates Start condition on SDAx and SCLx pins. Hardware is clear at the end of the master Start sequence. 0 = Start condition is not in progress

Note 1: When performing master operations, ensure that the IPMIEN bit is set to '0'.

R-0, HSC	R-0, HSC	U-0	U-0	U-0	R/C-0, HS	R-0, HSC	R-0, HSC	
ACKSTAT	TRSTAT	_	—	—	BCL	GCSTAT	ADD10	
bit 15					•		bit 8	
R/C-0, HS	R/C-0, HS	R-0, HSC	R/C-0, HSC	R/C-0, HSC	R-0, HSC	R-0, HSC	R-0, HSC	
IWCOL	I2COV	D_A	Р	S	R_W	RBF	TBF	
bit 7							bit 0	
Legend: C = Clearable bit		HS = Hardwa	re Settable bit	HSC = Hardware Settable/Clearable bit				
R = Readable bit W = Wri		W = Writable	W = Writable bit		nented bit, read	d as '0'		
-n = Value at POR		'1' = Bit is set		'0' = Bit is cleared		x = Bit is unknown		

REGISTER 19-2: I2CxSTAT: I2Cx STATUS REGISTER

bit 15	ACKSTAT: Acknowledge Status bit (when operating as I^2C^{TM} master, applicable to master transmit operation)
	1 = NACK received from slave 0 = ACK received from slave
	Hardware is set or clear at the end of slave Acknowledge.
bit 14	TRSTAT: Transmit Status bit (when operating as I^2C master, applicable to master transmit operation) 1 = Master transmit is in progress (8 bits + ACK)
	0 = Master transmit is not in progress Hardware is set at the beginning of master transmission. Hardware is clear at the end of slave Acknowledge.
bit 13-11	Unimplemented: Read as '0'
bit 10	BCL: Master Bus Collision Detect bit
	1 = A bus collision has been detected during a master operation0 = No bus collision detected
	Hardware is set at detection of a bus collision.
bit 9	GCSTAT: General Call Status bit
	1 = General call address was received
	0 = General call address was not received
1.11.0	Hardware is set when address matches general call address. Hardware is clear at Stop detection.
DIT 8	ADD10: 10-Bit Address Status bit
	I = 10-bit address was matched 0 = 10-bit address was not matched
	Hardware is set at the match of the 2nd byte of the matched 10-bit address. Hardware is clear at Stop detection.
bit 7	IWCOL: I2Cx Write Collision Detect bit
	1 = An attempt to write to the I2CxTRN register failed because the I^2 C module is busy 0 = No collision
	Hardware is set at the occurrence of a write to I2CxTRN while busy (cleared by software).
bit 6	I2COV: I2Cx Receive Overflow Flag bit
	 1 = A byte was received while the I2CxRCV register was still holding the previous byte 0 = No overflow
	Hardware is set at an attempt to transfer I2CxRSR to I2CxRCV (cleared by software).
bit 5	D_A: Data/Address bit (when operating as I ² C slave)
	1 = Indicates that the last byte received was data
	 Indicates that the last byte received was a device address Hardware is clear at a device address match. Hardware is set by reception of a slave byte.
bit 4	P: Stop bit
	1 = Indicates that a Stop bit has been detected last
	0 = Stop bit was not detected last
	Hardware is set or clear when a Start, Repeated Start or Stop is detected.

REGISTER 20-1: UXMODE: UARTX MODE REGISTER (CONTINUED)

bit 5	ABAUD: Auto-Baud Enable bit
	 1 = Enables baud rate measurement on the next character – requires reception of a Sync field (55h) before other data; cleared in hardware upon completion 0 = Baud rate measurement is disabled or completed
bit 4	URXINV: UARTx Receive Polarity Inversion bit
	1 = UxRX Idle state is '0' 0 = UxRX Idle state is '1'
bit 3	BRGH: High Baud Rate Enable bit
	 1 = BRG generates 4 clocks per bit period (4x baud clock, High-Speed mode) 0 = BRG generates 16 clocks per bit period (16x baud clock, Standard mode)
bit 2-1	PDSEL<1:0>: Parity and Data Selection bits
	 11 = 9-bit data, no parity 10 = 8-bit data, odd parity 01 = 8-bit data, even parity 00 = 8-bit data, no parity
bit 0	STSEL: Stop Bit Selection bit
	1 = Two Stop bits 0 = One Stop bit
Note 1:	Refer to the " UART " (DS70582) section in the <i>"dsPIC33/PIC24 Family Reference Manual"</i> for information on enabling the UARTx module for receive or transmit operation.

- 2: This feature is only available for the 16x BRG mode (BRGH = 0).
- 3: This feature is only available on 44-pin and 64-pin devices.
- 4: This feature is only available on 64-pin devices.

U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0			
_	_	_	_	_	_	_	_			
bit 15							bit 8			
R/W-0	R/W-0	R/W-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0			
IVRIE	WAKIE	ERRIE	—	FIFOIE	RBOVIE	RBIE	TBIE			
bit 7					•		bit 0			
Legend:										
R = Readable	bit	W = Writable	bit	U = Unimpler	mented bit, read	as '0'				
-n = Value at F	POR	'1' = Bit is set		'0' = Bit is cle	ared	x = Bit is unkr	nown			
bit 15-8	Unimplemen	ted: Read as ')'							
bit 7	IVRIE: Invalid	I Message Inter	rupt Enable b	bit						
	1 = Interrupt request is enabled									
		request is not e	nabled							
DIT 6	WAKIE: Bus Wake-up Activity Interrupt Enable bit									
	 I = Interrupt request is enabled Interrupt request is not enabled 									
bit 5	ERRIE: Frror	Interrupt Enab	le bit							
	1 = Interrupt request is enabled									
	0 = Interrupt request is not enabled									
bit 4	Unimplemen	ted: Read as ')'							
bit 3	FIFOIE: FIFO	Almost Full Int	errupt Enable	e bit						
	1 = Interrupt request is enabled									
	0 = Interrupt request is not enabled									
bit 2	RBOVIE: RX	Buffer Overflov	v Interrupt En	able bit						
	1 = Interrupt request is patient on abled									
hit 1	0 - michapi request is not enable bit									
bit 1	1 = Interrupt request is enabled									
	0 = Interrupt request is not enabled									
bit 0	TBIE: TX Buff	fer Interrupt En	able bit							
	1 = Interrupt r	request is enab	led							
	0 = Interrupt r	request is not e	nabled							

REGISTER 21-7: CXINTE: ECANX INTERRUPT ENABLE REGISTER

R/C-0	R/C-0	R/C-0	R/C-0	R/C-0	R/C-0	R/C-0	R/C-0
RXOVF15	RXOVF14	RXOVF13	RXOVF12	RXOVF11	RXOVF10	RXOVF9	RXOVF8
bit 15							bit 8
R/C-0	R/C-0	R/C-0	R/C-0	R/C-0	R/C-0	R/C-0	R/C-0

REGISTER 21-24: CxRXOVF1: ECANx RECEIVE BUFFER OVERFLOW REGISTER 1

RXOVF4

bit 7			bit 0
Legend:	C = Writable bit, but or	nly '0' can be written to clear the bit	
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	

RXOVF3

RXOVF2

R = Readable bit	vv = vvritable bit	U = Unimplemented bit, read	as 0
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15-0 RXOVF<15:0>: Receive Buffer n Overflow bits

RXOVF6

RXOVF7

1 = Module attempted to write to a full buffer (set by module)

0 = No overflow condition (cleared by user software)

RXOVF5

REGISTER 21-25: CxRXOVF2: ECANx RECEIVE BUFFER OVERFLOW REGISTER 2

| R/C-0 |
|---------|---------|---------|---------|---------|---------|---------|---------|
| RXOVF31 | RXOVF30 | RXOVF29 | RXOVF28 | RXOVF27 | RXOVF26 | RXOVF25 | RXOVF24 |
| bit 15 | | | | | | | bit 8 |

| R/C-0 |
|---------|---------|---------|---------|---------|---------|---------|---------|
| RXOVF23 | RXOVF22 | RXOVF21 | RXOVF20 | RXOVF19 | RXOVF18 | RXOVF17 | RXOVF16 |
| bit 7 | | | | | | | bit 0 |

Legend:	C = Writable bit, but only '0	' can be written to clear the bi	t
R = Readable bit	W = Writable bit	U = Unimplemented bit, read	d as '0'
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15-0 RXOVF<31:16>: Receive Buffer n Overflow bits

1 = Module attempted to write to a full buffer (set by module)

0 = No overflow condition (cleared by user software)

RXOVF0

RXOVF1

22.2 CTMU Control Registers

REGISTER	22-1. CTWO		CONTROL	REGISTER	1				
R/W-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0		
CTMUEN		CTMUSIDL	TGEN	EDGEN	EDGSEQEN	IDISSEN ⁽¹⁾	CTTRIG		
bit 15							bit 8		
U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0		
	—	—	—	_		_			
bit 7							bit 0		
Legend:									
R = Readable	e bit	W = Writable b	it	U = Unimplemented bit, read as '0'					
-n = Value at	POR	'1' = Bit is set		'0' = Bit is cleared x = Bit is unknow			iown		
bit 15	CTMUEN: C	TMU Enable bit							
	1 = Module i	s enabled							
	0 = Module i	s disabled							
bit 14	Unimplemen	nted: Read as '0'							
bit 13	CTMUSIDL:	CTMU Stop in Id	le Mode bit						
	1 = Discontinues module operation when device enters Idle mode								
	0 = Continue	es module operat	ion in Idle mo	ode					
bit 12	TGEN: Time	Generation Enab	ole bit						
	1 = Enables	edge delay gene	eration						
	0 = Disables	edge delay gene	eration						
bit 11	EDGEN: Edg	e Enable bit							

REGISTER 22-1: CTMUCON1: CTMU CONTROL REGISTER 1

1 = Hardware modules are used to trigger edges (TMRx, CTEDx, etc.)

- 0 = Software is used to trigger edges (manual set of EDGxSTAT)
- bit 10 EDGSEQEN: Edge Sequence Enable bit
 - 1 = Edge 1 event must occur before Edge 2 event can occur
 - 0 = No edge sequence is needed
- bit 9 IDISSEN: Analog Current Source Control bit⁽¹⁾
 - 1 = Analog current source output is grounded
 - 0 = Analog current source output is not grounded
- bit 8 CTTRIG: ADC Trigger Control bit
 - 1 = CTMU triggers ADC start of conversion
 - 0 = CTMU does not trigger ADC start of conversion
- bit 7-0 Unimplemented: Read as '0'
- **Note 1:** The ADC module Sample-and-Hold capacitor is not automatically discharged between sample/conversion cycles. Software using the ADC as part of a capacitance measurement must discharge the ADC capacitor before conducting the measurement. The IDISSEN bit, when set to '1', performs this function. The ADC must be sampling while the IDISSEN bit is active to connect the discharge sink to the capacitor array.

R/W-0	U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	
ADRC	—	—	SAMC4 ⁽¹⁾	SAMC3 ⁽¹⁾	SAMC2 ⁽¹⁾	SAMC1 ⁽¹⁾	SAMC0 ⁽¹⁾	
bit 15							bit 8	
R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	
ADCS7(2	²⁾ ADCS6 ⁽²⁾	ADCS5 ⁽²⁾	ADCS4 ⁽²⁾	ADCS3 ⁽²⁾	ADCS2 ⁽²⁾	ADCS1 ⁽²⁾	ADCS0 ⁽²⁾	
bit 7							bit 0	
Legend:			••			(0)		
R = Reada		W = Writable bit			nented bit, read			
-n = value	at POR	"1" = Bit is set		$0^{\circ} = Bit is cle$	ared	x = Bit is unknown		
bit 15	ADRC: ADC1 1 = ADC inter 0 = Clock deri	ADRC: ADC1 Conversion Clock Source bit 1 = ADC internal RC clock 0 = Clock derived from system clock						
bit 14-13	Unimplement	ted: Read as '0	,					
bit 12-8	SAMC<4:0>:	Auto-Sample T	ime bits ⁽¹⁾					
	11111 = 31 T. • • • • •	AD						
h:+ 7 0	00000 = 0 IA			at hita(2)				
DIT 7-0 ADCS<7:0>: ADC1 Conversion Clock Select DIts ⁽²⁾ 11111111 = TP • (ADCS<7:0> + 1) = TP • 256 = TAD • • • • • • • • • • • • •								
Note 1: 2:	This bit is only use This bit is not used	d if SSRC<2:0> if ADRC (AD10	(AD1CON1< CON3<15>) =	7:5>) = 111 ar 1.	nd SSRCG (AD	1CON1<4>) =	0.	

REGISTER 23-3: AD1CON3: ADC1 CONTROL REGISTER 3

Base Instr #	Assembly Mnemonic		Assembly Syntax	Description	# of Words	# of Cycles ⁽²⁾	Status Flags Affected
25	DAW	DAW	Wn	Wn = decimal adjust Wn	1	1	С
26	DEC	DEC	f	f = f - 1	1	1	C,DC,N,OV,Z
		DEC	f,WREG	WREG = f – 1	1	1	C,DC,N,OV,Z
		DEC	Ws,Wd	Wd = Ws - 1	1	1	C,DC,N,OV,Z
27	DEC2	DEC2	f	f = f – 2	1	1	C,DC,N,OV,Z
		DEC2	f,WREG	WREG = f – 2	1	1	C,DC,N,OV,Z
		DEC2	Ws,Wd	Wd = Ws - 2	1	1	C,DC,N,OV,Z
28	DISI	DISI	#lit14	Disable Interrupts for k instruction cycles	1	1	None
29	DIV	DIV.S	Wm,Wn	Signed 16/16-bit Integer Divide	1	18	N,Z,C,OV
		DIV.SD	Wm,Wn	Signed 32/16-bit Integer Divide	1	18	N,Z,C,OV
		DIV.U	Wm,Wn	Unsigned 16/16-bit Integer Divide	1	18	N,Z,C,OV
		DIV.UD	Wm,Wn	Unsigned 32/16-bit Integer Divide	1	18	N,Z,C,OV
30	DIVF	DIVF	Wm, Wn ⁽¹⁾	Signed 16/16-bit Fractional Divide	1	18	N,Z,C,OV
31	DO	DO	#lit15,Expr ⁽¹⁾	Do code to PC + Expr, lit15 + 1 times	2	2	None
		DO	Wn,Expr ⁽¹⁾	Do code to PC + Expr, (Wn) + 1 times	2	2	None
32	ED	ED	Wm*Wm,Acc,Wx,Wy,Wxd ⁽¹⁾	Euclidean Distance (no accumulate)	1	1	OA,OB,OAB, SA,SB,SAB
33	EDAC	EDAC	Wm*Wm,Acc,Wx,Wy,Wxd ⁽¹⁾	Euclidean Distance	1	1	OA,OB,OAB, SA,SB,SAB
34	EXCH	EXCH	Wns,Wnd	Swap Wns with Wnd	1	1	None
35	FBCL	FBCL	Ws,Wnd	Find Bit Change from Left (MSb) Side	1	1	С
36	FF1L	FF1L	Ws,Wnd	Find First One from Left (MSb) Side	1	1	С
37	FF1R	FF1R	Ws,Wnd	Find First One from Right (LSb) Side	1	1	С
38	GOTO	GOTO	Expr	Go to address	2	4	None
		GOTO	Wn	Go to indirect	1	4	None
		GOTO.L	Wn	Go to indirect (long address)	1	4	None
39	INC	INC	INC f f=f+1		1	1	C,DC,N,OV,Z
		INC	f,WREG	WREG = f + 1	1	1	C,DC,N,OV,Z
		INC	Ws,Wd	Wd = Ws + 1	1	1	C,DC,N,OV,Z
40	INC2	INC2	f	f = f + 2	1	1	C,DC,N,OV,Z
		INC2	f,WREG	WREG = f + 2	1	1	C,DC,N,OV,Z
		INC2	Ws,Wd	Wd = Ws + 2	1	1	C,DC,N,OV,Z
41	IOR	IOR	f	f = f .IOR. WREG	1	1	N,Z
		IOR	f,WREG	WREG = f.IOR. WREG	1	1	N,Z
		IOR	#lit10,Wn	Wd = lit10 .IOR. Wd	1	1	N,Z
		IOR	Wb,Ws,Wd	Wd = Wb .IOR. Ws	1	1	N,Z
		IOR	Wb,#lit5,Wd	Wd = Wb .IOR. lit5	1	1	N,Z
42	LAC	LAC	Wso,#Slit4,Acc	Load Accumulator	1	1	OA,OB,OAB, SA,SB,SAB
43	LNK	LNK	#lit14	Link Frame Pointer	1	1	SFA
44	LSR	LSR	f	f = Logical Right Shift f	1	1	C,N,OV,Z
		LSR	f,WREG	WREG = Logical Right Shift f	1	1	C,N,OV,Z
		LSR	Ws,Wd	Wd = Logical Right Shift Ws	1	1	C,N,OV,Z
		LSR	Wb,Wns,Wnd	Wnd = Logical Right Shift Wb by Wns	1	1	N,Z
		LSR	Wb,#lit5,Wnd	Wnd = Logical Right Shift Wb by lit5	1	1	N,Z
45	MAC	MAC Wm*Wn, Acc, Wx, Wxd, Wy, Wyd, AWB ⁽¹⁾ Multiply and Accumulate		Multiply and Accumulate	1	1	OA,OB,OAB, SA,SB,SAB
		MAC	Wm^*Wm , Acc, Wx, Wxd, Wy, Wyd ⁽¹⁾	Square and Accumulate	1	1	OA,OB,OAB, SA,SB,SAB

TABLE 28-2: INSTRUCTION SET OVERVIEW (CONTINUED)

Note 1: These instructions are available in dsPIC33EPXXXMC20X/50X and PIC24EPXXXMC20X devices only.

2: Read and Read-Modify-Write (e.g., bit operations and logical operations) on non-CPU SFRs incur an additional instruction cycle.

AC CHARACTERISTICS			$\begin{tabular}{lllllllllllllllllllllllllllllllllll$					
Maximum Data Rate	Master Transmit Only (Half-Duplex)	Master Transmit/Receive (Full-Duplex)	Slave Transmit/Receive CKE CKP S (Full-Duplex)		SMP			
15 MHz	Table 30-33		_	0,1	0,1	0,1		
9 MHz	—	Table 30-34	—	1	0,1	1		
9 MHz	—	Table 30-35	—	0	0,1	1		
15 MHz	—	—	Table 30-36	1	0	0		
11 MHz	—	—	Table 30-37	1	1	0		
15 MHz		_	Table 30-38	0	1	0		
11 MHz	_	_	Table 30-39	0	0	0		

TABLE 30-33: SPI2 MAXIMUM DATA/CLOCK RATE SUMMARY

FIGURE 30-14: SPI2 MASTER MODE (HALF-DUPLEX, TRANSMIT ONLY, CKE = 0) TIMING CHARACTERISTICS



TABLE 30-38:SPI2 SLAVE MODE (FULL-DUPLEX, CKE = 1, CKP = 1, SMP = 0)TIMING REQUIREMENTS

AC CHARACTERISTICS			Standard Operating Conditions: 3.0V to 3.6V (unless otherwise stated) Operating temperature $-40^{\circ}C \le TA \le +85^{\circ}C$ for Industrial $-40^{\circ}C \le TA \le +125^{\circ}C$ for Extended				
Param.	Symbol	Characteristic ⁽¹⁾	Min.	Typ. ⁽²⁾	Max.	Units	Conditions
SP70	FscP	Maximum SCK2 Input Frequency	_		Lesser of FP or 11	MHz	(Note 3)
SP72	TscF	SCK2 Input Fall Time	—	_	_	ns	See Parameter DO32 (Note 4)
SP73	TscR	SCK2 Input Rise Time	—	_	_	ns	See Parameter DO31 (Note 4)
SP30	TdoF	SDO2 Data Output Fall Time	—			ns	See Parameter DO32 (Note 4)
SP31	TdoR	SDO2 Data Output Rise Time	—			ns	See Parameter DO31 (Note 4)
SP35	TscH2doV, TscL2doV	SDO2 Data Output Valid after SCK2 Edge	—	6	20	ns	
SP36	TdoV2scH, TdoV2scL	SDO2 Data Output Setup to First SCK2 Edge	30	_	_	ns	
SP40	TdiV2scH, TdiV2scL	Setup Time of SDI2 Data Input to SCK2 Edge	30			ns	
SP41	TscH2diL, TscL2diL	Hold Time of SDI2 Data Input to SCK2 Edge	30	_	_	ns	
SP50	TssL2scH, TssL2scL	SS2 ↓ to SCK2 ↑ or SCK2 ↓ Input	120	_	-	ns	
SP51	TssH2doZ	SS2 ↑ to SDO2 Output High-Impedance	10	_	50	ns	(Note 4)
SP52	TscH2ssH TscL2ssH	SS2 ↑ after SCK2 Edge	1.5 TCY + 40	_	_	ns	(Note 4)
SP60	TssL2doV	SDO2 Data Output Valid after SS2 Edge	—	_	50	ns	

Note 1: These parameters are characterized, but are not tested in manufacturing.

2: Data in "Typical" column is at 3.3V, +25°C unless otherwise stated.

3: The minimum clock period for SCK2 is 91 ns. Therefore, the SCK2 clock generated by the master must not violate this specification.

4: Assumes 50 pF load on all SPI2 pins.

44-Lead Plastic Thin Quad Flatpack (PT) – 10x10x1 mm Body, 2.00 mm [TQFP]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



	MILLIMETERS				
	MIN	NOM	MAX		
Number of Leads	N				
Lead Pitch	e	0.80 BSC			
Overall Height	A	-	-	1.20	
Molded Package Thickness	A2	0.95	1.00	1.05	
Standoff	A1	0.05	-	0.15	
Foot Length	L	0.45	0.60	0.75	
Footprint	L1	1.00 REF			
Foot Angle	ф	0° 3.5° 7°			
Overall Width	E	12.00 BSC			
Overall Length D 12.00 BSC					
Molded Package Width	E1	E1 10.00 BSC			
Molded Package Length	D1	10.00 BSC			
Lead Thickness	С	0.09	-	0.20	
Lead Width	b	0.30	0.37	0.45	
Mold Draft Angle Top	α	11° 12° 13°			
Mold Draft Angle Bottom	β	11°	12°	13°	

Notes:

1. Pin 1 visual index feature may vary, but must be located within the hatched area.

2. Chamfers at corners are optional; size may vary.

3. Dimensions D1 and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.25 mm per side.

4. Dimensioning and tolerancing per ASME Y14.5M.

BSC: Basic Dimension. Theoretically exact value shown without tolerances.

REF: Reference Dimension, usually without tolerance, for information purposes only.

Microchip Technology Drawing C04-076B