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"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "<u>Embedded -</u> <u>Microcontrollers</u>"

#### Details

E·XFI

Product Status	Active
Core Processor	PIC
Core Size	16-Bit
Speed	70 MIPs
Connectivity	I <sup>2</sup> C, IrDA, LINbus, QEI, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, DMA, Motor Control PWM, POR, PWM, WDT
Number of I/O	21
Program Memory Size	32KB (10.7K x 24)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	2K x 16
Voltage - Supply (Vcc/Vdd)	3V ~ 3.6V
Data Converters	A/D 6x10b/12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	28-SOIC (0.295", 7.50mm Width)
Supplier Device Package	28-SOIC
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/pic24ep32mc202-i-so

Email: info@E-XFL.COM

Address: Room A, 16/F, Full Win Commercial Centre, 573 Nathan Road, Mongkok, Hong Kong

#### 3.7 CPU Control Registers

R/W-0	) R/W-0	R/W-0	R/W-0	R/C-0	R/C-0	R-0	R/W-0
0A <sup>(1)</sup>	OB <sup>(1)</sup>	SA <sup>(1,4)</sup>	SB <sup>(1,4)</sup>	OAB <sup>(1)</sup>	SAB <sup>(1)</sup>	DA <sup>(1)</sup>	DC
bit 15							bit 8
R/W-0 <sup>(2</sup>	R/W-0 <sup>(2,3)</sup>	R/W-0 <sup>(2,3)</sup>	R-0	R/W-0	R/W-0	R/W-0	R/W-0
IPL2	IPL1	IPL0	RA	N	OV	Z	С
bit 7							bit 0
Legend:		C = Clearable	bit				
R = Reada	able bit	W = Writable	bit	U = Unimpler	mented bit, read	l as '0'	
-n = Value	e at POR	'1'= Bit is set		'0' = Bit is cle	ared	x = Bit is unkr	nown
bit 15	OA: Accumu	lator A Overflow	v Status bit <sup>(1)</sup>				
	1 = Accumula	ator A has over	flowed				
	0 = Accumula	ator A has not c	verflowed				
bit 14	OB: Accumu	lator B Overflov	v Status bit <sup>(1)</sup>				
	1 = Accumula	ator B has over	flowed				
hit 13		lator A Saturatio	n 'Sticky' Sta	tue hit(1,4)			
DIL 15	$1 = \Delta c cumula$	ator A is saturat	ed or has her	n saturated at	some time		
	0 = Accumula	ator A is not sat	urated		Some time		
bit 12	SB: Accumu	lator B Saturatio	on 'Sticky' Sta	tus bit <sup>(1,4)</sup>			
	1 = Accumula	ator B is satura	ed or has bee	en saturated at	some time		
	0 = Accumula	ator B is not sat	urated				
bit 11	<b>OAB:</b> OA    (	OB Combined A	ccumulator O	verflow Status	bit <sup>(1)</sup>		
	1 = Accumula	ators A or B have	ve overflowed				
	0 = Neither A	Accumulators A	or B have ove	erflowed	(1)		
bit 10	SAB: SA    S	B Combined A	cumulator 'Si	icky Status bit		<b>1</b>	
	1 = Accumula  0 = Neither A	ators A or B are	or B are satur	nave been sat	urated at some	time	
hit 9		Active hit(1)		alou			
bit 0	1 = DO loop is	s in progress					
	0 = DO loop is	s not in progres	S				
bit 8	DC: MCU AL	U Half Carry/Bo	orrow bit				
	1 = A carry-o	out from the 4th	low-order bit (	for byte-sized o	data) or 8th low-	order bit (for wo	ord-sized data)
	of the re	sult occurred					
	0 = No carry	-out from the 4	th low-order t	bit (for byte-siz	ed data) or 8th	low-order bit (1	for word-sized
	uala) U						
Note 1:	This bit is availabl	e on dsPIC33E	PXXXMC20X	/50X and dsPl	C33EPXXXGP	50X devices on	ly.
2:	The IPL<2:0> bits	are concatenat	ed with the IF	PL<3> bit (COR	RCON<3>) to fo	rm the CPU Inte	errupt Priority
	Level. The value I IPL< $3 > = 1$ .	n parentheses i	naicates the I	PL, IT IPL<3> =	= ⊥. User interru	ipts are disable	a wnen

#### REGISTER 3-1: SR: CPU STATUS REGISTER

- 3: The IPL<2:0> Status bits are read-only when the NSTDIS bit (INTCON1<15>) = 1.
- **4:** A data write to the SR register can modify the SA and SB bits by either a data write to SA and SB or by clearing the SAB bit. To avoid a possible SA or SB bit write race condition, the SA and SB bits should not be modified using bit operations.





U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0	
_	—	—	—	—	—	—	—	
bit 15							bit 8	
U-0	U-0	U-0	U-0	R-0	R-0	R-0	R-0	
—	_	—	—	PWCOL3	PWCOL2	PWCOL1	PWCOL0	
bit 7							bit 0	
Legend:								
R = Readable	bit	W = Writable	bit	U = Unimplemented bit, read as '0'				
-n = Value at P	POR	'1' = Bit is set	'0' = Bit is cleared		x = Bit is unknown			
bit 15-4	Unimplemen	ted: Read as '	0'					
bit 3	PWCOL3: DN	VA Channel 3 F	Peripheral Wri	te Collision Fla	ag bit			
	1 = Write col	lision is detecte	ed					
	0 = No write	collision is dete	ected					
bit 2	PWCOL2: DN	MA Channel 2 I	Peripheral Wri	te Collision Fla	ag bit			
1 = Write collision is detected								
	0 = No write collision is detected							
bit 1 <b>PWCOL1:</b> DMA Channel 1 Peripheral Write Collision Flag bit								
	1 = Write col	lision is detecte	ed					
h:+ 0					h-14			
DIT U			Peripheral vvri	te Collision Fla	ag dit			
	$\perp = \text{VVrite COI}$	collision is detected	eted					

# REGISTER 8-11: DMAPWC: DMA PERIPHERAL WRITE COLLISION STATUS REGISTER

#### 10.3 Doze Mode

The preferred strategies for reducing power consumption are changing clock speed and invoking one of the powersaving modes. In some circumstances, this cannot be practical. For example, it may be necessary for an application to maintain uninterrupted synchronous communication, even while it is doing nothing else. Reducing system clock speed can introduce communication errors, while using a power-saving mode can stop communications completely.

Doze mode is a simple and effective alternative method to reduce power consumption while the device is still executing code. In this mode, the system clock continues to operate from the same source and at the same speed. Peripheral modules continue to be clocked at the same speed, while the CPU clock speed is reduced. Synchronization between the two clock domains is maintained, allowing the peripherals to access the SFRs while the CPU executes code at a slower rate.

Doze mode is enabled by setting the DOZEN bit (CLKDIV<11>). The ratio between peripheral and core clock speed is determined by the DOZE<2:0> bits (CLKDIV<14:12>). There are eight possible configurations, from 1:1 to 1:128, with 1:1 being the default setting.

Programs can use Doze mode to selectively reduce power consumption in event-driven applications. This allows clock-sensitive functions, such as synchronous communications, to continue without interruption while the CPU Idles, waiting for something to invoke an interrupt routine. An automatic return to full-speed CPU operation on interrupts can be enabled by setting the ROI bit (CLKDIV<15>). By default, interrupt events have no effect on Doze mode operation.

For example, suppose the device is operating at 20 MIPS and the ECAN<sup>™</sup> module has been configured for 500 kbps, based on this device operating speed. If the device is placed in Doze mode with a clock frequency ratio of 1:4, the ECAN module continues to communicate at the required bit rate of 500 kbps, but the CPU now starts executing instructions at a frequency of 5 MIPS.

#### 10.4 Peripheral Module Disable

The Peripheral Module Disable (PMD) registers provide a method to disable a peripheral module by stopping all clock sources supplied to that module. When a peripheral is disabled using the appropriate PMD control bit, the peripheral is in a minimum power consumption state. The control and status registers associated with the peripheral are also disabled, so writes to those registers do not have effect and read values are invalid.

A peripheral module is enabled only if both the associated bit in the PMD register is cleared and the peripheral is supported by the specific dsPIC<sup>®</sup> DSC variant. If the peripheral is present in the device, it is enabled in the PMD register by default.

Note:	If a PMD bit is set, the corresponding
	module is disabled after a delay of one
	instruction cycle. Similarly, if a PMD bit is
	cleared, the corresponding module is
	enabled after a delay of one instruction
	cycle (assuming the module control regis-
	ters are already configured to enable
	module operation).

#### 10.5 Power-Saving Resources

Many useful resources are provided on the main product page of the Microchip web site for the devices listed in this data sheet. This product page, which can be accessed using this link, contains the latest updates and additional information.



#### 10.5.1 KEY RESOURCES

- "Watchdog Timer and Power-Saving Modes" (DS70615) in the "dsPIC33/PIC24 Family Reference Manual"
- Code Samples
- Application Notes
- Software Libraries
- Webinars
- All Related "dsPIC33/PIC24 Family Reference Manual" Sections
- Development Tools

U-0	U-0	U-0	U-0	U-0	R/W-0	R/W-0	R/W-0	
_	—	—	_	—	PWM3MD <sup>(1)</sup>	PWM2MD <sup>(1)</sup>	PWM1MD <sup>(1)</sup>	
bit 15							bit 8	
U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0	
—	—		_		_			
bit 7							bit 0	
Legend:								
R = Readab	ole bit	W = Writable	bit	U = Unimplemented bit, read as '0'				
-n = Value a	at POR	'1' = Bit is set		'0' = Bit is cleared		x = Bit is unknown		
bit 15-11	Unimplemen	ted: Read as '	0'					
bit 10	PWM3MD: P	WM3 Module D	)isable bit <sup>(1)</sup>					
	1 = PWM3 mo	odule is disable	ed					
	0 = PWM3 mo	odule is enable	d					
bit 9	PWM2MD: P	WM2 Module D	isable bit <sup>(1)</sup>					
1 = PWM2 module is disa		odule is disable	ed					
	0 = PWM2 mc	odule is enable	d					
bit 8	PWM1MD: P	WM1 Module D	isable bit <sup>(1)</sup>					
	1 = PWM1 mo	odule is disable	ed					
	0 = PWM1 mo	odule is enable	d					
bit 7-0	Unimplemen	ted: Read as '	0'					

# REGISTER 10-5: PMD6: PERIPHERAL MODULE DISABLE CONTROL REGISTER 6

Note 1: This bit is available on dsPIC33EPXXXMC50X/20X and PIC24EPXXXMC20X devices only.

#### 11.4.4 INPUT MAPPING

The inputs of the Peripheral Pin Select options are mapped on the basis of the peripheral. That is, a control register associated with a peripheral dictates the pin it will be mapped to. The RPINRx registers are used to configure peripheral input mapping (see Register 11-1 through Register 11-17). Each register contains sets of 7-bit fields, with each set associated with one of the remappable peripherals. Programming a given peripheral's bit field with an appropriate 7-bit value maps the RPn pin with the corresponding value to that peripheral. For any given device, the valid range of values for any bit field corresponds to the maximum number of Peripheral Pin Selections supported by the device.

For example, Figure 11-2 illustrates remappable pin selection for the U1RX input.

#### FIGURE 11-2: REMAPPABLE INPUT FOR U1RX



#### 11.4.4.1 Virtual Connections

dsPIC33EPXXXGP50X, dsPIC33EPXXXMC20X/50X and PIC24EPXXXGP/MC20X devices support virtual (internal) connections to the output of the op amp/ comparator module (see Figure 25-1 in Section 25.0 "Op Amp/Comparator Module"), and the PTG module (see Section 24.0 "Peripheral Trigger Generator (PTG) Module").

In addition, dsPIC33EPXXXMC20X/50X and PIC24EPXXXMC20X devices support virtual connections to the filtered QEI module inputs: FINDX1, FHOME1, FINDX2 and FHOME2 (see Figure 17-1 in Section 17.0 "Quadrature Encoder Interface (QEI) Module (dsPIC33EPXXXMC20X/50X and PIC24EPXXXMC20X Devices Only)".

Virtual connections provide a simple way of interperipheral connection without utilizing a physical pin. For example, by setting the FLT1R<6:0> bits of the RPINR12 register to the value of `b0000001, the output of the analog comparator, C1OUT, will be connected to the PWM Fault 1 input, which allows the analog comparator to trigger PWM Faults without the use of an actual physical pin on the device.

Virtual connection to the QEI module allows peripherals to be connected to the QEI digital filter input. To utilize this filter, the QEI module must be enabled and its inputs must be connected to a physical RPn pin. Example 11-2 illustrates how the input capture module can be connected to the QEI digital filter.

# EXAMPLE 11-2: CONNECTING IC1 TO THE HOME1 QEI1 DIGITAL FILTER INPUT ON PIN 43 OF THE dsPIC33EPXXXMC206 DEVICE

RPINR15 = 0x2500;	/* Connect the QEI1 HOME1 input to RP37 (pin 43) */
RPINR7 = 0x009;	/* Connect the IC1 input to the digital filter on the FHOME1 input */
QEI1IOC = 0x4000;	/* Enable the QEI digital filter */
QEI1CON = 0x8000;	/* Enable the QEI module */

U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
				SCK2INR<6:0	>		
bit 15	·						bit 8
U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
—				SDI2R<6:0>			
bit 7							bit 0
Legend:							
R = Readab	le bit	W = Writable	bit	U = Unimplen	nented bit, rea	ad as '0'	
-n = Value a	t POR	'1' = Bit is set		'0' = Bit is cle	ared	x = Bit is unkı	nown
1.11.4 F			- <sup>1</sup>				
DIT 15	Unimpleme	nted: Read as	0.				
bit 14-8	SCK2INR<6 (see Table 1	5:0>: Assign SPI 1-2 for input pin	2 Clock Input selection nur	t (SCK2) to the mbers)	Correspondin	g RPn Pin bits	
	1111001 =	Input tied to RPI	121				
	•						
	0000001 =	Input tied to CM	P1				
	0000000 =	Input fied to Vss					
bit 7	Unimpleme	nted: Read as	0'				
bit 6-0	SDI2R<6:0> (see Table 1	<ul> <li>Assign SPI2 D</li> <li>1-2 for input pin</li> </ul>	ata Input (SE selection nur	012) to the Corre nbers)	esponding RP	n Pin bits	
	1111001 =	Input tied to RPI	121				
	•						
	0000001 =	Input tied to CM	P1				
	0000000 =	Input tied to Vss					

#### REGISTER 11-12: RPINR22: PERIPHERAL PIN SELECT INPUT REGISTER 22

U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	
—	—		RP43R<5:0>					
bit 15							bit 8	
U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	
—	—	RP42R<5:0>						

#### REGISTER 11-22: RPOR4: PERIPHERAL PIN SELECT OUTPUT REGISTER 4

bit	7

Legend:					
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'			
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown		

bit 15-14	Unimplemented: Read as '0'
bit 13-8	<b>RP43R&lt;5:0&gt;:</b> Peripheral Output Function is Assigned to RP43 Output Pin bits (see Table 11-3 for peripheral function numbers)
bit 7-6	Unimplemented: Read as '0'
bit 5-0	<b>RP42R&lt;5:0&gt;:</b> Peripheral Output Function is Assigned to RP42 Output Pin bits (see Table 11-3 for peripheral function numbers)

#### REGISTER 11-23: RPOR5: PERIPHERAL PIN SELECT OUTPUT REGISTER 5

U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	
—	—		RP55R<5:0>					
bit 15							bit 8	

U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
—	—			RP54	R<5:0>		
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read	l as '0'
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15-14	Unimplemented: Read as '0'
bit 13-8	<b>RP55R&lt;5:0&gt;:</b> Peripheral Output Function is Assigned to RP55 Output Pin bits (see Table 11-3 for peripheral function numbers)
bit 7-6	Unimplemented: Read as '0'
bit 5-0	<b>RP54R&lt;5:0&gt;:</b> Peripheral Output Function is Assigned to RP54 Output Pin bits (see Table 11-3 for peripheral function numbers)

bit 0

# 13.0 TIMER2/3 AND TIMER4/5

- Note 1: This data sheet summarizes the features of the dsPIC33EPXXXGP50X, dsPIC33EPXXXMC20X/50X and PIC24EPXXXGP/MC20X family of devices. It is not intended to be a comprehensive reference source. To complement the information in this data sheet, refer to "Timers" (DS70362) of the "dsPIC33/PIC24 Family Reference Manual", which is available from the Microchip web site (www.microchip.com).
  - 2: Some registers and associated bits described in this section may not be available on all devices. Refer to **Section 4.0 "Memory Organization"** in this data sheet for device-specific register and bit information.

The Timer2/3 and Timer4/5 modules are 32-bit timers, which can also be configured as four independent 16-bit timers with selectable operating modes.

As 32-bit timers, Timer2/3 and Timer4/5 operate in three modes:

- Two Independent 16-Bit Timers (e.g., Timer2 and Timer3) with all 16-Bit Operating modes (except Asynchronous Counter mode)
- Single 32-Bit Timer
- Single 32-Bit Synchronous Counter
- They also support these features:
- Timer Gate Operation
- Selectable Prescaler Settings
- Timer Operation during Idle and Sleep modes
- Interrupt on a 32-Bit Period Register Match
- Time Base for Input Capture and Output Compare Modules (Timer2 and Timer3 only)
- ADC1 Event Trigger (32-bit timer pairs, and Timer3 and Timer5 only)

Individually, all four of the 16-bit timers can function as synchronous timers or counters. They also offer the features listed previously, except for the event trigger; this is implemented only with Timer2/3. The operating modes and enabled features are determined by setting the appropriate bit(s) in the T2CON, T3CON, and T4CON, T5CON registers. T2CON and T4CON are shown in generic form in Register 13-1. T3CON and T5CON are shown in Register 13-2.

For 32-bit timer/counter operation, Timer2 and Timer4 are the least significant word (lsw); Timer3 and Timer5 are the most significant word (msw) of the 32-bit timers.

Note: For 32-bit operation, T3CON and T5CON control bits are ignored. Only T2CON and T4CON control bits are used for setup and control. Timer2 and Timer4 clock and gate inputs are utilized for the 32-bit timer modules, but an interrupt is generated with the Timer3 and Timer5 interrupt flags.

A block diagram for an example 32-bit timer pair (Timer2/3 and Timer4/5) is shown in Figure 13-3.

Note: Only Timer2, 3, 4 and 5 can trigger a DMA data transfer.

#### **REGISTER 15-1: OCxCON1: OUTPUT COMPARE x CONTROL REGISTER 1 (CONTINUED)**

- bit 3 TRIGMODE: Trigger Status Mode Select bit
  - 1 = TRIGSTAT (OCxCON2<6>) is cleared when OCxRS = OCxTMR or in software
  - 0 = TRIGSTAT is cleared only by software
- bit 2-0 OCM<2:0>: Output Compare x Mode Select bits
  - 111 = Center-Aligned PWM mode: Output set high when OCxTMR = OCxR and set low when OCxTMR = OCxRS<sup>(1)</sup>
  - 110 = Edge-Aligned PWM mode: Output set high when OCxTMR = 0 and set low when OCxTMR = OCxR<sup>(1)</sup>
  - 101 = Double Compare Continuous Pulse mode: Initializes OCx pin low, toggles OCx state continuously on alternate matches of OCxR and OCxRS
  - 100 = Double Compare Single-Shot mode: Initializes OCx pin low, toggles OCx state on matches of OCxR and OCxRS for one cycle
  - 011 = Single Compare mode: Compare event with OCxR, continuously toggles OCx pin
  - 010 = Single Compare Single-Shot mode: Initializes OCx pin high, compare event with OCxR, forces OCx pin low
  - 001 = Single Compare Single-Shot mode: Initializes OCx pin low, compare event with OCxR, forces OCx pin high
  - 000 = Output compare channel is disabled
- Note 1: OCxR and OCxRS are double-buffered in PWM mode only.
  - 2: Each Output Compare x module (OCx) has one PTG clock source. See Section 24.0 "Peripheral Trigger Generator (PTG) Module" for more information.
    - PTGO4 = OC1 PTGO5 = OC2
    - PTGO6 = OC3 PTGO7 = OC4

REGISTER 16-2: PTCON2: PWMx PRIMARY MASTER CLOCK DIVIDER SELECT REGISTER
--

U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
—	—	—	_	_	—	—	—
bit 15							bit 8
U-0	U-0	U-0	U-0	U-0	R/W-0	R/W-0	R/W-0
	_	—	—	—	PCLKDIV2 <sup>(1)</sup>	PCLKDIV1 <sup>(1)</sup>	PCLKDIV0(1)
bit 7							bit 0
Legend:							
R = Readable	bit	W = Writable	bit	U = Unimpler	mented bit, read	as '0'	
-n = Value at F	POR	'1' = Bit is set		'0' = Bit is cle	ared	x = Bit is unkn	iown
bit 15 2	Unimplomon	tod. Dood on '	۰ <b>'</b>				

#### bit 15-3 Unimplemented: Read as '0'

bit 2-0 PCLKDIV<2:0>: PWMx Input Clock Prescaler (Divider) Select bits<sup>(1)</sup>

- 111 = Reserved 110 = Divide-by-64 101 = Divide-by-32
- 100 = Divide-by-32100 = Divide-by-16
- 011 = Divide-by-8
- 010 = Divide-by-4
- 001 = Divide-by-2
- 000 = Divide-by-1, maximum PWMx timing resolution (power-on default)
- **Note 1:** These bits should be changed only when PTEN = 0. Changing the clock selection during operation will yield unpredictable results.

#### REGISTER 16-7: PWMCONx: PWMx CONTROL REGISTER (CONTINUED)

bit 7-6	6	DTC<1:0>: Dead-Time Control bits
		11 = Dead-Time Compensation mode
		10 = Dead-time function is disabled
		01 = Negative dead time is actively applied for Complementary Output mode
		0.0 = Positive dead time is actively applied for all output modes
bit 5		<b>DTCP:</b> Dead-Time Compensation Polarity bit <sup>13</sup>
		When Set to '1':
		If DTCMPx = 0, PWMxL is shortened and PWMxH is lengthened. If DTCMPx = 1, PWMxH is shortened and PWMxL is lengthened.
		When Set to '0':
		If DTCMPx = 0, PWMxH is shortened and PWMxL is lengthened.
		If DTCMPx = 1, PWMxL is shortened and PWMxH is lengthened.
bit 4		Unimplemented: Read as '0'
bit 3		MTBS: Master Time Base Select bit
		<ul> <li>1 = PWM generator uses the secondary master time base for synchronization and as the clock source for the PWM generation logic (if secondary time base is available)</li> </ul>
		0 = PWM generator uses the primary master time base for synchronization and as the clock source for the PWM generation logic
bit 2		CAM: Center-Aligned Mode Enable bit <sup>(2,4)</sup>
		1 = Center-Aligned mode is enabled
		0 = Edge-Aligned mode is enabled
bit 1		XPRES: External PWMx Reset Control bit <sup>(5)</sup>
		1 = Current-limit source resets the time base for this PWM generator if it is in Independent Time Base mode
		0 = External pins do not affect PWMx time base
bit 0		IUE: Immediate Update Enable bit <sup>(2)</sup>
		1 = Updates to the active MDC/PDCx/DTRx/ALTDTRx/PHASEx registers are immediate
		<ul> <li>Updates to the active MDC/PDCx/DTRx/ALTDTRx/PHASEx registers are synchronized to the PWMx period boundary</li> </ul>
Note	1:	Software must clear the interrupt status here and in the corresponding IFSx bit in the interrupt controller.
	2:	These bits should not be changed after the PWMx is enabled (PTEN = 1).
	3:	DTC<1:0> = 11 for DTCP to be effective; otherwise, DTCP is ignored.
	4:	The Independent Time Base (ITB = 1) mode must be enabled to use Center-Aligned mode. If ITB = 0, the CAM bit is ignored.

**5:** To operate in External Period Reset mode, the ITB bit must be '1' and the CLMOD bit in the FCLCONx register must be '0'.

U-0	U-0	U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0
	—	—	_		LEB	<11:8>	
bit 15							bit 8
R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
			LEE	3<7:0>			
bit 7							bit 0
Legend:							
R = Readable	bit	W = Writable	bit	U = Unimpler	nented bit, rea	d as '0'	
-n = Value at F	POR	'1' = Bit is set		'0' = Bit is cle	ared	x = Bit is unkr	nown

# REGISTER 16-17: LEBDLYx: PWMx LEADING-EDGE BLANKING DELAY REGISTER

bit 15-12 Unimplemented: Read as '0'

bit 11-0 LEB<11:0>: Leading-Edge Blanking Delay for Current-Limit and Fault Inputs bits

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	
	F15B	P<3:0>	F14BP<3:0>					
bit 15							bit 8	
R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	
-	F13B	P<3:0>			F12B	P<3:0>		
bit 7							bit 0	
Legend:								
R = Readab	le bit	W = Writable	bit	U = Unimpler	nented bit, rea	d as '0'		
-n = Value a	t POR	'1' = Bit is set	t	'0' = Bit is cle	ared	x = Bit is unki	nown	
L								
bit 15-12	F15BP<3:0	>: RX Buffer Ma	sk for Filter 1	5 bits				
	1111 = Filte	er hits received in	n RX FIFO bu	uffer				
	1110 = Filte	r hits received in	n RX Buffer 1	4				
	•							
	•							
	•	n hito no ocivio d iv						
	0001 = Filte	r hits received ii						
h:+ 44 0				4 h:ta (a a ma a ma)				
DIT 11-8	F14BP<3:0	>: RX Buffer Ma	SK for Fliter 1	4 bits (same va	iues as bits<15	):12>)		
bit 7-4	F13BP<3:0	>: RX Buffer Ma	sk for Filter 1	3 bits (same va	lues as bits<15	5:12>)		
bit 3-0	F12BP<3:0	RX Buffer Ma	<b>2BP&lt;3:0&gt;:</b> RX Buffer Mask for Filter 12 bits (same values as bits<15:12>)					

#### REGISTER 21-15: CxBUFPNT4: ECANx FILTER 12-15 BUFFER POINTER REGISTER 4

#### REGISTER 21-17: CxRXFnEID: ECANx ACCEPTANCE FILTER n EXTENDED IDENTIFIER REGISTER (n = 0-15)

R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x
EID15	EID14	EID13	EID12	EID11	EID10	EID9	EID8
bit 15							bit 8

| R/W-x |
|-------|-------|-------|-------|-------|-------|-------|-------|
| EID7  | EID6  | EID5  | EID4  | EID3  | EID2  | EID1  | EID0  |
| bit 7 |       |       |       |       |       |       | bit 0 |

# Legend:R = Readable bitW = Writable bitU = Unimplemented bit, read as '0'-n = Value at POR'1' = Bit is set'0' = Bit is clearedx = Bit is unknown

bit 15-0 EID<15:0>: Extended Identifier bits

1 = Message address bit, EIDx, must be '1' to match filter

0 = Message address bit, EIDx, must be '0' to match filter

#### REGISTER 21-18: CxFMSKSEL1: ECANx FILTER 7-0 MASK SELECTION REGISTER 1

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
F7M	SK<1:0>	F6MSI	K<1:0>	F5MS	K<1:0>	F4MS	K<1:0>
bit 15							bit 8
R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
F3M	SK<1:0>	F2MSI	K<1:0>	F1MS	K<1:0>	F0MS	K<1:0>
bit 7							bit 0
Legend:							
R = Readabl	le bit	W = Writable	bit	U = Unimplen	nented bit, rea	d as '0'	
-n = Value at	t POR	'1' = Bit is set	:	'0' = Bit is clea	ared	x = Bit is unkr	nown
bit 15-14	<b>F7MSK&lt;1:0:</b> 11 = Reserve 10 = Accepta 01 = Accepta 00 = Accepta	>: Mask Source ed ance Mask 2 re ance Mask 1 re ance Mask 0 re	for Filter 7 bi gisters contair gisters contair gisters contair	ts n mask n mask n mask			
bit 13-12	F6MSK<1:0	>: Mask Source	for Filter 6 bi	ts (same values	as bits<15:14	<b>!</b> >)	
bit 11-10	F5MSK<1:0	>: Mask Source	for Filter 5 bi	ts (same values	as bits<15:14	<b>!</b> >)	
bit 9-8	F4MSK<1:0	>: Mask Source	for Filter 4 bi	ts (same values	as bits<15:14	<b>!</b> >)	
bit 7-6	F3MSK<1:0:	>: Mask Source	for Filter 3 bi	ts (same values	s as bits<15:14	l>)	
bit 5-4	F2MSK<1:0	>: Mask Source	for Filter 2 bi	ts (same values	s as bits<15:14	<b>!</b> >)	
bit 3-2	F1MSK<1:0	>: Mask Source	for Filter 1 bi	ts (same values	s as bits<15:14	ł>)	
bit 1-0	F0MSK<1:0	Hask Source	for Filter 0 bi	ts (same values	s as bits<15:14	<b>!</b> >)	

R/W-0	R/W-0	U-0	U-0	U-0	R/W-0	R/W-0	R/W-0					
CSS31	CSS30		—	_	CSS26 <sup>(2)</sup>	CSS25 <sup>(2)</sup>	CSS24 <sup>(2)</sup>					
bit 15				•			bit 8					
U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0					
_				—								
bit 7							bit 0					
Legend:												
R = Readabl	e bit	W = Writable b	pit	U = Unimple	mented bit, read	d as '0'						
-n = Value at	POR	'1' = Bit is set		'0' = Bit is cle	eared	x = Bit is unknown						
bit 15	CSS31: ADC	1 Input Scan Se	election bit									
	1 = Selects C	1 = Selects CTMU capacitive and time measurement for input scan (Open)										
	0 = Skips CTI	MU capacitive a	ind time meas	surement for in	put scan (Open	)						
bit 14	CSS30: ADC	1 Input Scan Se	election bit									
	1 = Selects C 0 = Skips CTI	TMU on-chip te MU on-chip tem	mperature mea	easurement fo surement for i	r input scan (CT nput scan (CTM	MU TEMP) IU TEMP)						
bit 13-11	Unimplemen	ted: Read as '0	)'									
bit 10	CSS26: ADC	1 Input Scan Se	election bit <sup>(2)</sup>									
	1 = Selects O	A3/AN6 for inpu	ut scan									
	0 = Skips OA	3/AN6 for input	scan									
bit 9	CSS25: ADC	1 Input Scan Se	election bit <sup>(2)</sup>									
	1 = Selects O	A2/AN0 for inpu	ut scan									
	0 = Skips OA	2/AN0 for input	scan									
bit 8	CSS24: ADC	1 Input Scan Se	election bit <sup>(2)</sup>									
	1 = Selects O 0 = Skips OA	A1/AN3 for input 1/AN3 for input	ut scan scan									
bit 7-0	Unimplemen	ted: Read as 'o	)'									
Note 1: A	II AD1CSSH bits prresponding inpu	can be selected ut on the device	d by user softw , convert VRE	vare. However <sub>FL.</sub>	r, inputs selecte	d for scan, with	out a					

# REGISTER 23-7: AD1CSSH: ADC1 INPUT SCAN SELECT REGISTER HIGH<sup>(1)</sup>

2: The OAx input is used if the corresponding op amp is selected (OPMODE (CMxCON<10>) = 1); otherwise, the ANx input is used.

# 27.0 SPECIAL FEATURES

Note: This data sheet summarizes the features of the dsPIC33EPXXXGP50X. dsPIC33EPXXXMC20X/50X and PIC24EPXXXGP/MC20X families of devices. It is not intended to be a То comprehensive reference source. complement the information in this data sheet, refer to the related section of the "dsPIC33/PIC24 Familv Reference Manual', which is available from the Microchip web site (www.microchip.com).

dsPIC33EPXXXGP50X, dsPIC33EPXXXMC20X/50X and PIC24EPXXXGP/MC20X devices include several features intended to maximize application flexibility and reliability, and minimize cost through elimination of external components. These are:

- Flexible Configuration
- Watchdog Timer (WDT)
- Code Protection and CodeGuard<sup>™</sup> Security
- JTAG Boundary Scan Interface
- In-Circuit Serial Programming<sup>™</sup> (ICSP<sup>™</sup>)
- In-Circuit Emulation

# 27.1 Configuration Bits

In dsPIC33EPXXXGP50X, dsPIC33EPXXXMC20X/ 50X and PIC24EPXXXGP/MC20X devices, the Configuration bytes are implemented as volatile memory. This means that configuration data must be programmed each time the device is powered up. Configuration data is stored in at the top of the on-chip program memory space, known as the Flash Configuration bytes. Their specific locations are shown in Table 27-1. The configuration data is automatically loaded from the Flash Configuration bytes to the proper Configuration Shadow registers during device Resets.

Note:	Configuration data is reloaded on all types
	of device Resets.

When creating applications for these devices, users should always specifically allocate the location of the Flash Configuration bytes for configuration data in their code for the compiler. This is to make certain that program code is not stored in this address when the code is compiled.

The upper 2 bytes of all Flash Configuration Words in program memory should always be '1111 1111 1111 1111 1111 1111'. This makes them appear to be NOP instructions in the remote event that their locations are ever executed by accident. Since Configuration bits are not implemented in the corresponding locations, writing '1's to these locations has no effect on device operation.

**Note:** Performing a page erase operation on the last page of program memory clears the Flash Configuration bytes, enabling code protection as a result. Therefore, users should avoid performing page erase operations on the last page of program memory.

The Configuration Flash bytes map is shown in Table 27-1.

Base Instr #	Assembly Mnemonic		Assembly Syntax	Description	# of Words	# of Cycles <sup>(2)</sup>	Status Flags Affected
1	ADD	ADD	Acc <sup>(1)</sup>	Add Accumulators	1	1	OA,OB,SA,SB
		ADD	f	f = f + WREG	1	1	C,DC,N,OV,Z
		ADD	f,WREG	WREG = f + WREG	1	1	C,DC,N,OV,Z
		ADD	#lit10,Wn	Wd = lit10 + Wd	1	1	C,DC,N,OV,Z
		ADD	Wb,Ws,Wd	Wd = Wb + Ws	1	1	C,DC,N,OV,Z
		ADD	Wb,#lit5,Wd	Wd = Wb + lit5	1	1	C,DC,N,OV,Z
		ADD	Wso,#Slit4,Acc	16-bit Signed Add to Accumulator	1	1	OA,OB,SA,SB
2	ADDC	ADDC	f	f = f + WREG + (C)	1	1	C,DC,N,OV,Z
		ADDC	f,WREG	WREG = f + WREG + (C)	1	1	C,DC,N,OV,Z
		ADDC	#lit10,Wn	Wd = lit10 + Wd + (C)	1	1	C,DC,N,OV,Z
		ADDC	Wb,Ws,Wd	Wd = Wb + Ws + (C)	1	1	C,DC,N,OV,Z
		ADDC	Wb,#lit5,Wd	Wd = Wb + lit5 + (C)	1	1	C,DC,N,OV,Z
3	AND	AND	f	f = f .AND. WREG	1	1	N,Z
		AND	f,WREG	WREG = f .AND. WREG	1	1	N,Z
		AND	#lit10,Wn	Wd = lit10 .AND. Wd	1	1	N,Z
		AND	Wb,Ws,Wd	Wd = Wb .AND. Ws	1	1	N,Z
		AND	Wb,#lit5,Wd	Wd = Wb .AND. lit5	1	1	N,Z
4	ASR	ASR	f	f = Arithmetic Right Shift f	1	1	C,N,OV,Z
		ASR	f,WREG	WREG = Arithmetic Right Shift f	1	1	C,N,OV,Z
		ASR	Ws,Wd	Wd = Arithmetic Right Shift Ws	1	1	C,N,OV,Z
		ASR	Wb,Wns,Wnd	Wnd = Arithmetic Right Shift Wb by Wns	1	1	N,Z
		ASR	Wb,#lit5,Wnd	Wnd = Arithmetic Right Shift Wb by lit5	1	1	N,Z
5	BCLR	BCLR	f,#bit4	Bit Clear f	1	1	None
		BCLR	Ws,#bit4	Bit Clear Ws	1	1	None
6	BRA	BRA	C,Expr	Branch if Carry	1	1 (4)	None
		BRA	GE, Expr	Branch if greater than or equal	1	1 (4)	None
		BRA	GEU, Expr	Branch if unsigned greater than or equal	1	1 (4)	None
		BRA	GT, Expr	Branch if greater than	1	1 (4)	None
		BRA	GTU, Expr	Branch if unsigned greater than	1	1 (4)	None
		BRA	LE, Expr	Branch if less than or equal	1	1 (4)	None
		BRA	LEU, Expr	Branch if unsigned less than or equal	1	1 (4)	None
		BRA	LT,Expr	Branch if less than	1	1 (4)	None
		BRA	LTU, Expr	Branch if unsigned less than	1	1 (4)	None
		BRA	N,Expr	Branch if Negative	1	1 (4)	None
		BRA	NC, Expr	Branch if Not Carry	1	1 (4)	None
		BRA	NN, Expr	Branch if Not Negative	1	1 (4)	None
		BRA	NOV, Expr	Branch if Not Overflow	1	1 (4)	None
		BRA	NZ,Expr	Branch if Not Zero	1	1 (4)	None
		BRA	OA, Expr(1)	Branch if Accumulator A overflow	1	1 (4)	None
		BRA	OB, Expr(1)	Branch if Accumulator B overflow	1	1 (4)	None
		BRA	OV, Expr(1)	Branch if Overflow	1	1 (4)	None
		BRA	SA, Expr(1)	Branch if Accumulator A saturated	1	1 (4)	None
		BRA	SB, Expr <sup>(1)</sup>	Branch if Accumulator B saturated	1	1 (4)	None
		BRA	Expr	Branch Unconditionally	1	4	None
		BRA	Z,Expr	Branch if Zero	1	1 (4)	None
L		BRA	Wn	Computed Branch	1	4	None
7	BSET	BSET	f,#bit4	Bit Set f	1	1	None
		BSET	Ws,#bit4	Bit Set Ws	1	1	None
8	BSW	BSW.C	Ws,Wb	Write C bit to Ws <wb></wb>	1	1	None
		BSW.Z	Ws,Wb	Write Z bit to Ws <wb></wb>	1	1	None

#### TABLE 28-2: INSTRUCTION SET OVERVIEW

Note 1: These instructions are available in dsPIC33EPXXXMC20X/50X and PIC24EPXXXMC20X devices only.

2: Read and Read-Modify-Write (e.g., bit operations and logical operations) on non-CPU SFRs incur an additional instruction cycle.

DC CHARACTERISTICS			$\begin{array}{llllllllllllllllllllllllllllllllllll$								
Parameter No.	Тур.	Max.	Units	Conditions							
Operating Current (IDD) <sup>(1)</sup>											
DC20d	9	15	mA	-40°C		10 MIPS					
DC20a	9	15	mA	+25°C	3 3\/						
DC20b	9	15	mA	+85°C	3.5 V						
DC20c	9	15	mA	+125°C							
DC22d	16	25	mA	-40°C		20 MIPS					
DC22a	16	25	mA	+25°C	2.21/						
DC22b	16	25	mA	+85°C	3.3V						
DC22c	16	25	mA	+125°C							
DC24d	27	40	mA	-40°C		40 MIPS					
DC24a	27	40	mA	+25°C	2 2)/						
DC24b	27	40	mA	+85°C	3.3V						
DC24c	27	40	mA	+125°C							
DC25d	36	55	mA	-40°C		60 MIPS					
DC25a	36	55	mA	+25°C	2.21/						
DC25b	36	55	mA	+85°C	3.3V						
DC25c	36	55	mA	+125°C							
DC26d	41	60	mA	-40°C							
DC26a	41	60	mA	+25°C	3.3V	70 MIPS					
DC26b	41	60	mA	+85°C	7						

#### TABLE 30-6: DC CHARACTERISTICS: OPERATING CURRENT (IDD)

**Note 1:** IDD is primarily a function of the operating voltage and frequency. Other factors, such as I/O pin loading and switching rate, oscillator type, internal code execution pattern and temperature, also have an impact on the current consumption. The test conditions for all IDD measurements are as follows:

• Oscillator is configured in EC mode with PLL, OSC1 is driven with external square wave from rail-to-rail (EC clock overshoot/undershoot < 250 mV required)

- · CLKO is configured as an I/O input pin in the Configuration Word
- · All I/O pins are configured as inputs and pulled to Vss
- MCLR = VDD, WDT and FSCM are disabled
- CPU, SRAM, program memory and data memory are operational
- No peripheral modules are operating; however, every peripheral is being clocked (all PMDx bits are zeroed)
- CPU is executing while(1) {NOP(); } statement
- · JTAG is disabled



#### FIGURE 30-18: SPI2 SLAVE MODE (FULL-DUPLEX, CKE = 1, CKP = 0, SMP = 0) TIMING CHARACTERISTICS