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Details

Product Status	Active
Core Processor	PIC
Core Size	16-Bit
Speed	60 MIPS
Connectivity	I ² C, IrDA, LINbus, QEI, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, DMA, Motor Control PWM, POR, PWM, WDT
Number of I/O	35
Program Memory Size	32KB (10.7K x 24)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	2K x 16
Voltage - Supply (Vcc/Vdd)	3V ~ 3.6V
Data Converters	A/D 9x10b/12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 125°C (TA)
Mounting Type	Surface Mount
Package / Case	44-TQFP
Supplier Device Package	44-TQFP (10x10)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/pic24ep32mc204-e-pt

2.0 GUIDELINES FOR GETTING STARTED WITH 16-BIT DIGITAL SIGNAL CONTROLLERS AND MICROCONTROLLERS

Note 1: This data sheet summarizes the features of the dsPIC33EPXXXGP50X, dsPIC33EPXXXMC20X/50X and PIC24EPXXXGP/MC20X families of devices. It is not intended to be a comprehensive reference source. To complement the information in this data sheet, refer to the related section of the “dsPIC33/PIC24 Family Reference Manual”, which is available from the Microchip web site (www.microchip.com)

2: Some registers and associated bits described in this section may not be available on all devices. Refer to **Section 4.0 “Memory Organization”** in this data sheet for device-specific register and bit information.

2.1 Basic Connection Requirements

Getting started with the dsPIC33EPXXXGP50X, dsPIC33EPXXXMC20X/50X and PIC24EPXXXGP/MC20X families requires attention to a minimal set of device pin connections before proceeding with development. The following is a list of pin names, which must always be connected:

- All VDD and VSS pins
(see **Section 2.2 “Decoupling Capacitors”**)
- All AVDD and AVSS pins (regardless if ADC module is not used)
(see **Section 2.2 “Decoupling Capacitors”**)
- VCAP
(see **Section 2.3 “CPU Logic Filter Capacitor Connection (VCAP)”**)
- MCLR pin
(see **Section 2.4 “Master Clear (MCLR) Pin”**)
- PGECx/PGEDx pins used for In-Circuit Serial Programming™ (ICSP™) and debugging purposes
(see **Section 2.5 “ICSP Pins”**)
- OSC1 and OSC2 pins when external oscillator source is used
(see **Section 2.6 “External Oscillator Pins”**)

Additionally, the following pins may be required:

- VREF+/VREF- pins are used when external voltage reference for the ADC module is implemented

Note: The AVDD and AVSS pins must be connected, independent of the ADC voltage reference source.

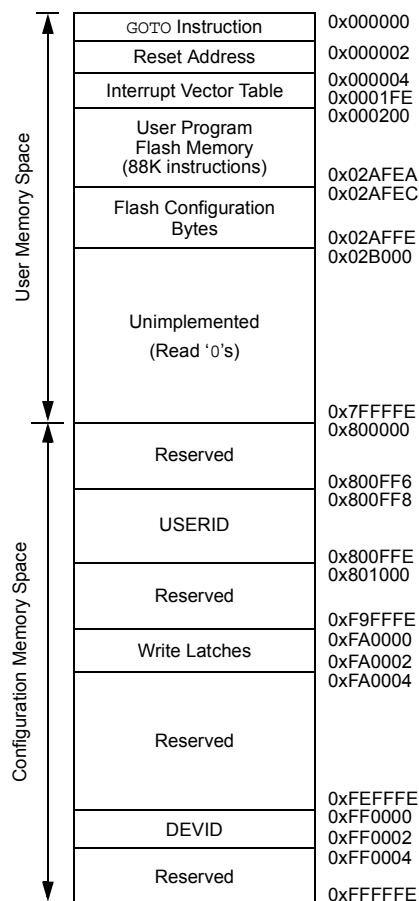
2.2 Decoupling Capacitors

The use of decoupling capacitors on every pair of power supply pins, such as VDD, VSS, AVDD and AVSS is required.

Consider the following criteria when using decoupling capacitors:

- **Value and type of capacitor:** Recommendation of 0.1 μF (100 nF), 10-20V. This capacitor should be a low-ESR and have resonance frequency in the range of 20 MHz and higher. It is recommended to use ceramic capacitors.
- **Placement on the printed circuit board:** The decoupling capacitors should be placed as close to the pins as possible. It is recommended to place the capacitors on the same side of the board as the device. If space is constricted, the capacitor can be placed on another layer on the PCB using a via; however, ensure that the trace length from the pin to the capacitor is within one-quarter inch (6 mm) in length.
- **Handling high-frequency noise:** If the board is experiencing high-frequency noise, above tens of MHz, add a second ceramic-type capacitor in parallel to the above described decoupling capacitor. The value of the second capacitor can be in the range of 0.01 μF to 0.001 μF . Place this second capacitor next to the primary decoupling capacitor. In high-speed circuit designs, consider implementing a decade pair of capacitances as close to the power and ground pins as possible. For example, 0.1 μF in parallel with 0.001 μF .
- **Maximizing performance:** On the board layout from the power supply circuit, run the power and return traces to the decoupling capacitors first, and then to the device pins. This ensures that the decoupling capacitors are first in the power chain. Equally important is to keep the trace length between the capacitor and the power pins to a minimum, thereby reducing PCB track inductance.

FIGURE 4-4: PROGRAM MEMORY MAP FOR dsPIC33EP256GP50X, dsPIC33EP256MC20X/50X AND PIC24EP256GP/MC20X DEVICES



Note: Memory areas are not shown to scale.

TABLE 4-29: PERIPHERAL PIN SELECT INPUT REGISTER MAP FOR PIC24EPXXXMC20X DEVICES ONLY

File Name	Addr.	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	All Resets		
RPINR0	06A0	—	INT1R<6:0>								—	—	—	—	—	—	—	—	0000	
RPINR1	06A2	—	—	—	—	—	—	—	—	—	INT2R<6:0>								0000	
RPINR3	06A6	—	—	—	—	—	—	—	—	—	T2CKR<6:0>								0000	
RPINR7	06AE	—	IC2R<6:0>								—	IC1R<6:0>								0000
RPINR8	06B0	—	IC4R<6:0>								—	IC3R<6:0>								0000
RPINR11	06B6	—	—	—	—	—	—	—	—	—	OCFAR<6:0>								0000	
RPINR12	06B8	—	FLT2R<6:0>								—	FLT1R<6:0>								0000
RPINR14	06BC	—	QEB1R<6:0>								—	QEA1R<6:0>								0000
RPINR15	06BE	—	HOME1R<6:0>								—	INDX1R<6:0>								0000
RPINR18	06C4	—	—	—	—	—	—	—	—	—	U1RXR<6:0>								0000	
RPINR19	06C6	—	—	—	—	—	—	—	—	—	U2RXR<6:0>								0000	
RPINR22	06CC	—	SCK2INR<6:0>								—	SDI2R<6:0>								0000
RPINR23	06CE	—	—	—	—	—	—	—	—	—	SS2R<6:0>								0000	
RPINR26	06D4	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000		
RPINR37	06EA	—	SYNC1R<6:0>								—	—	—	—	—	—	—	—	0000	
RPINR38	06EC	—	DTCMP1R<6:0>								—	—	—	—	—	—	—	—	0000	
RPINR39	06EE	—	DTCMP3R<6:0>								—	DTCMP2R<6:0>								0000

Legend: — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

TABLE 4-30: PERIPHERAL PIN SELECT INPUT REGISTER MAP FOR PIC24EPXXXGP20X DEVICES ONLY

File Name	Addr.	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	All Resets		
RPINR0	06A0	—	INT1R<6:0>								—	—	—	—	—	—	—	—	0000	
RPINR1	06A2	—	—	—	—	—	—	—	—	—	INT2R<6:0>								0000	
RPINR3	06A6	—	—	—	—	—	—	—	—	—	T2CKR<6:0>								0000	
RPINR7	06AE	—	IC2R<6:0>								—	IC1R<6:0>								0000
RPINR8	06B0	—	IC4R<6:0>								—	IC3R<6:0>								0000
RPINR11	06B6	—	—	—	—	—	—	—	—	—	OCFAR<6:0>								0000	
RPINR18	06C4	—	—	—	—	—	—	—	—	—	U1RXR<6:0>								0000	
RPINR19	06C6	—	—	—	—	—	—	—	—	—	U2RXR<6:0>								0000	
RPINR22	06CC	—	SCK2INR<6:0>								—	SDI2R<6:0>								0000
RPINR23	06CE	—	—	—	—	—	—	—	—	—	SS2R<6:0>								0000	

Legend: — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

TABLE 4-37: PMD REGISTER MAP FOR PIC24EPXXXGP20X DEVICES ONLY

File Name	Addr.	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	All Resets
PMD1	0760	T5MD	T4MD	T3MD	T2MD	T1MD	—	—	—	I2C1MD	U2MD	U1MD	SPI2MD	SPI1MD	—	—	AD1MD	0000
PMD2	0762	—	—	—	—	IC4MD	IC3MD	IC2MD	IC1MD	—	—	—	—	OC4MD	OC3MD	OC2MD	OC1MD	0000
PMD3	0764	—	—	—	—	—	CMPMD	—	—	CRCMD	—	—	—	—	—	I2C2MD	—	0000
PMD4	0766	—	—	—	—	—	—	—	—	—	—	—	—	REFOMD	CTMUMD	—	—	0000
PMD6	076A	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
PMD7	076C	—	—	—	—	—	—	—	—	—	—	—	DMA0MD	PTGMD	—	—	—	0000
													DMA1MD					
													DMA2MD					
													DMA3MD					

Legend: — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

TABLE 4-38: PMD REGISTER MAP FOR PIC24EPXXXMC20X DEVICES ONLY

File Name	Addr.	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	All Resets
PMD1	0760	T5MD	T4MD	T3MD	T2MD	T1MD	QE11MD	PWMMD	—	I2C1MD	U2MD	U1MD	SPI2MD	SPI1MD	—	—	AD1MD	0000
PMD2	0762	—	—	—	—	IC4MD	IC3MD	IC2MD	IC1MD	—	—	—	—	OC4MD	OC3MD	OC2MD	OC1MD	0000
PMD3	0764	—	—	—	—	—	CMPMD	—	—	CRCMD	—	—	—	—	—	I2C2MD	—	0000
PMD4	0766	—	—	—	—	—	—	—	—	—	—	—	—	REFOMD	CTMUMD	—	—	0000
PMD6	076A	—	—	—	—	—	PWM3MD	PWM2MD	PWM1MD	—	—	—	—	—	—	—	—	0000
PMD7	076C	—	—	—	—	—	—	—	—	—	—	—	DMA0MD	PTGMD	—	—	—	0000
													DMA1MD					
													DMA2MD					
													DMA3MD					

Legend: — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

6.0 RESETS

Note 1: This data sheet summarizes the features of the dsPIC33EPXXXGP50X, dsPIC33EPXXXMC20X/50X and PIC24EPXXXGP/MC20X families of devices. It is not intended to be a comprehensive reference source. To complement the information in this data sheet, refer to “Reset” (DS70602) in the “dsPIC33/PIC24 Family Reference Manual”, which is available from the Microchip web site (www.microchip.com).

2: Some registers and associated bits described in this section may not be available on all devices. Refer to **Section 4.0 “Memory Organization”** in this data sheet for device-specific register and bit information.

The Reset module combines all Reset sources and controls the device Master Reset Signal, $\overline{\text{SYSRST}}$. The following is a list of device Reset sources:

- POR: Power-on Reset
- BOR: Brown-out Reset
- $\overline{\text{MCLR}}$: Master Clear Pin Reset
- SWR: RESET Instruction
- WDTO: Watchdog Timer Time-out Reset
- CM: Configuration Mismatch Reset
- TRAPR: Trap Conflict Reset
- IOPUWR: Illegal Condition Device Reset
 - Illegal Opcode Reset
 - Uninitialized W Register Reset
 - Security Reset

A simplified block diagram of the Reset module is shown in Figure 6-1.

Any active source of Reset will make the $\overline{\text{SYSRST}}$ signal active. On system Reset, some of the registers associated with the CPU and peripherals are forced to a known Reset state and some are unaffected.

Note: Refer to the specific peripheral section or **Section 4.0 “Memory Organization”** of this manual for register Reset states.

All types of device Reset set a corresponding status bit in the RCON register to indicate the type of Reset (see Register 6-1).

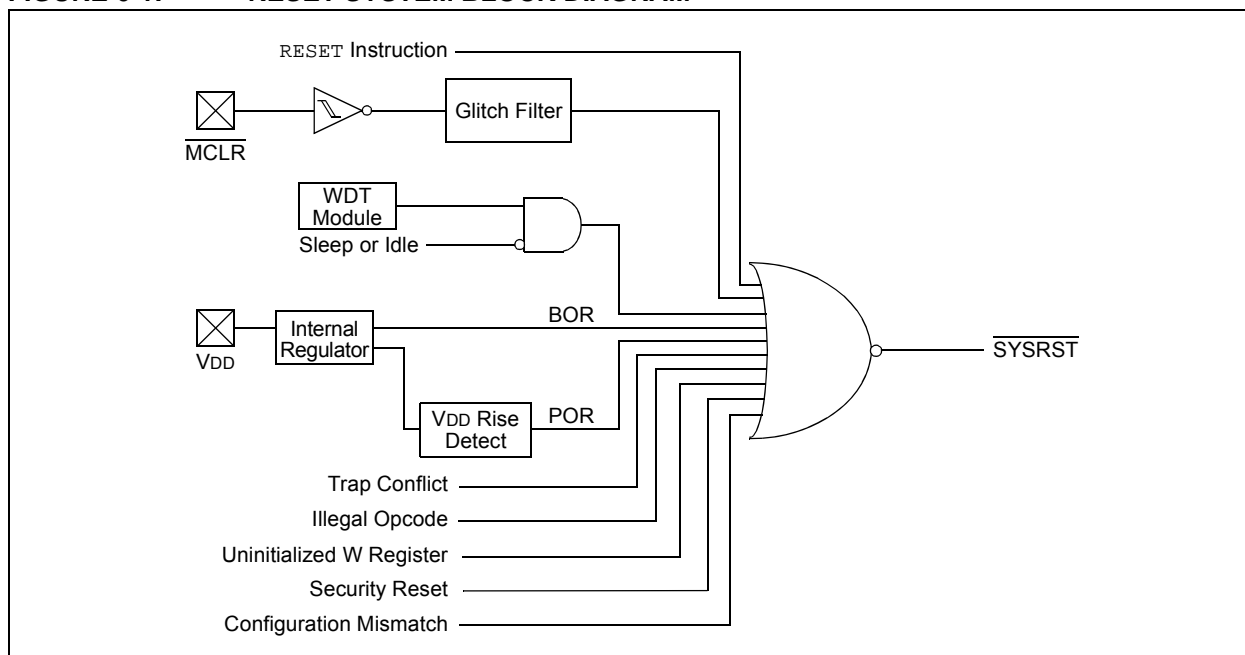
A POR clears all the bits, except for the POR and BOR bits (RCON<1:0>), that are set. The user application can set or clear any bit at any time during code execution. The RCON bits only serve as status bits. Setting a particular Reset status bit in software does not cause a device Reset to occur.

The RCON register also has other bits associated with the Watchdog Timer and device power-saving states. The function of these bits is discussed in other sections of this manual.

Note: The status bits in the RCON register should be cleared after they are read so that the next RCON register value after a device Reset is meaningful.

For all Resets, the default clock source is determined by the FNOSC<2:0> bits in the FOSCSEL Configuration register. The value of the FNOSC<2:0> bits is loaded into NOSC<2:0> (OSCCON<10:8>) on Reset, which in turn, initializes the system clock.

FIGURE 6-1: RESET SYSTEM BLOCK DIAGRAM



REGISTER 11-18: RPOR0: PERIPHERAL PIN SELECT OUTPUT REGISTER 0

U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
—	—	RP35R<5:0>					
bit 15							bit 8

U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
—	—	RP20R<5:0>					
bit 7							bit 0

Legend:

R = Readable bit W = Writable bit U = Unimplemented bit, read as '0'
-n = Value at POR '1' = Bit is set '0' = Bit is cleared x = Bit is unknown

bit 15-14 **Unimplemented:** Read as '0'
bit 13-8 **RP35R<5:0>:** Peripheral Output Function is Assigned to RP35 Output Pin bits
(see Table 11-3 for peripheral function numbers)
bit 7-6 **Unimplemented:** Read as '0'
bit 5-0 **RP20R<5:0>:** Peripheral Output Function is Assigned to RP20 Output Pin bits
(see Table 11-3 for peripheral function numbers)

REGISTER 11-19: RPOR1: PERIPHERAL PIN SELECT OUTPUT REGISTER 1

U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
—	—	RP37R<5:0>					
bit 15							bit 8

U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
—	—	RP36R<5:0>					
bit 7							bit 0

Legend:

R = Readable bit W = Writable bit U = Unimplemented bit, read as '0'
-n = Value at POR '1' = Bit is set '0' = Bit is cleared x = Bit is unknown

bit 15-14 **Unimplemented:** Read as '0'
bit 13-8 **RP37R<5:0>:** Peripheral Output Function is Assigned to RP37 Output Pin bits
(see Table 11-3 for peripheral function numbers)
bit 7-6 **Unimplemented:** Read as '0'
bit 5-0 **RP36R<5:0>:** Peripheral Output Function is Assigned to RP36 Output Pin bits
(see Table 11-3 for peripheral function numbers)

REGISTER 11-20: RPOR2: PERIPHERAL PIN SELECT OUTPUT REGISTER 2

U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
—	—	RP39R<5:0>					
bit 15							bit 8

U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
—	—	RP38R<5:0>					
bit 7							bit 0

Legend:

R = Readable bit W = Writable bit U = Unimplemented bit, read as '0'
-n = Value at POR '1' = Bit is set '0' = Bit is cleared x = Bit is unknown

- bit 15-14 **Unimplemented:** Read as '0'
- bit 13-8 **RP39R<5:0>:** Peripheral Output Function is Assigned to RP39 Output Pin bits
(see Table 11-3 for peripheral function numbers)
- bit 7-6 **Unimplemented:** Read as '0'
- bit 5-0 **RP38R<5:0>:** Peripheral Output Function is Assigned to RP38 Output Pin bits
(see Table 11-3 for peripheral function numbers)

REGISTER 11-21: RPOR3: PERIPHERAL PIN SELECT OUTPUT REGISTER 3

U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
—	—	RP41R<5:0>					
bit 15							bit 8

U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
—	—	RP40R<5:0>					
bit 7							bit 0

Legend:

R = Readable bit W = Writable bit U = Unimplemented bit, read as '0'
-n = Value at POR '1' = Bit is set '0' = Bit is cleared x = Bit is unknown

- bit 15-14 **Unimplemented:** Read as '0'
- bit 13-8 **RP41R<5:0>:** Peripheral Output Function is Assigned to RP41 Output Pin bits
(see Table 11-3 for peripheral function numbers)
- bit 7-6 **Unimplemented:** Read as '0'
- bit 5-0 **RP40R<5:0>:** Peripheral Output Function is Assigned to RP40 Output Pin bits
(see Table 11-3 for peripheral function numbers)

13.0 TIMER2/3 AND TIMER4/5

Note 1: This data sheet summarizes the features of the dsPIC33EPXXXGP50X, dsPIC33EPXXXMC20X/50X and PIC24EPXXXGP/MC20X family of devices. It is not intended to be a comprehensive reference source. To complement the information in this data sheet, refer to “**Timers**” (DS70362) of the “*dsPIC33/PIC24 Family Reference Manual*”, which is available from the Microchip web site (www.microchip.com).

- 2: Some registers and associated bits described in this section may not be available on all devices. Refer to **Section 4.0 “Memory Organization”** in this data sheet for device-specific register and bit information.

The Timer2/3 and Timer4/5 modules are 32-bit timers, which can also be configured as four independent 16-bit timers with selectable operating modes.

As 32-bit timers, Timer2/3 and Timer4/5 operate in three modes:

- Two Independent 16-Bit Timers (e.g., Timer2 and Timer3) with all 16-Bit Operating modes (except Asynchronous Counter mode)
- Single 32-Bit Timer
- Single 32-Bit Synchronous Counter

They also support these features:

- Timer Gate Operation
- Selectable Prescaler Settings
- Timer Operation during Idle and Sleep modes
- Interrupt on a 32-Bit Period Register Match
- Time Base for Input Capture and Output Compare Modules (Timer2 and Timer3 only)
- ADC1 Event Trigger (32-bit timer pairs, and Timer3 and Timer5 only)

Individually, all four of the 16-bit timers can function as synchronous timers or counters. They also offer the features listed previously, except for the event trigger; this is implemented only with Timer2/3. The operating modes and enabled features are determined by setting the appropriate bit(s) in the T2CON, T3CON, and T4CON, T5CON registers. T2CON and T4CON are shown in generic form in Register 13-1. T3CON and T5CON are shown in Register 13-2.

For 32-bit timer/counter operation, Timer2 and Timer4 are the least significant word (lsb); Timer3 and Timer5 are the most significant word (msb) of the 32-bit timers.

Note: For 32-bit operation, T3CON and T5CON control bits are ignored. Only T2CON and T4CON control bits are used for setup and control. Timer2 and Timer4 clock and gate inputs are utilized for the 32-bit timer modules, but an interrupt is generated with the Timer3 and Timer5 interrupt flags.

A block diagram for an example 32-bit timer pair (Timer2/3 and Timer4/5) is shown in Figure 13-3.

Note: Only Timer2, 3, 4 and 5 can trigger a DMA data transfer.

14.0 INPUT CAPTURE

Note 1: This data sheet summarizes the features of the dsPIC33EPXXXGP50X, dsPIC33EPXXXMC20X/50X and PIC24EPXXXGP/MC20X families of devices. It is not intended to be a comprehensive reference source. To complement the information in this data sheet, refer to “**Input Capture**” (DS70352) in the “*dsPIC33/dsPIC24 Family Reference Manual*”, which is available from the Microchip web site (www.microchip.com).

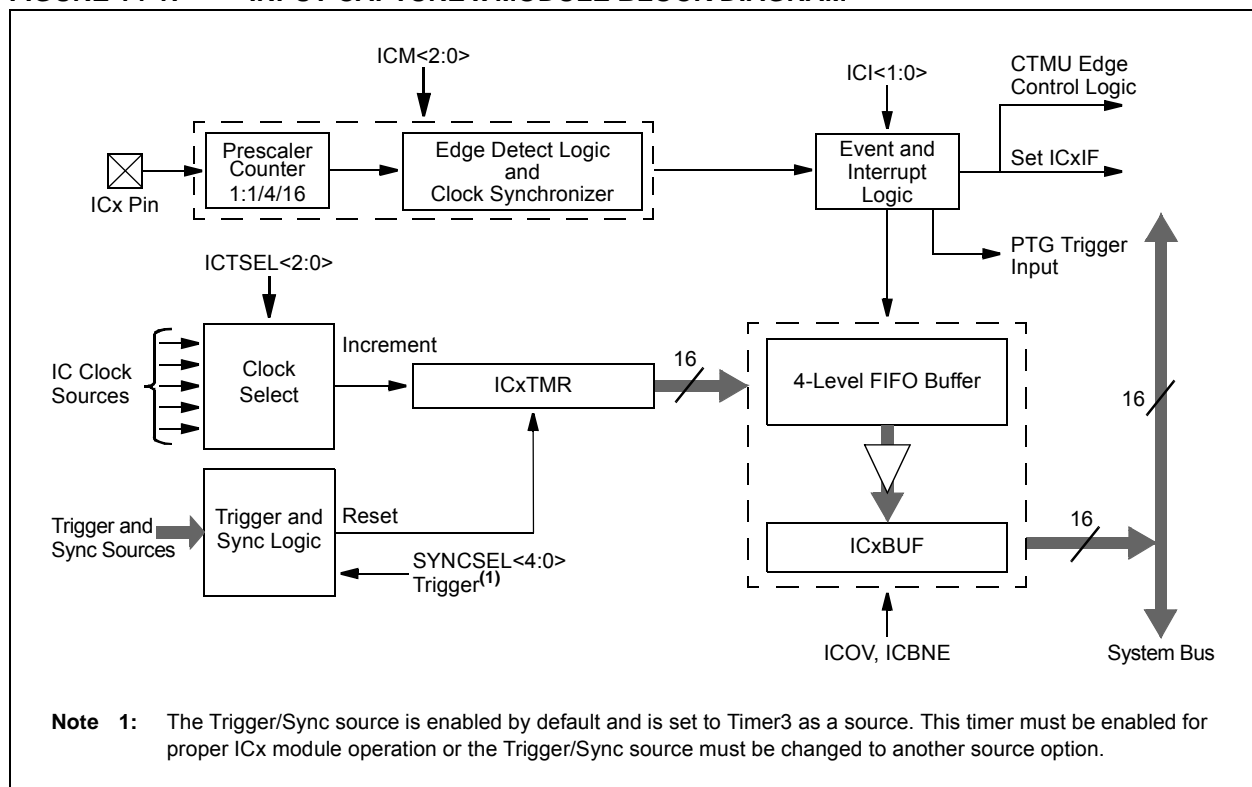
2: Some registers and associated bits described in this section may not be available on all devices. Refer to **Section 4.0 “Memory Organization”** in this data sheet for device-specific register and bit information.

The input capture module is useful in applications requiring frequency (period) and pulse measurement. The dsPIC33EPXXXGP50X, dsPIC33EPXXXMC20X/50X and PIC24EPXXXGP/MC20X devices support four input capture channels.

Key features of the input capture module include:

- Hardware-configurable for 32-bit operation in all modes by cascading two adjacent modules
- Synchronous and Trigger modes of output compare operation, with up to 19 user-selectable Trigger/Sync sources available
- A 4-level FIFO buffer for capturing and holding timer values for several events
- Configurable interrupt generation
- Up to six clock sources available for each module, driving a separate internal 16-bit counter

FIGURE 14-1: INPUT CAPTURE x MODULE BLOCK DIAGRAM



16.3 PWMx Control Registers

REGISTER 16-1: PTCON: PWMx TIME BASE CONTROL REGISTER

R/W-0	U-0	R/W-0	HS/HC-0	R/W-0	R/W-0	R/W-0	R/W-0
PTEN	—	PTSIDL	SESTAT	SEIEN	EIPU ⁽¹⁾	SYNCPOL ⁽¹⁾	SYNCOEN ⁽¹⁾
bit 15							bit 8

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
SYNCEN ⁽¹⁾	SYNCSRC2 ⁽¹⁾	SYNCSRC1 ⁽¹⁾	SYNCSRC0 ⁽¹⁾	SEVTPS3 ⁽¹⁾	SEVTPS2 ⁽¹⁾	SEVTPS1 ⁽¹⁾	SEVTPS0 ⁽¹⁾
bit 7							bit 0

Legend:	HC = Hardware Clearable bit	HS = Hardware Settable bit
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared x = Bit is unknown

- bit 15 **PTEN:** PWMx Module Enable bit
1 = PWMx module is enabled
0 = PWMx module is disabled
- bit 14 **Unimplemented:** Read as '0'
- bit 13 **PTSIDL:** PWMx Time Base Stop in Idle Mode bit
1 = PWMx time base halts in CPU Idle mode
0 = PWMx time base runs in CPU Idle mode
- bit 12 **SESTAT:** Special Event Interrupt Status bit
1 = Special event interrupt is pending
0 = Special event interrupt is not pending
- bit 11 **SEIEN:** Special Event Interrupt Enable bit
1 = Special event interrupt is enabled
0 = Special event interrupt is disabled
- bit 10 **EIPU:** Enable Immediate Period Updates bit⁽¹⁾
1 = Active Period register is updated immediately
0 = Active Period register updates occur on PWMx cycle boundaries
- bit 9 **SYNCPOL:** Synchronize Input and Output Polarity bit⁽¹⁾
1 = SYNCI1/SYNCO1 polarity is inverted (active-low)
0 = SYNCI1/SYNCO1 is active-high
- bit 8 **SYNCOEN:** Primary Time Base Sync Enable bit⁽¹⁾
1 = SYNCO1 output is enabled
0 = SYNCO1 output is disabled
- bit 7 **SYNCEN:** External Time Base Synchronization Enable bit⁽¹⁾
1 = External synchronization of primary time base is enabled
0 = External synchronization of primary time base is disabled

Note 1: These bits should be changed only when PTEN = 0. In addition, when using the SYNCI1 feature, the user application must program the period register with a value that is slightly larger than the expected period of the external synchronization input signal.

2: See **Section 24.0 “Peripheral Trigger Generator (PTG) Module”** for information on this selection.

19.1 I²C Resources

Many useful resources are provided on the main product page of the Microchip web site for the devices listed in this data sheet. This product page, which can be accessed using this link, contains the latest updates and additional information.

<p>Note: In the event you are not able to access the product page using the link above, enter this URL in your browser: http://www.microchip.com/wwwproducts/Devices.aspx?dDocName=en555464</p>
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19.1.1 KEY RESOURCES

- **“Inter-Integrated Circuit (I²C)”** (DS70330) in the *“dsPIC33/PIC24 Family Reference Manual”*
- Code Samples
- Application Notes
- Software Libraries
- Webinars
- All Related *“dsPIC33/PIC24 Family Reference Manual”* Sections
- Development Tools

REGISTER 19-3: I2CxMSK: I2Cx SLAVE MODE ADDRESS MASK REGISTER

U-0	U-0	U-0	U-0	U-0	U-0	R/W-0	R/W-0
—	—	—	—	—	—	AMSK9	AMSK8
bit 15						bit 8	

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
AMSK7	AMSK6	AMSK5	AMSK4	AMSK3	AMSK2	AMSK1	AMSK0
bit 7							bit 0

Legend:

R = Readable bit

W = Writable bit

U = Unimplemented bit, read as '0'

-n = Value at POR

'1' = Bit is set

'0' = Bit is cleared

x = Bit is unknown

bit 15-10

Unimplemented: Read as '0'

bit 9-0

AMSK<9:0>: Address Mask Select bits

For 10-Bit Address:

1 = Enables masking for bit Ax of incoming message address; bit match is not required in this position

0 = Disables masking for bit Ax; bit match is required in this position

For 7-Bit Address (I2CxMSK<6:0> only):

1 = Enables masking for bit Ax + 1 of incoming message address; bit match is not required in this position

0 = Disables masking for bit Ax + 1; bit match is required in this position

22.0 CHARGE TIME MEASUREMENT UNIT (CTMU)

Note 1: This data sheet summarizes the features of the dsPIC33EPXXXGP50X, dsPIC33EPXXXMC20X/50X and PIC24EPXXXGP/MC20X family of devices. It is not intended to be a comprehensive reference source. To complement the information in this data sheet, refer to “**Charge Time Measurement Unit (CTMU)**” (DS70661) in the “*dsPIC33/PIC24 Family Reference Manual*”, which is available on the Microchip web site (www.microchip.com).

2: Some registers and associated bits described in this section may not be available on all devices. Refer to **Section 4.0 “Memory Organization”** in this data sheet for device-specific register and bit information.

The Charge Time Measurement Unit is a flexible analog module that provides accurate differential time measurement between pulse sources, as well as asynchronous pulse generation. Its key features include:

- Four Edge Input Trigger Sources
- Polarity Control for Each Edge Source
- Control of Edge Sequence
- Control of Response to Edges
- Precise Time Measurement Resolution of 1 ns
- Accurate Current Source Suitable for Capacitive Measurement
- On-Chip Temperature Measurement using a Built-in Diode

Together with other on-chip analog modules, the CTMU can be used to precisely measure time, measure capacitance, measure relative changes in capacitance or generate output pulses that are independent of the system clock.

The CTMU module is ideal for interfacing with capacitive-based sensors. The CTMU is controlled through three registers: CTMUCON1, CTMUCON2 and CTMUICON. CTMUCON1 and CTMUCON2 enable the module and control edge source selection, edge source polarity selection and edge sequencing. The CTMUICON register controls the selection and trim of the current source.

22.2 CTMU Control Registers

REGISTER 22-1: CTMUCON1: CTMU CONTROL REGISTER 1

R/W-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
CTMUEN	—	CTMUSIDL	TGEN	EDGEN	EDGSEQEN	IDISSEN ⁽¹⁾	CTTRIG
bit 15							bit 8

U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
—	—	—	—	—	—	—	—
bit 7							bit 0

Legend:

R = Readable bit

W = Writable bit

U = Unimplemented bit, read as '0'

-n = Value at POR

'1' = Bit is set

'0' = Bit is cleared

x = Bit is unknown

- bit 15 **CTMUEN:** CTMU Enable bit
 1 = Module is enabled
 0 = Module is disabled
- bit 14 **Unimplemented:** Read as '0'
- bit 13 **CTMUSIDL:** CTMU Stop in Idle Mode bit
 1 = Discontinues module operation when device enters Idle mode
 0 = Continues module operation in Idle mode
- bit 12 **TGEN:** Time Generation Enable bit
 1 = Enables edge delay generation
 0 = Disables edge delay generation
- bit 11 **EDGEN:** Edge Enable bit
 1 = Hardware modules are used to trigger edges (TMRx, CTEDx, etc.)
 0 = Software is used to trigger edges (manual set of EDGxSTAT)
- bit 10 **EDGSEQEN:** Edge Sequence Enable bit
 1 = Edge 1 event must occur before Edge 2 event can occur
 0 = No edge sequence is needed
- bit 9 **IDISSEN:** Analog Current Source Control bit⁽¹⁾
 1 = Analog current source output is grounded
 0 = Analog current source output is not grounded
- bit 8 **CTTRIG:** ADC Trigger Control bit
 1 = CTMU triggers ADC start of conversion
 0 = CTMU does not trigger ADC start of conversion
- bit 7-0 **Unimplemented:** Read as '0'

Note 1: The ADC module Sample-and-Hold capacitor is not automatically discharged between sample/conversion cycles. Software using the ADC as part of a capacitance measurement must discharge the ADC capacitor before conducting the measurement. The IDISSEN bit, when set to '1', performs this function. The ADC must be sampling while the IDISSEN bit is active to connect the discharge sink to the capacitor array.

REGISTER 25-5: CMxMSKCON: COMPARATOR x MASK GATING CONTROL REGISTER

R/W-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
HLMS	—	OCEN	OCNEN	OBEN	OBNEN	OAEN	OANEN
bit 15							bit 8

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
NAGS	PAGS	ACEN	ACNEN	ABEN	ABNEN	AAEN	AANEN
bit 7							bit 0

Legend:

R = Readable bit W = Writable bit U = Unimplemented bit, read as '0'
 -n = Value at POR '1' = Bit is set '0' = Bit is cleared x = Bit is unknown

- bit 15 **HLMS:** High or Low-Level Masking Select bits
 1 = The masking (blanking) function will prevent any asserted ('0') comparator signal from propagating
 0 = The masking (blanking) function will prevent any asserted ('1') comparator signal from propagating
- bit 14 **Unimplemented:** Read as '0'
- bit 13 **OCEN:** OR Gate C Input Enable bit
 1 = MCI is connected to OR gate
 0 = MCI is not connected to OR gate
- bit 12 **OCNEN:** OR Gate C Input Inverted Enable bit
 1 = Inverted MCI is connected to OR gate
 0 = Inverted MCI is not connected to OR gate
- bit 11 **OBEN:** OR Gate B Input Enable bit
 1 = MBI is connected to OR gate
 0 = MBI is not connected to OR gate
- bit 10 **OBNEN:** OR Gate B Input Inverted Enable bit
 1 = Inverted MBI is connected to OR gate
 0 = Inverted MBI is not connected to OR gate
- bit 9 **OAEN:** OR Gate A Input Enable bit
 1 = MAI is connected to OR gate
 0 = MAI is not connected to OR gate
- bit 8 **OANEN:** OR Gate A Input Inverted Enable bit
 1 = Inverted MAI is connected to OR gate
 0 = Inverted MAI is not connected to OR gate
- bit 7 **NAGS:** AND Gate Output Inverted Enable bit
 1 = Inverted ANDI is connected to OR gate
 0 = Inverted ANDI is not connected to OR gate
- bit 6 **PAGS:** AND Gate Output Enable bit
 1 = ANDI is connected to OR gate
 0 = ANDI is not connected to OR gate
- bit 5 **ACEN:** AND Gate C Input Enable bit
 1 = MCI is connected to AND gate
 0 = MCI is not connected to AND gate
- bit 4 **ACNEN:** AND Gate C Input Inverted Enable bit
 1 = Inverted MCI is connected to AND gate
 0 = Inverted MCI is not connected to AND gate

**REGISTER 25-5: CMxMSKCON: COMPARATOR x MASK GATING
CONTROL REGISTER (CONTINUED)**

bit 3	ABEN: AND Gate B Input Enable bit 1 = MBI is connected to AND gate 0 = MBI is not connected to AND gate
bit 2	ABNEN: AND Gate B Input Inverted Enable bit 1 = Inverted MBI is connected to AND gate 0 = Inverted MBI is not connected to AND gate
bit 1	AAEN: AND Gate A Input Enable bit 1 = MAI is connected to AND gate 0 = MAI is not connected to AND gate
bit 0	AANEN: AND Gate A Input Inverted Enable bit 1 = Inverted MAI is connected to AND gate 0 = Inverted MAI is not connected to AND gate

FIGURE 30-6: INPUT CAPTURE x (ICx) TIMING CHARACTERISTICS

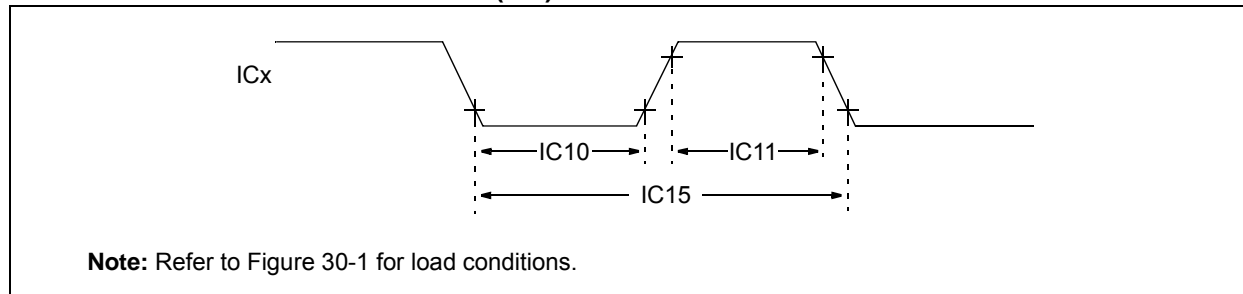


TABLE 30-26: INPUT CAPTURE x MODULE TIMING REQUIREMENTS

AC CHARACTERISTICS			Standard Operating Conditions: 3.0V to 3.6V (unless otherwise stated) Operating temperature -40°C ≤ TA ≤ +85°C for Industrial -40°C ≤ TA ≤ +125°C for Extended				
Param. No.	Symbol	Characteristics ⁽¹⁾	Min.	Max.	Units	Conditions	
IC10	TccL	ICx Input Low Time	Greater of 12.5 + 25 or (0.5 Tcy/N) + 25	—	ns	Must also meet Parameter IC15	N = prescale value (1, 4, 16)
IC11	TccH	ICx Input High Time	Greater of 12.5 + 25 or (0.5 Tcy/N) + 25	—	ns	Must also meet Parameter IC15	
IC15	TccP	ICx Input Period	Greater of 25 + 50 or (1 Tcy/N) + 50	—	ns		

Note 1: These parameters are characterized, but not tested in manufacturing.

Revision E (April 2012)

This revision includes typographical and formatting changes throughout the data sheet text.

All other major changes are referenced by their respective section in Table A-3.

TABLE A-4: MAJOR SECTION UPDATES

Section Name	Update Description
“16-bit Microcontrollers and Digital Signal Controllers (up to 512-Kbyte Flash and 48-Kbyte SRAM) with High-Speed PWM, Op amps, and Advanced Analog”	<p>The following 512-Kbyte devices were added to the General Purpose Families table (see Table 1):</p> <ul style="list-style-type: none"> • PIC24EP512GP202 • PIC24EP512GP204 • PIC24EP512GP206 • dsPIC33EP512GP502 • dsPIC33EP512GP504 • dsPIC33EP512GP506 <p>The following 512-Kbyte devices were added to the Motor Control Families table (see Table 2):</p> <ul style="list-style-type: none"> • PIC24EP512MC202 • PIC24EP512MC204 • PIC24EP512MC206 • dsPIC33EP512MC202 • dsPIC33EP512MC204 • dsPIC33EP512MC206 • dsPIC33EP512MC502 • dsPIC33EP512MC504 • dsPIC33EP512MC506 <p>Certain Pin Diagrams were updated to include the new 512-Kbyte devices.</p>
Section 4.0 “Memory Organization”	<p>Added a Program Memory Map for the new 512-Kbyte devices (see Figure 4-4).</p> <p>Added a Data Memory Map for the new dsPIC 512-Kbyte devices (see Figure 4-11).</p> <p>Added a Data Memory Map for the new PIC24 512-Kbyte devices (see Figure 4-16).</p>
Section 7.0 “Interrupt Controller”	Updated the VECNUM bits in the INTTREG register (see Register 7-7).
Section 11.0 “I/O Ports”	Added tip 6 to Section 11.5 “I/O Helpful Tips” .
Section 27.0 “Special Features”	<p>The following modifications were made to the Configuration Byte Register Map (see Table 27-1):</p> <ul style="list-style-type: none"> • Added the column Device Memory Size (Kbytes) • Removed Notes 1 through 4 • Added addresses for the new 512-Kbyte devices
Section 30.0 “Electrical Characteristics”	<p>Updated the Minimum value for Parameter DC10 (see Table 30-4).</p> <p>Added Power-Down Current (I_{pd}) parameters for the new 512-Kbyte devices (see Table 30-8).</p> <p>Updated the Minimum value for Parameter CM34 (see Table 30-53).</p> <p>Updated the Minimum and Maximum values and the Conditions for parameter SY12 (see Table 30-22).</p>

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PRODUCT IDENTIFICATION SYSTEM

To order or obtain information, e.g., on pricing or delivery, refer to the factory or the listed sales office.

		dsPIC 33 EP 64 MC5 04 T I / PT - XXX									
Microchip Trademark	_____										
Architecture	_____										
Flash Memory Family	_____										
Program Memory Size (Kbyte)	_____										
Product Group	_____										
Pin Count	_____										
Tape and Reel Flag (if applicable)	_____										
Temperature Range	_____										
Package	_____										
Pattern	_____										

Architecture:	33	=	16-bit Digital Signal Controller
	24	=	16-bit Microcontroller
Flash Memory Family:	EP	=	Enhanced Performance
Product Group:	GP	=	General Purpose family
	MC	=	Motor Control family
Pin Count:	02	=	28-pin
	03	=	36-pin
	04	=	44-pin
	06	=	64-pin
Temperature Range:	I	=	-40°C to +85°C (Industrial)
	E	=	-40°C to +125°C (Extended)
Package:	ML	=	Plastic Quad, No Lead Package - (44-pin) 8x8 mm body (QFN)
	MM	=	Plastic Quad, No Lead Package - (28-pin) 6x6 mm body (QFN-S)
	MR	=	Plastic Quad, No Lead Package - (64-pin) 9x9 mm body (QFN)
	MV	=	Thin Quad, No Lead Package - (48-pin) 6x6 mm body (UQFN)
	PT	=	Plastic Thin Quad Flatpack - (44-pin) 10x10 mm body (TQFP)
	PT	=	Plastic Thin Quad Flatpack - (64-pin) 10x10 mm body (TQFP)
	SO	=	Plastic Small Outline, Wide - (28-pin) 7.50 mm body (SOIC)
	SP	=	Skinny Plastic Dual In-Line - (28-pin) 300 mil body (SPDIP)
	SS	=	Plastic Shrink Small Outline - (28-pin) 5.30 mm body (SSOP)
	TL	=	Very Thin Leadless Array - (36-pin) 5x5 mm body (VTLA)
	TL	=	Very Thin Leadless Array - (44-pin) 6x6 mm body (VTLA)

Examples:

dsPIC33EP64MC504-I/PT:
dsPIC33, Enhanced Performance,
64-Kbyte Program Memory,
Motor Control, 44-Pin,
Industrial Temperature,
TQFP package.