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### What is "[Embedded - Microcontrollers](#)"?

"[Embedded - Microcontrollers](#)" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

### Applications of "[Embedded - Microcontrollers](#)"

#### Details

Product Status	Obsolete
Core Processor	PIC
Core Size	16-Bit
Speed	60 MIPS
Connectivity	I <sup>2</sup> C, IrDA, LINbus, QEI, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, DMA, Motor Control PWM, POR, PWM, WDT
Number of I/O	35
Program Memory Size	32KB (10.7K x 24)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	2K x 16
Voltage - Supply (Vcc/Vdd)	3V ~ 3.6V
Data Converters	A/D 9x10b/12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 150°C (TA)
Mounting Type	Surface Mount
Package / Case	44-TQFP
Supplier Device Package	44-TQFP (10x10)
Purchase URL	<a href="https://www.e-xfl.com/product-detail/microchip-technology/pic24ep32mc204-h-pt">https://www.e-xfl.com/product-detail/microchip-technology/pic24ep32mc204-h-pt</a>

**TABLE 2: dsPIC33EPXXXMC20X/50X and PIC24EPXXXMC20X MOTOR CONTROL FAMILIES (CONTINUED)**

Device	Page Erase Size (Instructions)	Program Flash Memory (Kbytes)	RAM (Kbytes)	Remappable Peripherals										CRC Generator	10-Bit/12-Bit ADC (Channels)	Op Amps/Comparators	CTMU	PTG	I/O Pins	Pins	Packages
				16-Bit/32-Bit Timers	Input Capture	Output Compare	Motor Control PWM <sup>(4)</sup> (Channels)	Quadrature Encoder Interface	UART	SPI <sup>(2)</sup>	ECAN <sup>TM</sup> Technology	External Interrupts <sup>(3)</sup>	I <sup>2</sup> C <sup>TM</sup>								
dsPIC33EP32MC504	512	32	4	5	4	4	6	1	2	2	1	3	2	1	9	3/4	Yes	Yes	35	44/ 48	VTLA <sup>(5)</sup> , TQFP, QFN, UQFN
dsPIC33EP64MC504	1024	64	8																		
dsPIC33EP128MC504	1024	128	16																		
dsPIC33EP256MC504	1024	256	32																		
dsPIC33EP512MC504	1024	512	48	5	4	4	6	1	2	2	1	3	2	1	16	3/4	Yes	Yes	53	64	TQFP, QFN
dsPIC33EP64MC506	1024	64	8																		
dsPIC33EP128MC506	1024	128	16																		
dsPIC33EP256MC506	1024	256	32																		
dsPIC33EP512MC506	1024	512	48																		

- Note 1:** On 28-pin devices, Comparator 4 does not have external connections. Refer to **Section 25.0 "Op Amp/Comparator Module"** for details.  
**2:** Only SPI2 is remappable.  
**3:** INT0 is not remappable.  
**4:** Only the PWM Faults are remappable.  
**5:** The SSOP and VTLA packages are not available for devices with 512 Kbytes of memory.

TABLE 1-1: PINOUT I/O DESCRIPTIONS (CONTINUED)

Pin Name <sup>(4)</sup>	Pin Type	Buffer Type	PPS	Description
U2CTS	I	ST	No	UART2 Clear-To-Send.
U2RTS	O	—	No	UART2 Ready-To-Send.
U2RX	I	ST	Yes	UART2 receive.
U2TX	O	—	Yes	UART2 transmit.
BCLK2	O	ST	No	UART2 IrDA <sup>®</sup> baud clock output.
SCK1	I/O	ST	No	Synchronous serial clock input/output for SPI1.
SDI1	I	ST	No	SPI1 data in.
SDO1	O	—	No	SPI1 data out.
SS1	I/O	ST	No	SPI1 slave synchronization or frame pulse I/O.
SCK2	I/O	ST	Yes	Synchronous serial clock input/output for SPI2.
SDI2	I	ST	Yes	SPI2 data in.
SDO2	O	—	Yes	SPI2 data out.
SS2	I/O	ST	Yes	SPI2 slave synchronization or frame pulse I/O.
SCL1	I/O	ST	No	Synchronous serial clock input/output for I2C1.
SDA1	I/O	ST	No	Synchronous serial data input/output for I2C1.
ASCL1	I/O	ST	No	Alternate synchronous serial clock input/output for I2C1.
ASDA1	I/O	ST	No	Alternate synchronous serial data input/output for I2C1.
SCL2	I/O	ST	No	Synchronous serial clock input/output for I2C2.
SDA2	I/O	ST	No	Synchronous serial data input/output for I2C2.
ASCL2	I/O	ST	No	Alternate synchronous serial clock input/output for I2C2.
ASDA2	I/O	ST	No	Alternate synchronous serial data input/output for I2C2.
TMS <sup>(5)</sup>	I	ST	No	JTAG Test mode select pin.
TCK	I	ST	No	JTAG test clock input pin.
TDI	I	ST	No	JTAG test data input pin.
TDO	O	—	No	JTAG test data output pin.
C1RX <sup>(2)</sup>	I	ST	Yes	ECAN1 bus receive pin.
C1TX <sup>(2)</sup>	O	—	Yes	ECAN1 bus transmit pin.
FLT1 <sup>(1)</sup> , FLT2 <sup>(1)</sup>	I	ST	Yes	PWM Fault Inputs 1 and 2.
FLT3 <sup>(1)</sup> , FLT4 <sup>(1)</sup>	I	ST	No	PWM Fault Inputs 3 and 4.
FLT32 <sup>(1,3)</sup>	I	ST	No	PWM Fault Input 32 (Class B Fault).
DTCMP1-DTCMP3 <sup>(1)</sup>	I	ST	Yes	PWM Dead-Time Compensation Inputs 1 through 3.
PWM1L-PWM3L <sup>(1)</sup>	O	—	No	PWM Low Outputs 1 through 3.
PWM1H-PWM3H <sup>(1)</sup>	O	—	No	PWM High Outputs 1 through 3.
SYNCl <sup>(1)</sup>	I	ST	Yes	PWM Synchronization Input 1.
SYNCO <sup>(1)</sup>	O	—	Yes	PWM Synchronization Output 1.
INDX1 <sup>(1)</sup>	I	ST	Yes	Quadrature Encoder Index1 pulse input.
HOME1 <sup>(1)</sup>	I	ST	Yes	Quadrature Encoder Home1 pulse input.
QEA1 <sup>(1)</sup>	I	ST	Yes	Quadrature Encoder Phase A input in QE11 mode. Auxiliary timer external clock/gate input in Timer mode.
QEB1 <sup>(1)</sup>	I	ST	Yes	Quadrature Encoder Phase B input in QE11 mode. Auxiliary timer external clock/gate input in Timer mode.
CNTCMP1 <sup>(1)</sup>	O	—	Yes	Quadrature Encoder Compare Output 1.

**Legend:** CMOS = CMOS compatible input or output      Analog = Analog input      P = Power  
ST = Schmitt Trigger input with CMOS levels      O = Output      I = Input  
PPS = Peripheral Pin Select      TTL = TTL input buffer

- Note 1:** This pin is available on dsPIC33EPXXXMC20X/50X and PIC24EPXXXMC20X devices only.
- 2:** This pin is available on dsPIC33EPXXXGP/MC50X devices only.
- 3:** This is the default Fault on Reset for dsPIC33EPXXXMC20X/50X and PIC24EPXXXMC20X devices. See **Section 16.0 “High-Speed PWM Module (dsPIC33EPXXXMC20X/50X and PIC24EPXXXMC20X Devices Only)”** for more information.
- 4:** Not all pins are available in all packages variants. See the **“Pin Diagrams”** section for pin availability.
- 5:** There is an internal pull-up resistor connected to the TMS pin when the JTAG interface is active. See the JTAGEN bit field in Table 27-2.

## 2.0 GUIDELINES FOR GETTING STARTED WITH 16-BIT DIGITAL SIGNAL CONTROLLERS AND MICROCONTROLLERS

**Note 1:** This data sheet summarizes the features of the dsPIC33EPXXXGP50X, dsPIC33EPXXXMC20X/50X and PIC24EPXXXGP/MC20X families of devices. It is not intended to be a comprehensive reference source. To complement the information in this data sheet, refer to the related section of the “dsPIC33/PIC24 Family Reference Manual”, which is available from the Microchip web site ([www.microchip.com](http://www.microchip.com))

**2:** Some registers and associated bits described in this section may not be available on all devices. Refer to **Section 4.0 “Memory Organization”** in this data sheet for device-specific register and bit information.

### 2.1 Basic Connection Requirements

Getting started with the dsPIC33EPXXXGP50X, dsPIC33EPXXXMC20X/50X and PIC24EPXXXGP/MC20X families requires attention to a minimal set of device pin connections before proceeding with development. The following is a list of pin names, which must always be connected:

- All VDD and VSS pins  
(see **Section 2.2 “Decoupling Capacitors”**)
- All AVDD and AVSS pins (regardless if ADC module is not used)  
(see **Section 2.2 “Decoupling Capacitors”**)
- VCAP  
(see **Section 2.3 “CPU Logic Filter Capacitor Connection (VCAP)”**)
- MCLR pin  
(see **Section 2.4 “Master Clear (MCLR) Pin”**)
- PGECx/PGEDx pins used for In-Circuit Serial Programming™ (ICSP™) and debugging purposes  
(see **Section 2.5 “ICSP Pins”**)
- OSC1 and OSC2 pins when external oscillator source is used  
(see **Section 2.6 “External Oscillator Pins”**)

Additionally, the following pins may be required:

- VREF+/VREF- pins are used when external voltage reference for the ADC module is implemented

**Note:** The AVDD and AVSS pins must be connected, independent of the ADC voltage reference source.

### 2.2 Decoupling Capacitors

The use of decoupling capacitors on every pair of power supply pins, such as VDD, VSS, AVDD and AVSS is required.

Consider the following criteria when using decoupling capacitors:

- **Value and type of capacitor:** Recommendation of 0.1  $\mu\text{F}$  (100 nF), 10-20V. This capacitor should be a low-ESR and have resonance frequency in the range of 20 MHz and higher. It is recommended to use ceramic capacitors.
- **Placement on the printed circuit board:** The decoupling capacitors should be placed as close to the pins as possible. It is recommended to place the capacitors on the same side of the board as the device. If space is constricted, the capacitor can be placed on another layer on the PCB using a via; however, ensure that the trace length from the pin to the capacitor is within one-quarter inch (6 mm) in length.
- **Handling high-frequency noise:** If the board is experiencing high-frequency noise, above tens of MHz, add a second ceramic-type capacitor in parallel to the above described decoupling capacitor. The value of the second capacitor can be in the range of 0.01  $\mu\text{F}$  to 0.001  $\mu\text{F}$ . Place this second capacitor next to the primary decoupling capacitor. In high-speed circuit designs, consider implementing a decade pair of capacitances as close to the power and ground pins as possible. For example, 0.1  $\mu\text{F}$  in parallel with 0.001  $\mu\text{F}$ .
- **Maximizing performance:** On the board layout from the power supply circuit, run the power and return traces to the decoupling capacitors first, and then to the device pins. This ensures that the decoupling capacitors are first in the power chain. Equally important is to keep the trace length between the capacitor and the power pins to a minimum, thereby reducing PCB track inductance.

**REGISTER 3-2: CORCON: CORE CONTROL REGISTER**

R/W-0	U-0	R/W-0	R/W-0	R/W-0	R-0	R-0	R-0
VAR	—	US1 <sup>(1)</sup>	US0 <sup>(1)</sup>	EDT <sup>(1,2)</sup>	DL2 <sup>(1)</sup>	DL1 <sup>(1)</sup>	DL0 <sup>(1)</sup>
bit 15							bit 8

R/W-0	R/W-0	R/W-1	R/W-0	R/C-0	R-0	R/W-0	R/W-0
SATA <sup>(1)</sup>	SATB <sup>(1)</sup>	SATDW <sup>(1)</sup>	ACCSAT <sup>(1)</sup>	IPL3 <sup>(3)</sup>	SFA	RND <sup>(1)</sup>	IF <sup>(1)</sup>
bit 7							bit 0

<b>Legend:</b>	C = Clearable bit		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

- bit 15      **VAR:** Variable Exception Processing Latency Control bit  
1 = Variable exception processing latency is enabled  
0 = Fixed exception processing latency is enabled
- bit 14      **Unimplemented:** Read as '0'
- bit 13-12   **US<1:0>:** DSP Multiply Unsigned/Signed Control bits<sup>(1)</sup>  
11 = Reserved  
10 = DSP engine multiplies are mixed-sign  
01 = DSP engine multiplies are unsigned  
00 = DSP engine multiplies are signed
- bit 11      **EDT:** Early DO Loop Termination Control bit<sup>(1,2)</sup>  
1 = Terminates executing DO loop at end of current loop iteration  
0 = No effect
- bit 10-8   **DL<2:0>:** DO Loop Nesting Level Status bits<sup>(1)</sup>  
111 = 7 DO loops are active  
•  
•  
•  
001 = 1 DO loop is active  
000 = 0 DO loops are active
- bit 7      **SATA:** ACCA Saturation Enable bit<sup>(1)</sup>  
1 = Accumulator A saturation is enabled  
0 = Accumulator A saturation is disabled
- bit 6      **SATB:** ACCB Saturation Enable bit<sup>(1)</sup>  
1 = Accumulator B saturation is enabled  
0 = Accumulator B saturation is disabled
- bit 5      **SATDW:** Data Space Write from DSP Engine Saturation Enable bit<sup>(1)</sup>  
1 = Data Space write saturation is enabled  
0 = Data Space write saturation is disabled
- bit 4      **ACCSAT:** Accumulator Saturation Mode Select bit<sup>(1)</sup>  
1 = 9.31 saturation (super saturation)  
0 = 1.31 saturation (normal saturation)
- bit 3      **IPL3:** CPU Interrupt Priority Level Status bit<sup>(3)</sup>  
1 = CPU Interrupt Priority Level is greater than 7  
0 = CPU Interrupt Priority Level is 7 or less

- Note 1:** This bit is available on dsPIC33EPXXXMC20X/50X and dsPIC33EPXXXGP50X devices only.  
**2:** This bit is always read as '0'.  
**3:** The IPL3 bit is concatenated with the IPL<2:0> bits (SR<7:5>) to form the CPU Interrupt Priority Level.

FIGURE 4-14: DATA MEMORY MAP FOR PIC24EP128GP/MC20X/50X DEVICES

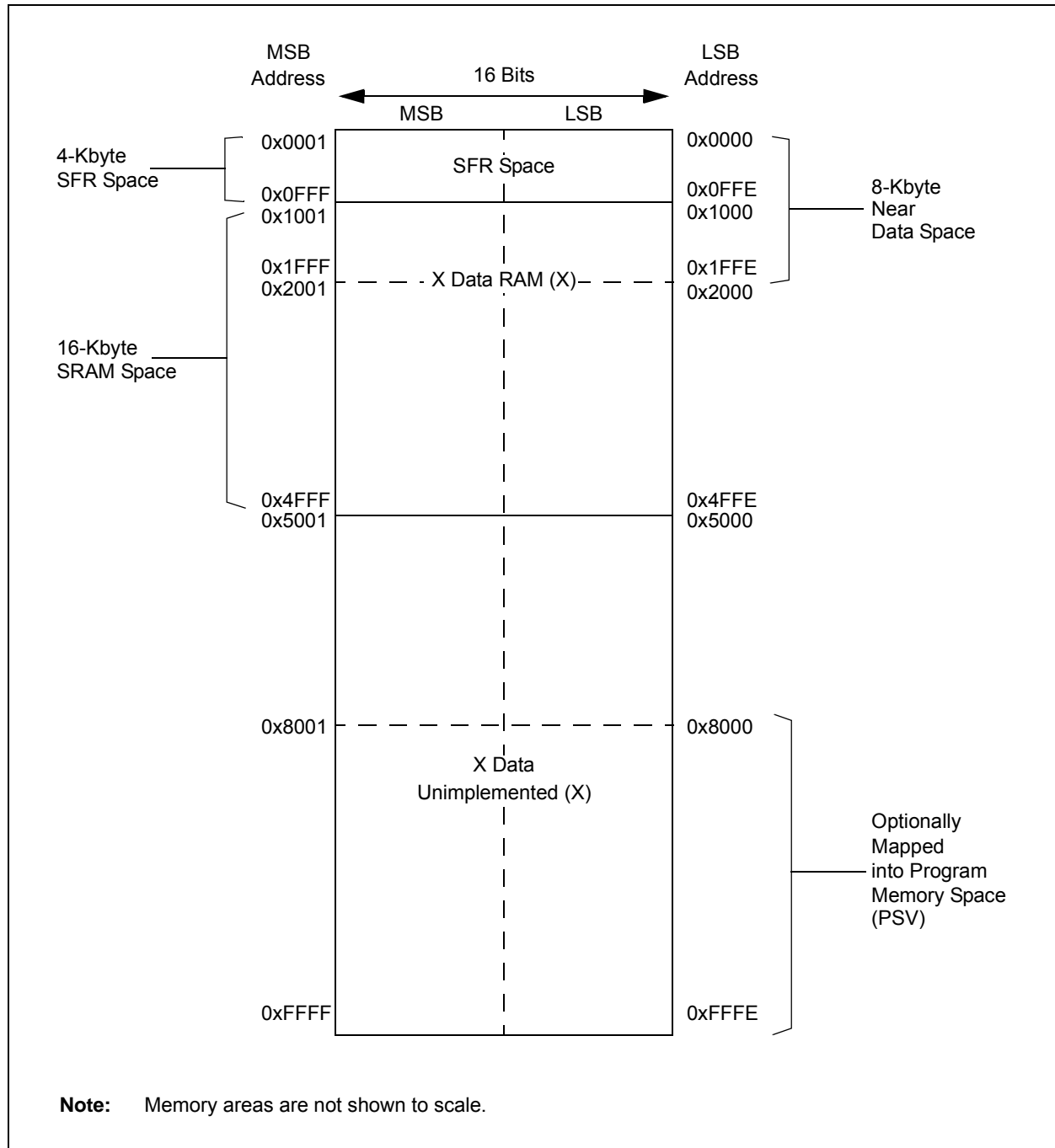


TABLE 4-11: PTG REGISTER MAP

File Name	Addr.	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	All Resets
PTGCST	0AC0	PTGEN	—	PTGSIDL	PTGTOGL	—	PTGSWT	PTGSSEN	PTGIVIS	PTGSTRT	PTGWTO	—	—	—	—	PTGITM<1:0>		0000
PTGCON	0AC2	PTGCLK<2:0>			PTGDIV<4:0>					PTGPWD<3:0>				—	PTGWDT<2:0>			0000
PTGBTE	0AC4	ADCTS<4:1>				IC4TSS	IC3TSS	IC2TSS	IC1TSS	OC4CS	OC3CS	OC2CS	OC1CS	OC4TSS	OC3TSS	OC2TSS	OC1TSS	0000
PTGHOLD	0AC6	PTGHOLD<15:0>																0000
PTGT0LIM	0AC8	PTGT0LIM<15:0>																0000
PTGT1LIM	0ACA	PTGT1LIM<15:0>																0000
PTGSDLIM	0ACC	PTGSDLIM<15:0>																0000
PTGC0LIM	0ACE	PTGC0LIM<15:0>																0000
PTGC1LIM	0AD0	PTGC1LIM<15:0>																0000
PTGADJ	0AD2	PTGADJ<15:0>																0000
PTGL0	0AD4	PTGL0<15:0>																0000
PTGQPTR	0AD6	—	—	—	—	—	—	—	—	—	—	—	PTGQPTR<4:0>					0000
PTGQUE0	0AD8	STEP1<7:0>								STEP0<7:0>								0000
PTGQUE1	0ADA	STEP3<7:0>								STEP2<7:0>								0000
PTGQUE2	0ADC	STEP5<7:0>								STEP4<7:0>								0000
PTGQUE3	0ADE	STEP7<7:0>								STEP6<7:0>								0000
PTGQUE4	0AE0	STEP9<7:0>								STEP8<7:0>								0000
PTGQUE5	0AE2	STEP11<7:0>								STEP10<7:0>								0000
PTGQUE6	0AE4	STEP13<7:0>								STEP12<7:0>								0000
PTGQUE7	0AE6	STEP15<7:0>								STEP14<7:0>								0000

**Legend:** — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

**TABLE 4-56: PORTA REGISTER MAP FOR PIC24EPXXXGP/MC203 AND dsPIC33EPXXXGP/MC203/503 DEVICES ONLY**

File Name	Addr.	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	All Resets
TRISA	0E00	—	—	—	—	—	—	—	TRISA8	—	—	—	TRISA4	TRISA3	TRISA2	TRISA1	TRISA0	011F
PORTA	0E02	—	—	—	—	—	—	—	RA8	—	—	—	RA4	RA3	RA2	RA1	RA0	0000
LATA	0E04	—	—	—	—	—	—	—	LATA8	—	—	—	LATA4	LATA3	LATA2	LA1TA1	LA0TA0	0000
ODCA	0E06	—	—	—	—	—	—	—	ODCA8	—	—	—	ODCA4	ODCA3	ODCA2	ODCA1	ODCA0	0000
CNENA	0E08	—	—	—	—	—	—	—	CNIEA8	—	—	—	CNIEA4	CNIEA3	CNIEA2	CNIEA1	CNIEA0	0000
CNPUA	0E0A	—	—	—	—	—	—	—	CNPUA8	—	—	—	CNPUA4	CNPUA3	CNPUA2	CNPUA1	CNPUA0	0000
CNPDA	0E0C	—	—	—	—	—	—	—	CNPDA8	—	—	—	CNPDA4	CNPDA3	CNPDA2	CNPDA1	CNPDA0	0000
ANSELA	0E0E	—	—	—	—	—	—	—	—	—	—	—	ANSA4	—	—	ANSA1	ANSA0	0013

**Legend:** — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

**TABLE 4-57: PORTB REGISTER MAP FOR PIC24EPXXXGP/MC203 AND dsPIC33EPXXXGP/MC203/503 DEVICES ONLY**

File Name	Addr.	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	All Resets
TRISB	0E10	TRISB15	TRISB14	TRISB13	TRISB12	TRISB11	TRISB10	TRISB9	TRISB8	TRISB7	TRISB6	TRISB5	TRISB4	TRISB3	TRISB2	TRISB1	TRISB0	FFFF
PORTB	0E12	RB15	RB14	RB13	RB12	RB11	RB10	RB9	RB8	RB7	RB6	RB5	RB4	RB3	RB2	RB1	RB0	xxxx
LATB	0E14	LATB15	LATB14	LATB13	LATB12	LATB11	LATB10	LATB9	LATB8	LATB7	LATB6	LATB5	LATB4	LATB3	LATB2	LATB1	LATB0	xxxx
ODCB	0E16	ODCB15	ODCB14	ODCB13	ODCB12	ODCB11	ODCB10	ODCB9	ODCB8	ODCB7	ODCB6	ODCB5	ODCB4	ODCB3	ODCB2	ODCB1	ODCB0	0000
CNENB	0E18	CNIEB15	CNIEB14	CNIEB13	CNIEB12	CNIEB11	CNIEB10	CNIEB9	CNIEB8	CNIEB7	CNIEB6	CNIEB5	CNIEB4	CNIEB3	CNIEB2	CNIEB1	CNIEB0	0000
CNPUB	0E1A	CNPUB15	CNPUB14	CNPUB13	CNPUB12	CNPUB11	CNPUB10	CNPUB9	CNPUB8	CNPUB7	CNPUB6	CNPUB5	CNPUB4	CNPUB3	CNPUB2	CNPUB1	CNPUB0	0000
CNPDB	0E1C	CNPDB15	CNPDB14	CNPDB13	CNPDB12	CNPDB11	CNPDB10	CNPDB9	CNPDB8	CNPDB7	CNPDB6	CNPDB5	CNPDB4	CNPDB3	CNPDB2	CNPDB1	CNPDB0	0000
ANSELB	0E1E	—	—	—	—	—	—	—	ANSB8	—	—	—	—	ANSB3	ANSB2	ANSB1	ANSB0	010F

**Legend:** x = unknown value on Reset, — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

**TABLE 4-58: PORTC REGISTER MAP FOR PIC24EPXXXGP/MC203 AND dsPIC33EPXXXGP/MC203/503 DEVICES ONLY**

File Name	Addr.	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	All Resets
TRISC	0E20	—	—	—	—	—	—	—	TRISC8	—	—	—	—	—	—	TRISC1	TRISC0	0103
PORTC	0E22	—	—	—	—	—	—	—	RC8	—	—	—	—	—	—	RC1	RC0	xxxx
LATC	0E24	—	—	—	—	—	—	—	LATC8	—	—	—	—	—	—	LATC1	LATC0	xxxx
ODCC	0E26	—	—	—	—	—	—	—	ODCC8	—	—	—	—	—	—	ODCC1	ODCC0	0000
CNENC	0E28	—	—	—	—	—	—	—	CNIEC8	—	—	—	—	—	—	CNIEC1	CNIEC0	0000
CNPUC	0E2A	—	—	—	—	—	—	—	CNPUC8	—	—	—	—	—	—	CNPUC1	CNPUC0	0000
CNPDC	0E2C	—	—	—	—	—	—	—	CNPDC8	—	—	—	—	—	—	CNPDC1	CNPDC0	0000
ANSELC	0E2E	—	—	—	—	—	—	—	—	—	—	—	—	—	—	ANSC1	ANSC0	0003

**Legend:** x = unknown value on Reset, — = unimplemented, read as '0'. Reset values are shown in hexadecimal.



## 10.0 POWER-SAVING FEATURES

**Note 1:** This data sheet summarizes the features of the dsPIC33EPXXXGP50X, dsPIC33EPXXXMC20X/50X and PIC24EPXXXGP/MC20X families of devices. It is not intended to be a comprehensive reference source. To complement the information in this data sheet, refer to “**Watchdog Timer and Power-Saving Modes**” (DS70615) in the “*dsPIC33/PIC24 Family Reference Manual*”, which is available from the Microchip web site ([www.microchip.com](http://www.microchip.com)).

**2:** Some registers and associated bits described in this section may not be available on all devices. Refer to **Section 4.0 “Memory Organization”** in this data sheet for device-specific register and bit information.

The dsPIC33EPXXXGP50X, dsPIC33EPXXXMC20X/50X and PIC24EPXXXGP/MC20X devices provide the ability to manage power consumption by selectively managing clocking to the CPU and the peripherals. In general, a lower clock frequency and a reduction in the number of peripherals being clocked constitutes lower consumed power.

dsPIC33EPXXXGP50X, dsPIC33EPXXXMC20X/50X and PIC24EPXXXGP/MC20X devices can manage power consumption in four ways:

- Clock Frequency
- Instruction-Based Sleep and Idle modes
- Software-Controlled Doze mode
- Selective Peripheral Control in Software

Combinations of these methods can be used to selectively tailor an application's power consumption while still maintaining critical application features, such as timing-sensitive communications.

## 10.1 Clock Frequency and Clock Switching

The dsPIC33EPXXXGP50X, dsPIC33EPXXXMC20X/50X and PIC24EPXXXGP/MC20X devices allow a wide range of clock frequencies to be selected under application control. If the system clock configuration is not locked, users can choose low-power or high-precision oscillators by simply changing the NOSCx bits (OSCCON<10:8>). The process of changing a system clock during operation, as well as limitations to the process, are discussed in more detail in **Section 9.0 “Oscillator Configuration”**.

## 10.2 Instruction-Based Power-Saving Modes

The dsPIC33EPXXXGP50X, dsPIC33EPXXXMC20X/50X and PIC24EPXXXGP/MC20X devices have two special power-saving modes that are entered through the execution of a special PWRSAV instruction. Sleep mode stops clock operation and halts all code execution. Idle mode halts the CPU and code execution, but allows peripheral modules to continue operation. The assembler syntax of the PWRSAV instruction is shown in Example 10-1.

**Note:** SLEEP\_MODE and IDLE\_MODE are constants defined in the assembler include file for the selected device.

Sleep and Idle modes can be exited as a result of an enabled interrupt, WDT time-out or a device Reset. When the device exits these modes, it is said to “wake-up”.

### EXAMPLE 10-1: PWRSAV INSTRUCTION SYNTAX

```
PWRSAV #SLEEP_MODE    ; Put the device into Sleep mode
PWRSAV #IDLE_MODE      ; Put the device into Idle mode
```

**REGISTER 11-12: RPINR22: PERIPHERAL PIN SELECT INPUT REGISTER 22**

U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
—	SCK2INR<6:0>						
bit 15							bit 8

U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
—	SDI2R<6:0>						
bit 7							bit 0

**Legend:**

R = Readable bit

W = Writable bit

U = Unimplemented bit, read as '0'

-n = Value at POR

'1' = Bit is set

'0' = Bit is cleared

x = Bit is unknown

bit 15 **Unimplemented:** Read as '0'

bit 14-8 **SCK2INR<6:0>:** Assign SPI2 Clock Input (SCK2) to the Corresponding RPn Pin bits  
(see Table 11-2 for input pin selection numbers)

1111001 = Input tied to RPI121

.

.

.

0000001 = Input tied to CMP1

0000000 = Input tied to Vss

bit 7 **Unimplemented:** Read as '0'

bit 6-0 **SDI2R<6:0>:** Assign SPI2 Data Input (SDI2) to the Corresponding RPn Pin bits  
(see Table 11-2 for input pin selection numbers)

1111001 = Input tied to RPI121

.

.

.

0000001 = Input tied to CMP1

0000000 = Input tied to Vss

## 16.2 PWM Resources

Many useful resources are provided on the main product page of the Microchip web site for the devices listed in this data sheet. This product page, which can be accessed using this link, contains the latest updates and additional information.

<p><b>Note:</b> In the event you are not able to access the product page using the link above, enter this URL in your browser: <a href="http://www.microchip.com/wwwproducts/Devices.aspx?dDocName=en555464">http://www.microchip.com/wwwproducts/Devices.aspx?dDocName=en555464</a></p>
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### 16.2.1 KEY RESOURCES

- **“High-Speed PWM”** (DS70645) in the *“dsPIC33/PIC24 Family Reference Manual”*
- Code Samples
- Application Notes
- Software Libraries
- Webinars
- All Related *“dsPIC33/PIC24 Family Reference Manual”* Sections
- Development Tools

## 19.1 I<sup>2</sup>C Resources

Many useful resources are provided on the main product page of the Microchip web site for the devices listed in this data sheet. This product page, which can be accessed using this link, contains the latest updates and additional information.

<p><b>Note:</b> In the event you are not able to access the product page using the link above, enter this URL in your browser: <a href="http://www.microchip.com/wwwproducts/Devices.aspx?dDocName=en555464">http://www.microchip.com/wwwproducts/Devices.aspx?dDocName=en555464</a></p>
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### 19.1.1 KEY RESOURCES

- **“Inter-Integrated Circuit (I<sup>2</sup>C)”** (DS70330) in the *“dsPIC33/PIC24 Family Reference Manual”*
- Code Samples
- Application Notes
- Software Libraries
- Webinars
- All Related *“dsPIC33/PIC24 Family Reference Manual”* Sections
- Development Tools

**REGISTER 21-7: CxINTE: ECANx INTERRUPT ENABLE REGISTER**

U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
—	—	—	—	—	—	—	—
bit 15							bit 8

R/W-0	R/W-0	R/W-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0
IVRIE	WAKIE	ERRIE	—	FIFOIE	RBOVIE	RBIE	TBIE
bit 7							bit 0

**Legend:**

R = Readable bit

W = Writable bit

U = Unimplemented bit, read as '0'

-n = Value at POR

'1' = Bit is set

'0' = Bit is cleared

x = Bit is unknown

- bit 15-8      **Unimplemented:** Read as '0'
- bit 7      **IVRIE:** Invalid Message Interrupt Enable bit  
1 = Interrupt request is enabled  
0 = Interrupt request is not enabled
- bit 6      **WAKIE:** Bus Wake-up Activity Interrupt Enable bit  
1 = Interrupt request is enabled  
0 = Interrupt request is not enabled
- bit 5      **ERRIE:** Error Interrupt Enable bit  
1 = Interrupt request is enabled  
0 = Interrupt request is not enabled
- bit 4      **Unimplemented:** Read as '0'
- bit 3      **FIFOIE:** FIFO Almost Full Interrupt Enable bit  
1 = Interrupt request is enabled  
0 = Interrupt request is not enabled
- bit 2      **RBOVIE:** RX Buffer Overflow Interrupt Enable bit  
1 = Interrupt request is enabled  
0 = Interrupt request is not enabled
- bit 1      **RBIE:** RX Buffer Interrupt Enable bit  
1 = Interrupt request is enabled  
0 = Interrupt request is not enabled
- bit 0      **TBIE:** TX Buffer Interrupt Enable bit  
1 = Interrupt request is enabled  
0 = Interrupt request is not enabled

**REGISTER 21-17: CxRXFnEID: ECANx ACCEPTANCE FILTER n EXTENDED IDENTIFIER REGISTER (n = 0-15)**

R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x
EID15	EID14	EID13	EID12	EID11	EID10	EID9	EID8
bit 15							bit 8

R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x
EID7	EID6	EID5	EID4	EID3	EID2	EID1	EID0
bit 7							bit 0

**Legend:**

R = Readable bit                      W = Writable bit                      U = Unimplemented bit, read as '0'  
-n = Value at POR                      '1' = Bit is set                      '0' = Bit is cleared                      x = Bit is unknown

bit 15-0                      **EID<15:0>**: Extended Identifier bits  
1 = Message address bit, EIDx, must be '1' to match filter  
0 = Message address bit, EIDx, must be '0' to match filter

**REGISTER 21-18: CxFMSKSEL1: ECANx FILTER 7-0 MASK SELECTION REGISTER 1**

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
F7MSK<1:0>		F6MSK<1:0>		F5MSK<1:0>		F4MSK<1:0>	
bit 15							bit 8

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
F3MSK<1:0>		F2MSK<1:0>		F1MSK<1:0>		F0MSK<1:0>	
bit 7							bit 0

**Legend:**

R = Readable bit                      W = Writable bit                      U = Unimplemented bit, read as '0'  
-n = Value at POR                      '1' = Bit is set                      '0' = Bit is cleared                      x = Bit is unknown

bit 15-14                      **F7MSK<1:0>**: Mask Source for Filter 7 bits  
11 = Reserved  
10 = Acceptance Mask 2 registers contain mask  
01 = Acceptance Mask 1 registers contain mask  
00 = Acceptance Mask 0 registers contain mask

bit 13-12                      **F6MSK<1:0>**: Mask Source for Filter 6 bits (same values as bits<15:14>)

bit 11-10                      **F5MSK<1:0>**: Mask Source for Filter 5 bits (same values as bits<15:14>)

bit 9-8                      **F4MSK<1:0>**: Mask Source for Filter 4 bits (same values as bits<15:14>)

bit 7-6                      **F3MSK<1:0>**: Mask Source for Filter 3 bits (same values as bits<15:14>)

bit 5-4                      **F2MSK<1:0>**: Mask Source for Filter 2 bits (same values as bits<15:14>)

bit 3-2                      **F1MSK<1:0>**: Mask Source for Filter 1 bits (same values as bits<15:14>)

bit 1-0                      **F0MSK<1:0>**: Mask Source for Filter 0 bits (same values as bits<15:14>)

## 24.0 PERIPHERAL TRIGGER GENERATOR (PTG) MODULE

**Note 1:** This data sheet summarizes the features of the dsPIC33EPXXXGP50X, dsPIC33EPXXXMC20X/50X and PIC24EPXXXGP/MC20X families of devices. It is not intended to be a comprehensive reference source. To complement the information in this data sheet, refer to “**Peripheral Trigger Generator (PTG)**” (DS70669) in the “*dsPIC33/PIC24 Family Reference Manual*”, which is available from the Microchip web site ([www.microchip.com](http://www.microchip.com)).

**2:** Some registers and associated bits described in this section may not be available on all devices. Refer to **Section 4.0 “Memory Organization”** in this data sheet for device-specific register and bit information.

### 24.1 Module Introduction

The Peripheral Trigger Generator (PTG) provides a means to schedule complex high-speed peripheral operations that would be difficult to achieve using software. The PTG module uses 8-bit commands, called “Steps”, that the user writes to the PTG Queue registers (PTGQUE0-PTGQUE7), which perform operations, such as wait for input signal, generate output trigger and wait for timer.

The PTG module has the following major features:

- Multiple clock sources
- Two 16-bit general purpose timers
- Two 16-bit general limit counters
- Configurable for rising or falling edge triggering
- Generates processor interrupts to include:
  - Four configurable processor interrupts
  - Interrupt on a Step event in Single-Step mode
  - Interrupt on a PTG Watchdog Timer time-out
- Able to receive trigger signals from these peripherals:
  - ADC
  - PWM
  - Output Compare
  - Input Capture
  - Op Amp/Comparator
  - INT2
- Able to trigger or synchronize to these peripherals:
  - Watchdog Timer
  - Output Compare
  - Input Capture
  - ADC
  - PWM
  - Op Amp/Comparator

TABLE 30-12: DC CHARACTERISTICS: I/O PIN OUTPUT SPECIFICATIONS

DC CHARACTERISTICS			Standard Operating Conditions: 3.0V to 3.6V (unless otherwise stated) Operating temperature -40°C ≤ TA ≤ +85°C for Industrial -40°C ≤ TA ≤ +125°C for Extended				
Param.	Symbol	Characteristic	Min.	Typ.	Max.	Units	Conditions
DO10	VOL	<b>Output Low Voltage</b> 4x Sink Driver Pins <sup>(2)</sup>	—	—	0.4	V	VDD = 3.3V, IOL ≤ 6 mA, -40°C ≤ TA ≤ +85°C IOL ≤ 5 mA, +85°C < TA ≤ +125°C
		<b>Output Low Voltage</b> 8x Sink Driver Pins <sup>(3)</sup>	—	—	0.4	V	VDD = 3.3V, IOL ≤ 12 mA, -40°C ≤ TA ≤ +85°C IOL ≤ 8 mA, +85°C < TA ≤ +125°C
DO20	VOH	<b>Output High Voltage</b> 4x Source Driver Pins <sup>(2)</sup>	2.4	—	—	V	IOH ≥ -10 mA, VDD = 3.3V
		<b>Output High Voltage</b> 8x Source Driver Pins <sup>(3)</sup>	2.4	—	—	V	IOH ≥ -15 mA, VDD = 3.3V
DO20A	VOH1	<b>Output High Voltage</b> 4x Source Driver Pins <sup>(2)</sup>	1.5 <sup>(1)</sup>	—	—	V	IOH ≥ -14 mA, VDD = 3.3V
			2.0 <sup>(1)</sup>	—	—		IOH ≥ -12 mA, VDD = 3.3V
			3.0 <sup>(1)</sup>	—	—		IOH ≥ -7 mA, VDD = 3.3V
		<b>Output High Voltage</b> 8x Source Driver Pins <sup>(3)</sup>	1.5 <sup>(1)</sup>	—	—	V	IOH ≥ -22 mA, VDD = 3.3V
			2.0 <sup>(1)</sup>	—	—		IOH ≥ -18 mA, VDD = 3.3V
			3.0 <sup>(1)</sup>	—	—		IOH ≥ -10 mA, VDD = 3.3V

**Note 1:** Parameters are characterized but not tested.

**2:** Includes all I/O pins that are not 8x Sink Driver pins (see below).

**3:** Includes the following pins:

**For devices with less than 64 pins:** RA3, RA4, RA9, RB<7:15> and RC3

**For 64-pin devices:** RA4, RA9, RB<7:15>, RC3 and RC15

TABLE 30-13: ELECTRICAL CHARACTERISTICS: BOR

DC CHARACTERISTICS			Standard Operating Conditions: 3.0V to 3.6V (unless otherwise stated) <sup>(1)</sup> Operating temperature -40°C ≤ TA ≤ +85°C for Industrial -40°C ≤ TA ≤ +125°C for Extended				
Param No.	Symbol	Characteristic	Min. <sup>(2)</sup>	Typ.	Max.	Units	Conditions
BO10	VBOR	BOR Event on VDD Transition High-to-Low	2.65	—	2.95	V	VDD (Notes 2 and 3)

**Note 1:** Device is functional at VBORMIN < VDD < VDDMIN, but will have degraded performance. Device functionality is tested, but not characterized. Analog modules (ADC, op amp/comparator and comparator voltage reference) may have degraded performance.

**2:** Parameters are for design guidance only and are not tested in manufacturing.

**3:** The VBOR specification is relative to VDD.



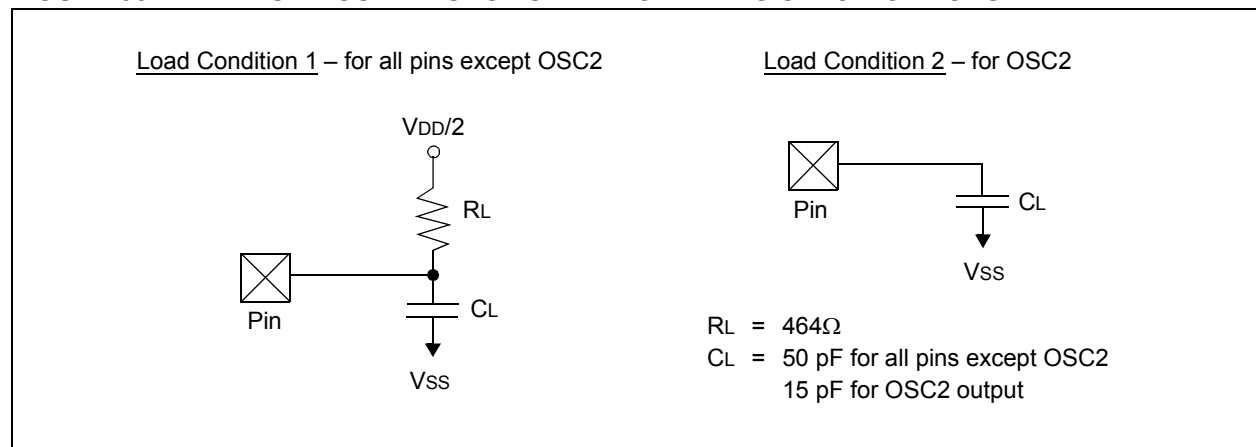
## 30.2 AC Characteristics and Timing Parameters

This section defines dsPIC33EPXXXGP50X, dsPIC33EPXXXMC20X/50X and PIC24EPXXXGP/MC20X AC characteristics and timing parameters.

**TABLE 30-15: TEMPERATURE AND VOLTAGE SPECIFICATIONS – AC**

<b>AC CHARACTERISTICS</b>	<b>Standard Operating Conditions: 3.0V to 3.6V (unless otherwise stated)</b> Operating temperature $-40^{\circ}\text{C} \leq T_A \leq +85^{\circ}\text{C}$ for Industrial $-40^{\circ}\text{C} \leq T_A \leq +125^{\circ}\text{C}$ for Extended Operating voltage $V_{DD}$ range as described in <b>Section 30.1 “DC Characteristics”</b> .
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**FIGURE 30-1: LOAD CONDITIONS FOR DEVICE TIMING SPECIFICATIONS**

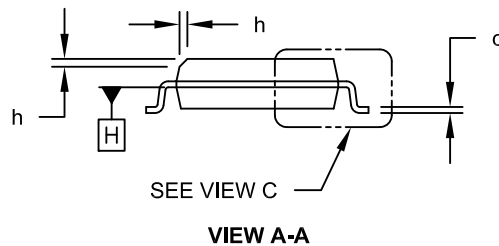
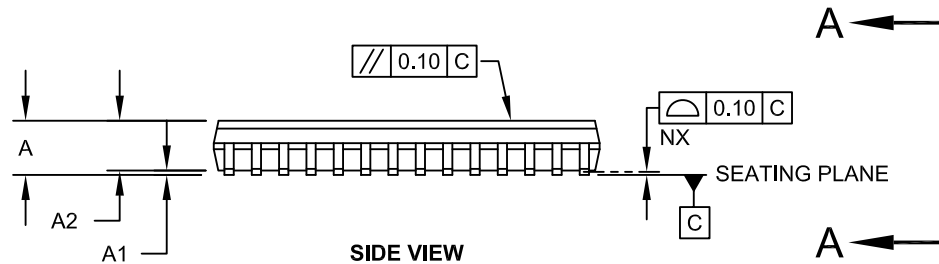
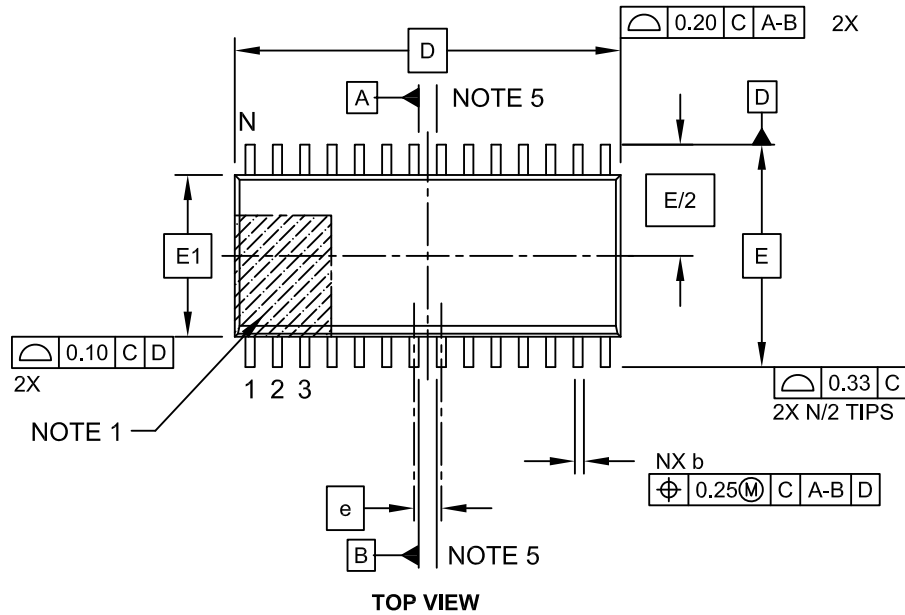


**TABLE 30-16: CAPACITIVE LOADING REQUIREMENTS ON OUTPUT PINS**

Param No.	Symbol	Characteristic	Min.	Typ.	Max.	Units	Conditions
DO50	Cosco	OSC2 Pin	—	—	15	pF	In XT and HS modes, when external clock is used to drive OSC1
DO56	Cio	All I/O Pins and OSC2	—	—	50	pF	EC mode
DO58	CB	SCLx, SDAx	—	—	400	pF	In I <sup>2</sup> C™ mode

28-Lead Plastic Small Outline (SO) - Wide, 7.50 mm Body [SOIC]

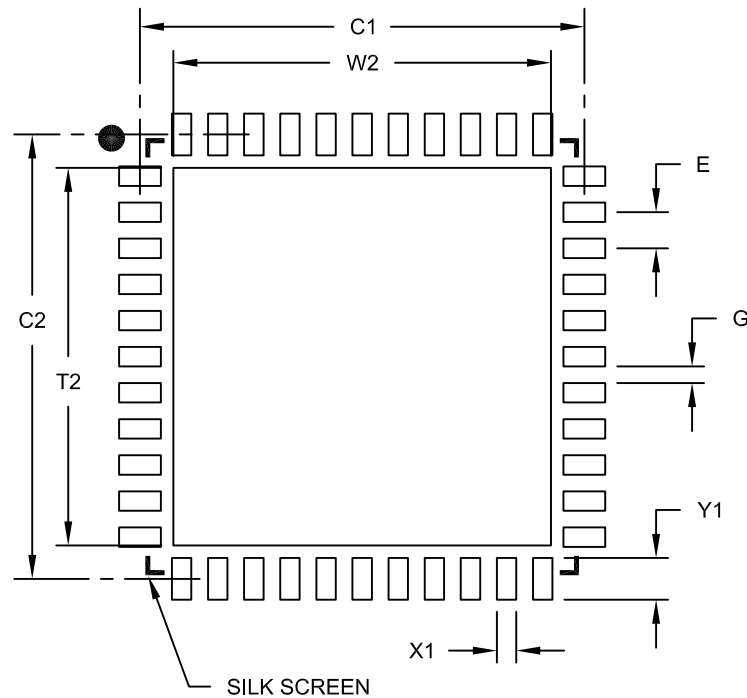
**Note:** For the most current package drawings, please see the Microchip Packaging Specification located at <http://www.microchip.com/packaging>



Microchip Technology Drawing C04-052C Sheet 1 of 2

44-Lead Plastic Quad Flat, No Lead Package (ML) - 8x8 mm Body [QFN]

**Note:** For the most current package drawings, please see the Microchip Packaging Specification located at <http://www.microchip.com/packaging>



RECOMMENDED LAND PATTERN

Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Contact Pitch	E	0.65 BSC		
Optional Center Pad Width	W2			6.60
Optional Center Pad Length	T2			6.60
Contact Pad Spacing	C1		8.00	
Contact Pad Spacing	C2		8.00	
Contact Pad Width (X44)	X1			0.35
Contact Pad Length (X44)	Y1			0.85
Distance Between Pads	G	0.25		

Notes:

1. Dimensioning and tolerancing per ASME Y14.5M

BSC: Basic Dimension. Theoretically exact value shown without tolerances.

Microchip Technology Drawing No. C04-2103B

**Revision H (August 2013)**

This revision includes minor typographical and formatting changes throughout the text.

Other major changes are referenced by their respective section in Table A-6.

**TABLE A-6: MAJOR SECTION UPDATES**

Section Name	Update Description
<b>Cover Section</b>	<ul style="list-style-type: none"> <li>• Adds Peripheral Pin Select (PPS) to allow Digital Function Remapping and Change Notification Interrupts to Input/Output section</li> <li>• Adds heading information to 64-Pin TQFP</li> </ul>
<b>Section 4.0 “Memory Organization”</b>	<ul style="list-style-type: none"> <li>• Corrects Reset values for ANSELE, TRISF, TRISC, ANSELC and TRISA</li> <li>• Corrects address range from 0x2FFF to 0x7FFF</li> <li>• Corrects DSRPAG and DSWPAG (now 3 hex digits)</li> <li>• Changes Call Stack Frame from &lt;15:1&gt; to PC&lt;15:0&gt;</li> <li>• Word length in Figure 4-20 is changed to 50 words for clarity</li> </ul>
<b>Section 5.0 “Flash Program Memory”</b>	<ul style="list-style-type: none"> <li>• Corrects descriptions of NVM registers</li> </ul>
<b>Section 9.0 “Oscillator Configuration”</b>	<ul style="list-style-type: none"> <li>• Removes resistor from Figure 9-1</li> <li>• Adds Fast RC Oscillator with Divide-by-16 (FRCDIV16) row to Table 9-1</li> <li>• Removes incorrect information from ROI bit in Register 9-2</li> </ul>
<b>Section 14.0 “Input Capture”</b>	<ul style="list-style-type: none"> <li>• Changes 31 user-selectable Trigger/Sync interrupts to 19 user-selectable Trigger/Sync interrupts</li> <li>• Corrects ICTSEL&lt;12:10&gt; bits (now ICTSEL&lt;2:0&gt;)</li> </ul>
<b>Section 17.0 “Quadrature Encoder Interface (QEI) Module (dsPIC33EPXXXMC20X/50X and PIC24EPXXXMC20X Devices Only)”</b>	<ul style="list-style-type: none"> <li>• Corrects QCAPEN bit description</li> </ul>
<b>Section 19.0 “Inter-Integrated Circuit™ (I<sup>2</sup>C™)”</b>	<ul style="list-style-type: none"> <li>• Adds note to clarify that 100kbit/sec operation of I<sup>2</sup>C is not possible at high processor speeds</li> </ul>
<b>Section 22.0 “Charge Time Measurement Unit (CTMU)”</b>	<ul style="list-style-type: none"> <li>• Clarifies Figure 22-1 to accurately reflect peripheral behavior</li> </ul>
<b>Section 23.0 “10-Bit/12-Bit Analog-to-Digital Converter (ADC)”</b>	<ul style="list-style-type: none"> <li>• Correct Figure 23-1 (changes CH123x to CH123Sx)</li> </ul>
<b>Section 24.0 “Peripheral Trigger Generator (PTG) Module”</b>	<ul style="list-style-type: none"> <li>• Adds footnote to Register 24-1 (In order to operate with CVRSS=1, at least one of the comparator modules must be enabled).</li> </ul>
<b>Section 25.0 “Op Amp/Comparator Module”</b>	<ul style="list-style-type: none"> <li>• Adds note to Figure 25-3 (In order to operate with CVRSS=1, at least one of the comparator modules must be enabled)</li> <li>• Adds footnote to Register 25-2 (COE is not available when OPMODE (CMxCON&lt;10&gt;) = 1)</li> </ul>
<b>Section 27.0 “Special Features”</b>	<ul style="list-style-type: none"> <li>• Corrects the bit description for FNOSC&lt;2:0&gt;</li> </ul>
<b>Section 30.0 “Electrical Characteristics”</b>	<ul style="list-style-type: none"> <li>• Corrects 512K part power-down currents based on test data</li> <li>• Corrects WDT timing limits based on LPRC oscillator tolerance</li> </ul>
<b>Section 31.0 “High-Temperature Electrical Characteristics”</b>	<ul style="list-style-type: none"> <li>• Adds Table 31-5 (DC Characteristics: Idle Current (I<sub>IDLE</sub>))</li> </ul>

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