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Applications of "<u>Embedded -</u> <u>Microcontrollers</u>"

Details

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Product Status	Active
Core Processor	PIC
Core Size	16-Bit
Speed	70 MIPs
Connectivity	I²C, IrDA, LINbus, QEI, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, DMA, Motor Control PWM, POR, PWM, WDT
Number of I/O	35
Program Memory Size	32KB (10.7K x 24)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	2K x 16
Voltage - Supply (Vcc/Vdd)	3V ~ 3.6V
Data Converters	A/D 9x10b/12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	44-VQFN Exposed Pad
Supplier Device Package	44-QFN (8x8)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/pic24ep32mc204-i-ml

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3.5 **Programmer's Model**

The programmer's model for the dsPIC33EPXXXGP50X, dsPIC33EPXXXMC20X/50X and PIC24EPXXXGP/MC20X is shown in Figure 3-2. All registers in the programmer's model are memory mapped and can be manipulated directly by instructions. Table 3-1 lists a description of each register.

In addition to the registers contained in the programmer's model, the dsPIC33EPXXXGP50X, dsPIC33EPXXXMC20X/50X and PIC24EPXXXGP/

MC20X devices contain control registers for Modulo Addressing (dsPIC33EPXXXMC20X/50X and dsPIC33EPXXXGP50X devices only), Bit-Reversed Addressing (dsPIC33EPXXXMC20X/50X and dsPIC33EPXXXGP50X devices only) and interrupts. These registers are described in subsequent sections of this document.

All registers associated with the programmer's model are memory mapped, as shown in Table 4-1.

Register(s) Name	Description
W0 through W15	Working Register Array
ACCA, ACCB	40-Bit DSP Accumulators
PC	23-Bit Program Counter
SR	ALU and DSP Engine STATUS Register
SPLIM	Stack Pointer Limit Value Register
TBLPAG	Table Memory Page Address Register
DSRPAG	Extended Data Space (EDS) Read Page Register
DSWPAG	Extended Data Space (EDS) Write Page Register
RCOUNT	REPEAT Loop Count Register
DCOUNT ⁽¹⁾	DO Loop Count Register
DOSTARTH ^(1,2) , DOSTARTL ^(1,2)	DO Loop Start Address Register (High and Low)
DOENDH ⁽¹⁾ , DOENDL ⁽¹⁾	DO Loop End Address Register (High and Low)
CORCON	Contains DSP Engine, DO Loop Control and Trap Status bits

TABLE 3-1: PROGRAMMER'S MODEL REGISTER DESCRIPTIONS

Note 1: This register is available on dsPIC33EPXXXMC20X/50X and dsPIC33EPXXXGP50X devices only.

2: The DOSTARTH and DOSTARTL registers are read-only.

IADLE 4-2	:s: ⊏	CANT REGISTER WAP WHEN WIN (CICIRLICOS) = 1 FO						DR dspic33epaaamic/gp30a devices oner (continued)										
File Name	Addr	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	All Resets
C1RXF11EID	046E		EID<15:8>								EID<	7:0>				xxxx		
C1RXF12SID	0470		SID<10:3>						SID<2:0>		—	EXIDE	_	EID<1	7:16>	xxxx		
C1RXF12EID	0472	EID<15:8>								EID<	7:0>				xxxx			
C1RXF13SID	0474		SID<10:3>						SID<2:0>		_	EXIDE	_	EID<1	7:16>	xxxx		
C1RXF13EID	0476		EID<15:8>								EID<	7:0>				xxxx		
C1RXF14SID	0478		SID<10:3>						SID<2:0>		_	EXIDE	_	EID<1	7:16>	xxxx		
C1RXF14EID	047A		EID<15:8>								EID<	7:0>				xxxx		
C1RXF15SID	047C		SID<10:3>						SID<2:0>		_	EXIDE	_	EID<1	7:16>	xxxx		
C1RXF15EID	047E				EID<	:15:8>							EID<	7:0>				xxxx

ECANI DECISTED MAD WHEN WIN (CICTDI 1 -0.) 1 EOD doDIC22EDXXXMC/CDE0X DEVICES ONLY (CONTINUED) 1 22.

Legend: x = unknown value on Reset, — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

4.6 Modulo Addressing (dsPIC33EPXXXMC20X/50X and dsPIC33EPXXXGP50X Devices Only)

Modulo Addressing mode is a method of providing an automated means to support circular data buffers using hardware. The objective is to remove the need for software to perform data address boundary checks when executing tightly looped code, as is typical in many DSP algorithms.

Modulo Addressing can operate in either Data or Program Space (since the Data Pointer mechanism is essentially the same for both). One circular buffer can be supported in each of the X (which also provides the pointers into Program Space) and Y Data Spaces. Modulo Addressing can operate on any W Register Pointer. However, it is not advisable to use W14 or W15 for Modulo Addressing since these two registers are used as the Stack Frame Pointer and Stack Pointer, respectively.

In general, any particular circular buffer can be configured to operate in only one direction, as there are certain restrictions on the buffer start address (for incrementing buffers) or end address (for decrementing buffers), based upon the direction of the buffer.

The only exception to the usage restrictions is for buffers that have a power-of-two length. As these buffers satisfy the start and end address criteria, they can operate in a bidirectional mode (that is, address boundary checks are performed on both the lower and upper address boundaries).

4.6.1 START AND END ADDRESS

The Modulo Addressing scheme requires that a starting and ending address be specified, and loaded into the 16-bit Modulo Buffer Address registers: XMODSRT, XMODEND, YMODSRT and YMODEND (see Table 4-1).

Note:	Y space Modulo Addressing EA calcula-								
	tions assume word-sized data (LSb of								
	every EA is always clear).								

The length of a circular buffer is not directly specified. It is determined by the difference between the corresponding start and end addresses. The maximum possible length of the circular buffer is 32K words (64 Kbytes).

4.6.2 W ADDRESS REGISTER SELECTION

The Modulo and Bit-Reversed Addressing Control register, MODCON<15:0>, contains enable flags as well as a W register field to specify the W Address registers. The XWM and YWM fields select the registers that operate with Modulo Addressing:

- If XWM = 1111, X RAGU and X WAGU Modulo Addressing is disabled
- If YWM = 1111, Y AGU Modulo Addressing is disabled

The X Address Space Pointer W register (XWM), to which Modulo Addressing is to be applied, is stored in MODCON<3:0> (see Table 4-1). Modulo Addressing is enabled for X Data Space when XWM is set to any value other than '1111' and the XMODEN bit is set (MODCON<15>).

The Y Address Space Pointer W register (YWM), to which Modulo Addressing is to be applied, is stored in MODCON<7:4>. Modulo Addressing is enabled for Y Data Space when YWM is set to any value other than '1111' and the YMODEN bit is set at MODCON<14>.



FIGURE 4-20: MODULO ADDRESSING OPERATION EXAMPLE

6.0 RESETS

- Note 1: This data sheet summarizes the features of the dsPIC33EPXXXGP50X, dsPIC33EPXXXMC20X/50X and PIC24EPXXXGP/MC20X families of devices. It is not intended to be a comprehensive reference source. To complement the information in this data sheet, refer to "Reset" (DS70602) in the "dsPIC33/PIC24 Family Reference Manual", which is available from the Microchip web site (www.microchip.com).
 - 2: Some registers and associated bits described in this section may not be available on all devices. Refer to Section 4.0 "Memory Organization" in this data sheet for device-specific register and bit information.

The Reset module combines all Reset sources and controls the device Master Reset Signal, SYSRST. The following is a list of device Reset sources:

- · POR: Power-on Reset
- · BOR: Brown-out Reset
- MCLR: Master Clear Pin Reset
- SWR: RESET Instruction
- WDTO: Watchdog Timer Time-out Reset
- CM: Configuration Mismatch Reset
- TRAPR: Trap Conflict Reset
- IOPUWR: Illegal Condition Device Reset
- Illegal Opcode Reset
- Uninitialized W Register Reset
- Security Reset

FIGURE 6-1: RESET SYSTEM BLOCK DIAGRAM

A simplified block diagram of the Reset module is shown in Figure 6-1.

Any active source of Reset will make the SYSRST signal active. On system Reset, some of the registers associated with the CPU and peripherals are forced to a known Reset state and some are unaffected.

Note: Refer to the specific peripheral section or Section 4.0 "Memory Organization" of this manual for register Reset states.

All types of device Reset set a corresponding status bit in the RCON register to indicate the type of Reset (see Register 6-1).

A POR clears all the bits, except for the POR and BOR bits (RCON<1:0>), that are set. The user application can set or clear any bit at any time during code execution. The RCON bits only serve as status bits. Setting a particular Reset status bit in software does not cause a device Reset to occur.

The RCON register also has other bits associated with the Watchdog Timer and device power-saving states. The function of these bits is discussed in other sections of this manual.

Note: The status bits in the RCON register should be cleared after they are read so that the next RCON register value after a device Reset is meaningful.

For all Resets, the default clock source is determined by the FNOSC<2:0> bits in the FOSCSEL Configuration register. The value of the FNOSC<2:0> bits is loaded into NOSC<2:0> (OSCCON<10:8>) on Reset, which in turn, initializes the system clock.



In addition, DMA transfers can be triggered by timers as well as external interrupts. Each DMA channel is unidirectional. Two DMA channels must be allocated to read and write to a peripheral. If more than one channel receives a request to transfer data, a simple fixed priority scheme based on channel number, dictates which channel completes the transfer and which channel, or channels, are left pending. Each DMA channel moves a block of data, after which, it generates an interrupt to the CPU to indicate that the block is available for processing.

The DMA Controller provides these functional capabilities:

- Four DMA channels
- Register Indirect with Post-Increment Addressing mode
- Register Indirect without Post-Increment Addressing mode

- Peripheral Indirect Addressing mode (peripheral generates destination address)
- CPU interrupt after half or full block transfer complete
- Byte or word transfers
- · Fixed priority channel arbitration
- Manual (software) or automatic (peripheral DMA requests) transfer initiation
- One-Shot or Auto-Repeat Block Transfer modes
- Ping-Pong mode (automatic switch between two SRAM start addresses after each block transfer is complete)
- DMA request for each channel can be selected from any supported interrupt source
- Debug support features

The peripherals that can utilize DMA are listed in Table 8-1.

Peripheral to DMA Association	DMAxREQ Register IRQSEL<7:0> Bits	DMAxPAD Register (Values to Read from Peripheral)	DMAxPAD Register (Values to Write to Peripheral)	
INT0 – External Interrupt 0	00000000	—	—	
IC1 – Input Capture 1	0000001	0x0144 (IC1BUF)	—	
IC2 – Input Capture 2	00000101	0x014C (IC2BUF)	_	
IC3 – Input Capture 3	00100101	0x0154 (IC3BUF)	—	
IC4 – Input Capture 4	00100110	0x015C (IC4BUF)	—	
OC1 – Output Compare 1	00000010	_	0x0906 (OC1R) 0x0904 (OC1RS)	
OC2 – Output Compare 2	00000110	_	0x0910 (OC2R) 0x090E (OC2RS)	
OC3 – Output Compare 3	00011001	_	0x091A (OC3R) 0x0918 (OC3RS)	
OC4 – Output Compare 4	00011010	_	0x0924 (OC4R) 0x0922 (OC4RS)	
TMR2 – Timer2	00000111	—	—	
TMR3 – Timer3	00001000	-	—	
TMR4 – Timer4	00011011	_	—	
TMR5 – Timer5	00011100	—	—	
SPI1 Transfer Done	00001010	0x0248 (SPI1BUF)	0x0248 (SPI1BUF)	
SPI2 Transfer Done	00100001	0x0268 (SPI2BUF)	0x0268 (SPI2BUF)	
UART1RX – UART1 Receiver	00001011	0x0226 (U1RXREG)	—	
UART1TX – UART1 Transmitter	00001100	—	0x0224 (U1TXREG)	
UART2RX – UART2 Receiver	00011110	0x0236 (U2RXREG)	—	
UART2TX – UART2 Transmitter	00011111	—	0x0234 (U2TXREG)	
ECAN1 – RX Data Ready	00100010	0x0440 (C1RXD)		
ECAN1 – TX Data Request	01000110	—	0x0442 (C1TXD)	
ADC1 – ADC1 Convert Done	00001101	0x0300 (ADC1BUF0)	_	

TABLE 8-1: DMA CHANNEL TO PERIPHERAL ASSOCIATIONS

dsPIC33EPXXXGP50X, dsPIC33EPXXXMC20X/50X AND PIC24EPXXXGP/MC20X

U-0	U-0	U-0	U-0	U-0	R/W-0	R/W-0	R/W-0	
_	—	—	_	—	PWM3MD ⁽¹⁾	PWM2MD ⁽¹⁾	PWM1MD ⁽¹⁾	
bit 15							bit 8	
U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0	
—	—		_		_			
bit 7							bit 0	
Legend:								
R = Readab	ole bit	W = Writable	bit	U = Unimplen	nented bit, read	l as '0'		
-n = Value at POR '1' = Bit is set		'0' = Bit is cleared x = Bit is unknown						
bit 15-11	Unimplemented: Read as '0'							
bit 10	10 PWM3MD: PWM3 Module Disable bit ⁽¹⁾							
	1 = PWM3 mo	odule is disable	ed					
	0 = PWM3 mo	odule is enable	d					
bit 9	PWM2MD: P	WM2 Module D	isable bit ⁽¹⁾					
	1 = PWM2 mo	odule is disable	ed					
	0 = PWM2 mc	odule is enable	d					
bit 8	PWM1MD: P	WM1 Module D	isable bit ⁽¹⁾					
	1 = PWM1 mo	odule is disable	ed					
	0 = PWM1 mo	odule is enable	d					
bit 7-0	Unimplemen	ted: Read as '	0'					

REGISTER 10-5: PMD6: PERIPHERAL MODULE DISABLE CONTROL REGISTER 6

Note 1: This bit is available on dsPIC33EPXXXMC50X/20X and PIC24EPXXXMC20X devices only.

REGISTER 16-1: PTCON: PWMx TIME BASE CONTROL REGISTER (CONTINUED)

bit 6-4	SYNCSRC<2:0>: Synchronous Source Selection bits ⁽¹⁾ 111 = Reserved
	•
	• 100 = Reserved 011 = PTGO17 ⁽²⁾ 010 = PTGO16 ⁽²⁾ 001 = Reserved 000 = SYNCI1 input from PPS
bit 3-0	<pre>SEVTPS<3:0>: PWMx Special Event Trigger Output Postscaler Select bits⁽¹⁾ 1111 = 1:16 Postscaler generates Special Event Trigger on every sixteenth compare match event</pre>
	0001 = 1:2 Postscaler generates Special Event Trigger on every second compare match event 0000 = 1:1 Postscaler generates Special Event Trigger on every compare match event

- **Note 1:** These bits should be changed only when PTEN = 0. In addition, when using the SYNCI1 feature, the user application must program the period register with a value that is slightly larger than the expected period of the external synchronization input signal.
 - 2: See Section 24.0 "Peripheral Trigger Generator (PTG) Module" for information on this selection.

·										
R/W-1	R/W-1	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0			
PENH	PENL	POLH	POLL	PMOD1 ⁽¹⁾	PMOD0 ⁽¹⁾	OVRENH	OVRENL			
bit 15							bit 8			
R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0			
OVRDAT1	OVRDAT0	FLTDAT1	FLTDAT0	CLDAT1	CLDAT0	SWAP	OSYNC			
bit 7							bit 0			
Legend:										
R = Readable	bit	W = Writable	bit	U = Unimplei	mented bit, read	l as '0'				
-n = Value at F	POR	'1' = Bit is set		'0' = Bit is cle	eared	x = Bit is unkr	nown			
bit 15	PENH: PWM	(H Output Pin (Ownership bit							
	1 = PWMx mc	dule controls I	PWMxH pin WMx⊟ pin							
hit 11										
DIL 14	1 = DM/Mx mc	a Output Pin C								
	1 = PWWX IIIC 0 = GPIO model	dule controls P	WMxL pin							
hit 13		H Output Pin I	Polarity bit							
	1 = PWMxH nin is active-low									
	0 = PWMxH pin is active-high									
bit 12	POLL: PWMxL Output Pin Polarity bit									
	1 = PWMxL pin is active-low									
	0 = PWMxL pin is active-high									
bit 11-10	PMOD<1:0>:	PWMx # I/O P	in Mode bits ⁽¹)						
	11 = Reserve	d; do not use								
	10 = PWMx I/O pin pair is in the Push-Pull Output mode									
	01 = PWMx I/O pin pair is in the Redundant Output mode									
hit 9	OVRENH: Override Enable for PWMxH Pin bit									
bit o	1 = OVRDAT<1> controls output on PWMxH pin									
	= PWMx generator controls PWMxH pin									
bit 8	bit 8 OVRENL: Override Enable for PWMxL Pin bit									
	1 = OVRDAT	<0> controls ou	Itput on PWM	xL pin						
	0 = PWMx generator controls PWMxL pin									
bit 7-6	OVRDAT<1:0	>: Data for PW	/MxH, PWMxl	L Pins if Overr	ide is Enabled b	its				
	If OVERENH	= 1, PWMxH is	s driven to the	state specifie	d by OVRDAT<	1>.				
	If OVERENL = 1, PWMxL is driven to the state specified by OVRDAT<0>.									
bit 5-4	FLTDAT<1:0>	Data for PW	MxH and PWI	MxL Pins if FL	TMOD is Enable	ed bits				
	If Fault is activ	ve, PWMxH is	driven to the s	state specified	by FLTDAT<1>					
hit 2 0		VE, FVVIVIXL IS (UY FLIDAISUS.	hita				
DIL 3-2	LUAI <1:0>			IXL PILIS IT ULN						
	If current-limit	is active. PWN	/IxL is driven t	the state sp	ecified by CLDA	T<0>.				
Note 1: The	ese bits should i	not be changed	d after the PW	Mx module is	enabled (PTEN	= 1).				

REGISTER 16-13: IOCONx: PWMx I/O CONTROL REGISTER⁽²⁾

2: If the PWMLOCK Configuration bit (FOSCSEL<6>) is a '1', the IOCONx register can only be written after the unlock sequence has been executed.

17.2 QEI Control Registers

|--|

R/W-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0			
QEIEN		QEISIDL	PIMOD2 ⁽¹⁾	PIMOD1 ⁽¹⁾	PIMOD0 ⁽¹⁾	IMV1 ⁽²⁾	IMV0 ⁽²⁾			
bit 15							bit 8			
U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0			
_	INTDIV2 ⁽³⁾	INTDIV1 ⁽³⁾	INTDIV0 ⁽³⁾	CNTPOL	GATEN	CCM1	CCM0			
bit 7							bit 0			
Legend:										
R = Readable	bit	W = Writable	bit	U = Unimpler	nented bit, read	l as '0'				
-n = Value at I	POR	'1' = Bit is set		'0' = Bit is cle	ared	x = Bit is unkr	Iown			
bit 15 QEIEN: Quadrature Encoder Interface Module Counter Enable bit 1 = Module counters are enabled 0 = Module counters are disabled, but SFRs can be read or written to										
bit 14	Unimplemented: Read as '0'									
bit 13	QEISIDL: QEI Stop in Idle Mode bit									
	 1 = Discontinues module operation when device enters Idle mode 0 = Continues module operation in Idle mode 									
bit 12-10	PIMOD<2:0>	: Position Coun	iter Initializatio	n Mode Selec	t bits ⁽¹⁾					
111 = Reserved 110 = Modulo Count mode for position counter 101 = Resets the position counter when the position counter equals QEI1GEC register 100 = Second index event after home event initializes position counter with contents of QEI1IC register 011 = First index event after home event initializes position counter with contents of QEI1IC register 010 = Next index input event initializes the position counter with contents of QEI1IC register 010 = Every index input event resets the position counter 000 = Index input event does not affect position counter										
bit 9	IMV1: Index Match Value for Phase B bit ⁽²⁾									
	1 = Phase B match occurs when QEB = 1 0 = Phase B match occurs when QEB = 0									
bit 8	IMV0: Index N	Match Value for	Phase A bit ⁽²⁾)						
	1 = Phase A r 0 = Phase A r	match occurs w match occurs w	/hen QEA = 1 /hen QEA = 0							
bit 7	Unimplemen	ted: Read as 'o	י)							
	0014.4.0		(II) OF							

Note 1: When CCM<1:0> = 10 or 11, all of the QEI counters operate as timers and the PIMOD<2:0> bits are ignored.

2: When CCM<1:0> = 00, and QEA and QEB values match the Index Match Value (IMV), the POSCNTH and POSCNTL registers are reset. QEA/QEB signals used for the index match have swap and polarity values applied, as determined by the SWPAB and QEAPOL/QEBPOL bits.

3: The selected clock rate should be at least twice the expected maximum quadrature count rate.

REGISTER 17-4: POSICNTH: POSITION COUNTER 1 HIGH WORD REGISTER

-n = Value at POR '1' = Bit is set			'0' = Bit is cleared x = Bit is unknown				
R = Readable bit W = Writable bit			bit	U = Unimpler	mented bit, rea	d as '0'	
Legend:							
bit 7							bit 0
			POSCN	IT<23:16>			
R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
bit 15							bit 8
			POSCN	IT<31:24>			
R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0

bit 15-0 **POSCNT<31:16>:** High Word Used to Form 32-Bit Position Counter Register (POS1CNT) bits

REGISTER 17-5: POS1CNTL: POSITION COUNTER 1 LOW WORD REGISTER

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
			POSCN	T<15:8>			
bit 15							bit 8

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	
POSCNT<7:0>								
bit 7							bit 0	

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read	as '0'
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15-0 POSCNT<15:0>: Low Word Used to Form 32-Bit Position Counter Register (POS1CNT) bits

REGISTER 17-6: POS1HLD: POSITION COUNTER 1 HOLD REGISTER

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
			POSH	LD<15:8>			
bit 15							bit 8
R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
			POSH	ILD<7:0>			
bit 7							bit 0
Legend:							
R = Readable bit W = Writable bit U = Unimplemented bit, read as '0'			d as '0'				
-n = Value at POR '1' = Bit is set '0' = Bit is cleared x = Bit is r				x = Bit is unkr	nown		

bit 15-0 **POSHLD<15:0>:** Hold Register for Reading and Writing POS1CNTH bits

18.3 SPIx Control Registers

R/W-0 U-0 R/W-0 U-0 R/W-0 R/W-0 R/W-0 U-0 SPIEN SPISIDL SPIBEC<2:0> _____ bit 15 R/W-0 R/W-0 R/W-0 R/C-0, HS R/W-0 R/W-0 R-0, HS, HC R-0, HS, HC SRMPT SPIROV SRXMPT SISEL2 SISEL1 SISEL0 SPITBF SPIRBF bit 7 bit 0 Legend: C = Clearable bit HS = Hardware Settable bit HC = Hardware Clearable bit R = Readable bit W = Writable bit U = Unimplemented bit, read as '0' -n = Value at POR '1' = Bit is set '0' = Bit is cleared x = Bit is unknown bit 15 SPIEN: SPIx Enable bit 1 = Enables the module and configures SCKx, SDOx, SDIx and \overline{SSx} as serial port pins 0 = Disables the module bit 14 Unimplemented: Read as '0' bit 13 SPISIDL: SPIx Stop in Idle Mode bit 1 = Discontinues the module operation when device enters Idle mode 0 = Continues the module operation in Idle mode bit 12-11 Unimplemented: Read as '0' bit 10-8 SPIBEC<2:0>: SPIx Buffer Element Count bits (valid in Enhanced Buffer mode) Master mode: Number of SPIx transfers that are pending. Slave mode: Number of SPIx transfers that are unread. **SRMPT:** SPIx Shift Register (SPIxSR) Empty bit (valid in Enhanced Buffer mode) bit 7 1 = SPIx Shift register is empty and Ready-To-Send or receive the data 0 = SPIx Shift register is not empty bit 6 SPIROV: SPIx Receive Overflow Flag bit

REGISTER 18-1: SPIxSTAT: SPIx STATUS AND CONTROL REGISTER

1 = A new byte/word is completely received and discarded; the user application has not read the previous data in the SPIxBUF register 0 = No overflow has occurred SRXMPT: SPIx Receive FIFO Empty bit (valid in Enhanced Buffer mode) bit 5 1 = RX FIFO is empty 0 = RX FIFO is not empty bit 4-2 SISEL<2:0>: SPIx Buffer Interrupt Mode bits (valid in Enhanced Buffer mode) 111 = Interrupt when the SPIx transmit buffer is full (SPITBF bit is set) 110 = Interrupt when last bit is shifted into SPIxSR and as a result, the TX FIFO is empty 101 = Interrupt when the last bit is shifted out of SPIxSR and the transmit is complete 100 = Interrupt when one data is shifted into the SPIxSR and as a result, the TX FIFO has one open memory location 011 = Interrupt when the SPIx receive buffer is full (SPIRBF bit is set) 010 = Interrupt when the SPIx receive buffer is 3/4 or more full 001 = Interrupt when data is available in the receive buffer (SRMPT bit is set) 000 = Interrupt when the last data in the receive buffer is read and as a result, the buffer is empty

bit 8

U-0	U-0	U-0	U-0	U-0	U-0	R/W-0	R/W-0
—	—	—	—		—	AMSK9	AMSK8
bit 15							bit 8
R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
AMSK7	AMSK6	AMSK5	AMSK4	AMSK3	AMSK2	AMSK1	AMSK0
bit 7							bit 0

REGISTER 19-3: I2CxMSK: I2Cx SLAVE MODE ADDRESS MASK REGISTER

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit	, read as '0'
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15-10 Unimplemented: Read as '0'

bit 9-0

AMSK<9:0>: Address Mask Select bits

For 10-Bit Address:

1 = Enables masking for bit Ax of incoming message address; bit match is not required in this position

0 = Disables masking for bit Ax; bit match is required in this position

For 7-Bit Address (I2CxMSK<6:0> only):

1 = Enables masking for bit Ax + 1 of incoming message address; bit match is not required in this position

0 = Disables masking for bit Ax + 1; bit match is required in this position

20.0 UNIVERSAL ASYNCHRONOUS RECEIVER TRANSMITTER (UART)

- Note 1: This data sheet summarizes the features of the dsPIC33EPXXXGP50X, dsPIC33EPXXXMC20X/50X and PIC24EPXXXGP/MC20X families of devices. It is not intended to be a comprehensive reference source. To complement the information in this data sheet, refer to "UART" (DS70582) in the "dsPIC33/ PIC24 Family Reference Manual", which is available from the Microchip web site (www.microchip.com).
 - 2: Some registers and associated bits described in this section may not be available on all devices. Refer to Section 4.0 "Memory Organization" in this data sheet for device-specific register and bit information.

The dsPIC33EPXXXGP50X, dsPIC33EPXXXMC20X/ 50X and PIC24EPXXXGP/MC20X family of devices contains two UART modules.

The Universal Asynchronous Receiver Transmitter (UART) module is one of the serial I/O modules available in the dsPIC33EPXXXGP50X, dsPIC33EPXXXMC20X/ 50X and PIC24EPXXXGP/MC20X device family. The UART is a full-duplex, asynchronous system that can communicate with peripheral devices, such as personal computers, LIN/J2602, RS-232 and RS-485 interfaces. The module also supports a hardware flow control option with the UxCTS and UxRTS pins, and also includes an IrDA[®] encoder and decoder.

Note: <u>Hardware</u> flow control using UxRTS and UxCTS is not available on all pin count devices. See the "**Pin Diagrams**" section for availability.

The primary features of the UARTx module are:

- Full-Duplex, 8 or 9-Bit Data Transmission through the UxTX and UxRX Pins
- Even, Odd or No Parity Options (for 8-bit data)
- One or Two Stop bits
- Hardware Flow Control Option with UxCTS and UxRTS Pins
- Fully Integrated Baud Rate Generator with 16-Bit Prescaler
- Baud Rates Ranging from 4.375 Mbps to 67 bps at 16x mode at 70 MIPS
- Baud Rates Ranging from 17.5 Mbps to 267 bps at 4x mode at 70 MIPS
- 4-Deep First-In First-Out (FIFO) Transmit Data Buffer
- 4-Deep FIFO Receive Data Buffer
- Parity, Framing and Buffer Overrun Error Detection
- Support for 9-bit mode with Address Detect (9th bit = 1)
- · Transmit and Receive Interrupts
- A Separate Interrupt for all UARTx Error Conditions
- · Loopback mode for Diagnostic Support
- · Support for Sync and Break Characters
- Support for Automatic Baud Rate Detection
- IrDA[®] Encoder and Decoder Logic
- 16x Baud Clock Output for IrDA Support

A simplified block diagram of the UARTx module is shown in Figure 20-1. The UARTx module consists of these key hardware elements:

- · Baud Rate Generator
- Asynchronous Transmitter
- Asynchronous Receiver

FIGURE 20-1: UARTx SIMPLIFIED BLOCK DIAGRAM



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REGISTER 23-6: AD1CHS0: ADC1 INPUT CHANNEL 0 SELECT REGISTER (CONTINUED)

bit 4-0	CH0SA<4:0>: Channel 0 Positive Input Select for Sample MUXA bits ⁽¹⁾
	11111 = Open; use this selection with CTMU capacitive and time measurement
	11110 = Channel 0 positive input is connected to the CTMU temperature measurement diode (CTMU TEMP)
	11101 - Reserved
	11011 = Reserved
	11010 = Channel 0 positive input is the output of OA3/AN6 ^(2,3)
	11001 = Channel 0 positive input is the output of OA2/AN0 ⁽²⁾
	11000 = Channel 0 positive input is the output of OA1/AN3 ⁽⁻⁾
	•
	•
	•
	10000 = Reserved
	01111 = Channel 0 positive input is AN15 ^(1,3)
	01110 = Channel 0 positive input is AN14 ^(1,3)
	01101 = Channel 0 positive input is AN13 ^(1,3)
	•
	•
	• (1 2)
	00010 = Channel 0 positive input is AN2 ^(1,3)
	00001 = Channel 0 positive input is AN1(1,3)
	00000 = Channel 0 positive input is AN0(',3)

- **Note 1:** AN0 through AN7 are repurposed when comparator and op amp functionality is enabled. See Figure 23-1 to determine how enabling a particular op amp or comparator affects selection choices for Channels 1, 2 and 3.
 - 2: The OAx input is used if the corresponding op amp is selected (OPMODE (CMxCON<10>) = 1); otherwise, the ANx input is used.
 - 3: See the "Pin Diagrams" section for the available analog channels for each device.

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
CSS15	CSS14	CSS13	CSS12	CSS11	CSS10	CSS9	CSS8
bit 15							bit 8
R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
CSS7	CSS6	CSS5	CSS4	CSS3	CSS2	CSS1	CSS0
bit 7	·					•	bit 0
Legend:							
R = Readable bit W = Writable bit U = Unimplemented bit, read as '0'							
-n = Value at POR '1' = Bit is set '0' = Bit is cleared x = Bit is unkno					nown		

REGISTER 23-8: AD1CSSL: ADC1 INPUT SCAN SELECT REGISTER LOW^(1,2)

bit 15-0 CSS<15:0>: ADC1 Input Scan Selection bits

1 = Selects ANx for input scan

0 = Skips ANx for input scan

Note 1: On devices with less than 16 analog inputs, all AD1CSSL bits can be selected by the user. However, inputs selected for scan, without a corresponding input on the device, convert VREFL.

2: CSSx = ANx, where x = 0-15.

30.0 ELECTRICAL CHARACTERISTICS

This section provides an overview of dsPIC33EPXXXGP50X, dsPIC33EPXXXMC20X/50X and PIC24EPXXXGP/ MC20X electrical characteristics. Additional information will be provided in future revisions of this document as it becomes available.

Absolute maximum ratings for the dsPIC33EPXXXGP50X, dsPIC33EPXXXMC20X/50X and PIC24EPXXXGP/MC20X family are listed below. Exposure to these maximum rating conditions for extended periods may affect device reliability. Functional operation of the device at these or any other conditions above the parameters indicated in the operation listings of this specification is not implied.

Absolute Maximum Ratings⁽¹⁾

Ambient temperature under bias	40°C to +125°C
Storage temperature	65°C to +150°C
Voltage on VDD with respect to Vss	-0.3V to +4.0V
Voltage on any pin that is not 5V tolerant, with respect to Vss ⁽³⁾	0.3V to (VDD + 0.3V)
Voltage on any 5V tolerant pin with respect to Vss when $VDD \ge 3.0V^{(3)}$	0.3V to +5.5V
Voltage on any 5V tolerant pin with respect to Vss when $VDD < 3.0V^{(3)}$	-0.3V to +3.6V
Maximum current out of Vss pin	
Maximum current into VDD pin ⁽²⁾	
Maximum current sunk/sourced by any 4x I/O pin	
Maximum current sunk/sourced by any 8x I/O pin	25 mA
Maximum current sunk by all ports ^(2,4)	200 mA

- **Note 1:** Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only, and functional operation of the device at those or any other conditions above those indicated in the operation listings of this specification is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.
 - 2: Maximum allowable current is a function of device maximum power dissipation (see Table 30-2).
 - 3: See the "Pin Diagrams" section for the 5V tolerant pins.
 - 4: Exceptions are: dsPIC33EPXXXGP502, dsPIC33EPXXXMC202/502 and PIC24EPXXXGP/MC202 devices, which have a maximum sink/source capability of 130 mA.

TABLE 30-38:SPI2 SLAVE MODE (FULL-DUPLEX, CKE = 1, CKP = 1, SMP = 0)TIMING REQUIREMENTS

AC CHARACTERISTICS			Standard Operating Conditions: 3.0V to 3.6V (unless otherwise stated) Operating temperature $-40^{\circ}C \le TA \le +85^{\circ}C$ for Industrial $-40^{\circ}C \le TA \le +125^{\circ}C$ for Extended				
Param.	Symbol	Characteristic ⁽¹⁾	Min.	Typ. ⁽²⁾	Max.	Units	Conditions
SP70	FscP	Maximum SCK2 Input Frequency	_		Lesser of FP or 11	MHz	(Note 3)
SP72	TscF	SCK2 Input Fall Time	—	_	_	ns	See Parameter DO32 (Note 4)
SP73	TscR	SCK2 Input Rise Time	—	_	_	ns	See Parameter DO31 (Note 4)
SP30	TdoF	SDO2 Data Output Fall Time	—			ns	See Parameter DO32 (Note 4)
SP31	TdoR	SDO2 Data Output Rise Time	—			ns	See Parameter DO31 (Note 4)
SP35	TscH2doV, TscL2doV	SDO2 Data Output Valid after SCK2 Edge	—	6	20	ns	
SP36	TdoV2scH, TdoV2scL	SDO2 Data Output Setup to First SCK2 Edge	30			ns	
SP40	TdiV2scH, TdiV2scL	Setup Time of SDI2 Data Input to SCK2 Edge	30			ns	
SP41	TscH2diL, TscL2diL	Hold Time of SDI2 Data Input to SCK2 Edge	30			ns	
SP50	TssL2scH, TssL2scL	SS2 ↓ to SCK2 ↑ or SCK2 ↓ Input	120			ns	
SP51	TssH2doZ	SS2 ↑ to SDO2 Output High-Impedance	10	_	50	ns	(Note 4)
SP52	TscH2ssH TscL2ssH	SS2 ↑ after SCK2 Edge	1.5 TCY + 40	_	_	ns	(Note 4)
SP60	TssL2doV	SDO2 Data Output Valid after SS2 Edge	—	-	50	ns	

Note 1: These parameters are characterized, but are not tested in manufacturing.

2: Data in "Typical" column is at 3.3V, +25°C unless otherwise stated.

3: The minimum clock period for SCK2 is 91 ns. Therefore, the SCK2 clock generated by the master must not violate this specification.

4: Assumes 50 pF load on all SPI2 pins.



FIGURE 30-26: SPI1 SLAVE MODE (FULL-DUPLEX, CKE = 1, CKP = 0, SMP = 0) TIMING CHARACTERISTICS

DC CHARACTERISTICS			Standard Operating Conditions: 3.0V to 3.6V(unless otherwise stated)Operating temperature $-40^{\circ}C \le TA \le +150^{\circ}C$				
Param.	Symbol	Characteristic	Characteristic Min. Typ. Max. Units				
HDO10 Vol		Output Low Voltage 4x Sink Driver Pins ⁽²⁾	_	—	0.4	V	IOL ≤ 5 mA, VDD = 3.3V (Note 1)
		Output Low Voltage 8x Sink Driver Pins ⁽³⁾	—	_	0.4	V	IOL ≤ 8 mA, VDD = 3.3V (Note 1)
HDO20	Vон	Output High Voltage 4x Source Driver Pins ⁽²⁾	2.4	—		V	IOH ≥ -10 mA, VDD = 3.3V (Note 1)
		Output High Voltage 8x Source Driver Pins ⁽³⁾	2.4	—		V	IOH ≥ 15 mA, VDD = 3.3V (Note 1)
HDO20A Voh1		Output High Voltage 4x Source Driver Pins ⁽²⁾	1.5	—	_	V	IOH ≥ -3.9 mA, VDD = 3.3V (Note 1)
			2.0	—			IOH ≥ -3.7 mA, VDD = 3.3V (Note 1)
			3.0	—			IOH ≥ -2 mA, VDD = 3.3V (Note 1)
		Output High Voltage 8x Source Driver Pins ⁽³⁾	1.5	_		V	IOH ≥ -7.5 mA, VDD = 3.3V (Note 1)
			2.0	_			IOH ≥ -6.8 mA, VDD = 3.3V (Note 1)
			3.0	—	_		IOH ≥ -3 mA, VDD = 3.3V (Note 1)

TABLE 31-8: DC CHARACTERISTICS: I/O PIN OUTPUT SPECIFICATIONS

Note 1: Parameters are characterized, but not tested.

2: Includes all I/O pins that are not 8x Sink Driver pins (see below).

Includes the following pins:
 For devices with less than 64 pins: RA3, RA4, RA9, RB<15:7> and RC3
 For 64-pin devices: RA4, RA9, RB<15:7>, RC3 and RC15