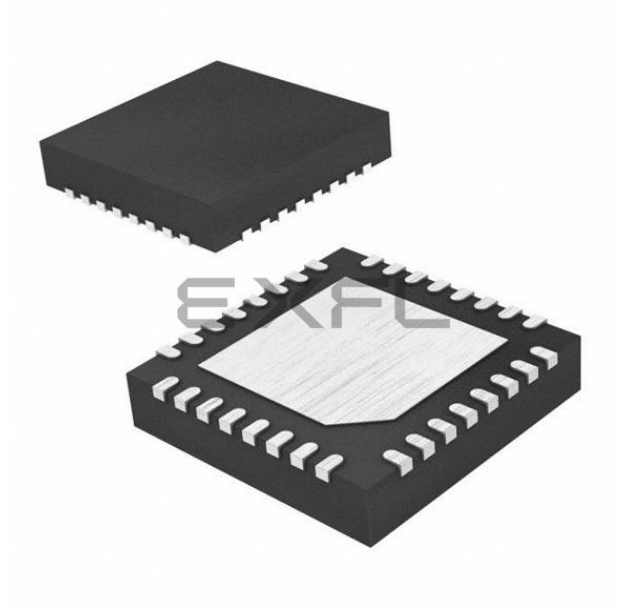

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Details	
Product Status	Active
Core Processor	PIC
Core Size	16-Bit
Speed	60 MIPs
Connectivity	I²C, IrDA, LINbus, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, DMA, POR, PWM, WDT
Number of I/O	21
Program Memory Size	512KB (170K x 24)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	24K x 16
Voltage - Supply (Vcc/Vdd)	3V ~ 3.6V
Data Converters	A/D 6x10b/12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 125°C (TA)
Mounting Type	Surface Mount
Package / Case	28-VQFN Exposed Pad
Supplier Device Package	28-QFN-S (6x6)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/pic24ep512gp202-e-mm

TABLE 1-1: PINOUT I/O DESCRIPTIONS (CONTINUED)

Pin Name(4)	Pin Type	Buffer Type	PPS	Description
U2CTS	I	ST	No	UART2 Clear-To-Send.
U2RTS	O	—	No	UART2 Ready-To-Send.
U2RX	I	ST	Yes	UART2 receive.
U2TX	O	—	Yes	UART2 transmit.
BCLK2	O	ST	No	UART2 IrDA® baud clock output.
SCK1	I/O	ST	No	Synchronous serial clock input/output for SPI1.
SDI1	I	ST	No	SPI1 data in.
SDO1	O	—	No	SPI1 data out.
SS1	I/O	ST	No	SPI1 slave synchronization or frame pulse I/O.
SCK2	I/O	ST	Yes	Synchronous serial clock input/output for SPI2.
SDI2	I	ST	Yes	SPI2 data in.
SDO2	O	—	Yes	SPI2 data out.
SS2	I/O	ST	Yes	SPI2 slave synchronization or frame pulse I/O.
SCL1	I/O	ST	No	Synchronous serial clock input/output for I2C1.
SDA1	I/O	ST	No	Synchronous serial data input/output for I2C1.
ASCL1	I/O	ST	No	Alternate synchronous serial clock input/output for I2C1.
ASDA1	I/O	ST	No	Alternate synchronous serial data input/output for I2C1.
SCL2	I/O	ST	No	Synchronous serial clock input/output for I2C2.
SDA2	I/O	ST	No	Synchronous serial data input/output for I2C2.
ASCL2	I/O	ST	No	Alternate synchronous serial clock input/output for I2C2.
ASDA2	I/O	ST	No	Alternate synchronous serial data input/output for I2C2.
TMS(5)	I	ST	No	JTAG Test mode select pin.
TCK	I	ST	No	JTAG test clock input pin.
TDI	I	ST	No	JTAG test data input pin.
TDO	O	—	No	JTAG test data output pin.
C1RX(2)	I	ST	Yes	ECAN1 bus receive pin.
C1TX(2)	O	—	Yes	ECAN1 bus transmit pin.
FLT1(1), FLT2(1)	I	ST	Yes	PWM Fault Inputs 1 and 2.
FLT3(1), FLT4(1)	I	ST	No	PWM Fault Inputs 3 and 4.
FLT32(1,3)	I	ST	No	PWM Fault Input 32 (Class B Fault).
DTCMP1-DTCMP3(1)	I	ST	Yes	PWM Dead-Time Compensation Inputs 1 through 3.
PWM1L-PWM3L(1)	O	—	No	PWM Low Outputs 1 through 3.
PWM1H-PWM3H(1)	O	—	No	PWM High Outputs 1 through 3.
SYNCI1(1)	I	ST	Yes	PWM Synchronization Input 1.
SYNCO1(1)	O	—	Yes	PWM Synchronization Output 1.
INDX1(1)	I	ST	Yes	Quadrature Encoder Index1 pulse input.
HOME1(1)	I	ST	Yes	Quadrature Encoder Home1 pulse input.
QEA1(1)	I	ST	Yes	Quadrature Encoder Phase A input in QEI1 mode. Auxiliary timer external clock/gate input in Timer mode.
QEB1(1)	I	ST	Yes	Quadrature Encoder Phase B input in QEI1 mode. Auxiliary timer external clock/gate input in Timer mode.
CNTCMP1(1)	O	—	Yes	Quadrature Encoder Compare Output 1.

Legend: CMOS = CMOS compatible input or output; Analog = Analog input; P = Power
ST = Schmitt Trigger input with CMOS levels; O = Output; I = Input
PPS = Peripheral Pin Select; TTL = TTL input buffer

Note 1: This pin is available on dsPIC33EPXXXMC20X/50X and PIC24EPXXXMC20X devices only.

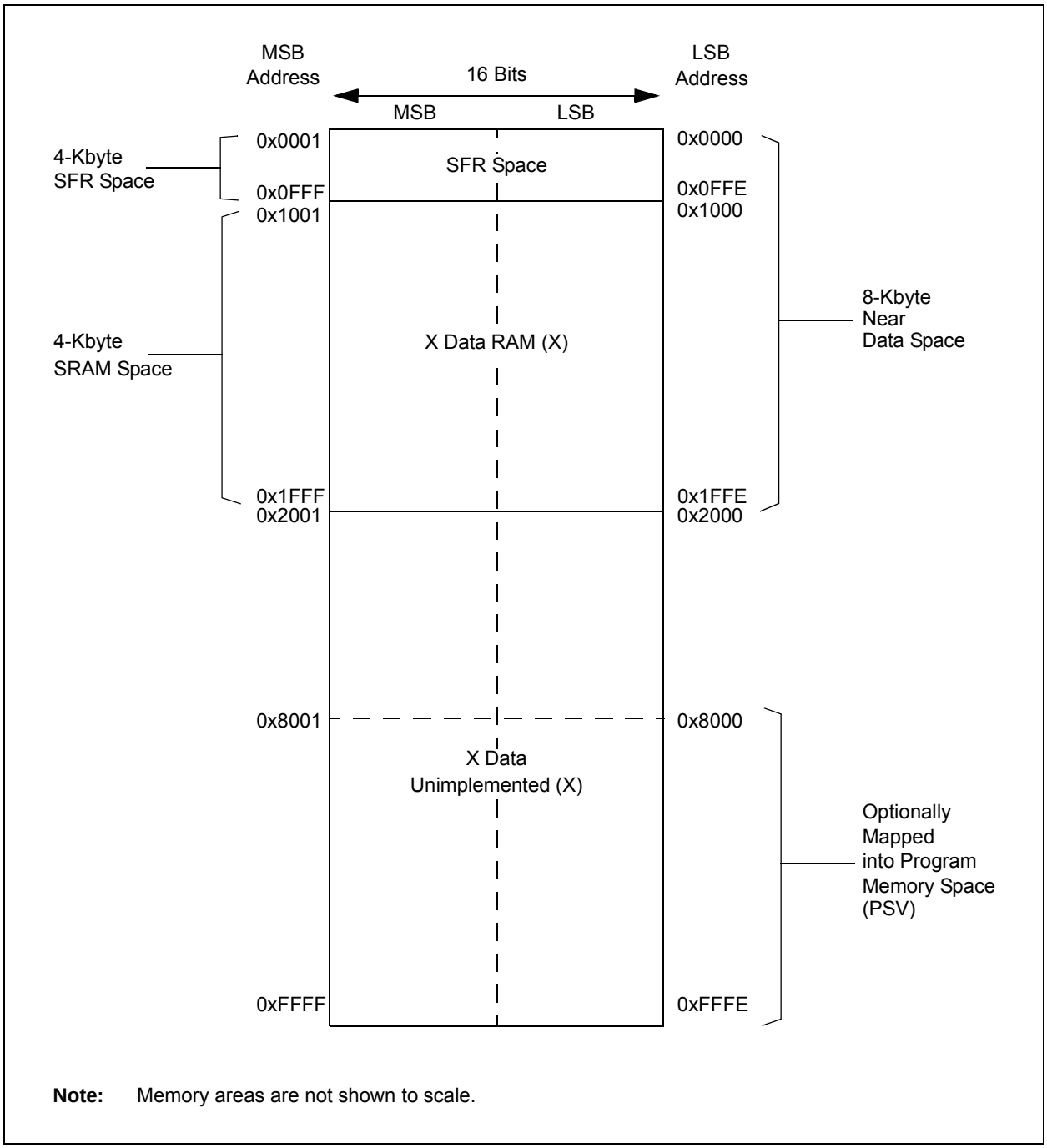
2: This pin is available on dsPIC33EPXXXGP/MC50X devices only.

3: This is the default Fault on Reset for dsPIC33EPXXXMC20X/50X and PIC24EPXXXMC20X devices. See **Section 16.0 "High-Speed PWM Module (dsPIC33EPXXXMC20X/50X and PIC24EPXXXMC20X Devices Only)"** for more information.

4: Not all pins are available in all packages variants. See the **"Pin Diagrams"** section for pin availability.

5: There is an internal pull-up resistor connected to the TMS pin when the JTAG interface is active. See the JTAGEN bit field in Table 27-2.

FIGURE 4-12: DATA MEMORY MAP FOR PIC24EP32GP/MC20X/50X DEVICES



Note: Memory areas are not shown to scale.

TABLE 4-9: INPUT CAPTURE 1 THROUGH INPUT CAPTURE 4 REGISTER MAP

File Name	Addr.	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	All Resets
IC1CON1	0140	—	—	ICSIDL	ICTSEL<2:0>			—	—	—	ICI<1:0>		ICOV	ICBNE	ICM<2:0>			0000
IC1CON2	0142	—	—	—	—	—	—	—	IC32	ICTRIG	TRIGSTAT	—	SYNCSEL<4:0>					000D
IC1BUF	0144	Input Capture 1 Buffer Register																xxxx
IC1TMR	0146	Input Capture 1 Timer																0000
IC2CON1	0148	—	—	ICSIDL	ICTSEL<2:0>			—	—	—	ICI<1:0>		ICOV	ICBNE	ICM<2:0>			0000
IC2CON2	014A	—	—	—	—	—	—	—	IC32	ICTRIG	TRIGSTAT	—	SYNCSEL<4:0>					000D
IC2BUF	014C	Input Capture 2 Buffer Register																xxxx
IC2TMR	014E	Input Capture 2 Timer																0000
IC3CON1	0150	—	—	ICSIDL	ICTSEL<2:0>			—	—	—	ICI<1:0>		ICOV	ICBNE	ICM<2:0>			0000
IC3CON2	0152	—	—	—	—	—	—	—	IC32	ICTRIG	TRIGSTAT	—	SYNCSEL<4:0>					000D
IC3BUF	0154	Input Capture 3 Buffer Register																xxxx
IC3TMR	0156	Input Capture 3 Timer																0000
IC4CON1	0158	—	—	ICSIDL	ICTSEL<2:0>			—	—	—	ICI<1:0>		ICOV	ICBNE	ICM<2:0>			0000
IC4CON2	015A	—	—	—	—	—	—	—	IC32	ICTRIG	TRIGSTAT	—	SYNCSEL<4:0>					000D
IC4BUF	015C	Input Capture 4 Buffer Register																xxxx
IC4TMR	015E	Input Capture 4 Timer																0000

Legend: x = unknown value on Reset, — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

TABLE 4-46: PORTA REGISTER MAP FOR PIC24EPXXXGP/MC206 AND dsPIC33EPXXXGP/MC206/506 DEVICES ONLY

File Name	Addr.	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	All Resets
TRISA	0E00	—	—	—	TRISA12	TRISA11	TRISA10	TRISA9	TRISA8	TRISA7	—	—	TRISA4	—	—	TRISA1	TRISA0	1F93
PORTA	0E02	—	—	—	RA12	RA11	RA10	RA9	RA8	RA7	—	—	RA4	—	—	RA1	RA0	0000
LATA	0E04	—	—	—	LATA12	LATA11	LATA10	LATA9	LATA8	LATA7	—	—	LATA4	—	—	LA1TA1	LA0TA0	0000
ODCA	0E06	—	—	—	ODCA12	ODCA11	ODCA10	ODCA9	ODCA8	ODCA7	—	—	ODCA4	—	—	ODCA1	ODCA0	0000
CNENA	0E08	—	—	—	CNIEA12	CNIEA11	CNIEA10	CNIEA9	CNIEA8	CNIEA7	—	—	CNIEA4	—	—	CNIEA1	CNIEA0	0000
CNPUA	0E0A	—	—	—	CNPUA12	CNPUA11	CNPUA10	CNPUA9	CNPUA8	CNPUA7	—	—	CNPUA4	—	—	CNPUA1	CNPUA0	0000
CNPDA	0E0C	—	—	—	CNPDA12	CNPDA11	CNPDA10	CNPDA9	CNPDA8	CNPDA7	—	—	CNPDA4	—	—	CNPDA1	CNPDA0	0000
ANSELA	0E0E	—	—	—	ANSA12	ANSA11	—	—	—	—	—	—	ANSA4	—	—	ANSA1	ANSA0	1813

Legend: — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

TABLE 4-47: PORTB REGISTER MAP FOR PIC24EPXXXGP/MC206 AND dsPIC33EPXXXGP/MC206/506 DEVICES ONLY

File Name	Addr.	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	All Resets
TRISB	0E10	TRISB15	TRISB14	TRISB13	TRISB12	TRISB11	TRISB10	TRISB9	TRISB8	TRISB7	TRISB6	TRISB5	TRISB4	TRISB3	TRISB2	TRISB1	TRISB0	FFFF
PORTB	0E12	RB15	RB14	RB13	RB12	RB11	RB10	RB9	RB8	RB7	RB6	RB5	RB4	RB3	RB2	RB1	RB0	xxxx
LATB	0E14	LATB15	LATB14	LATB13	LATB12	LATB11	LATB10	LATB9	LATB8	LATB7	LATB6	LATB5	LATB4	LATB3	LATB2	LATB1	LATB0	xxxx
ODCB	0E16	ODCB15	ODCB14	ODCB13	ODCB12	ODCB11	ODCB10	ODCB9	ODCB8	ODCB7	ODCB6	ODCB5	ODCB4	ODCB3	ODCB2	ODCB1	ODCB0	0000
CNENB	0E18	CNIEB15	CNIEB14	CNIEB13	CNIEB12	CNIEB11	CNIEB10	CNIEB9	CNIEB8	CNIEB7	CNIEB6	CNIEB5	CNIEB4	CNIEB3	CNIEB2	CNIEB1	CNIEB0	0000
CNPUB	0E1A	CNPUB15	CNPUB14	CNPUB13	CNPUB12	CNPUB11	CNPUB10	CNPUB9	CNPUB8	CNPUB7	CNPUB6	CNPUB5	CNPUB4	CNPUB3	CNPUB2	CNPUB1	CNPUB0	0000
CNPDB	0E1C	CNPDB15	CNPDB14	CNPDB13	CNPDB12	CNPDB11	CNPDB10	CNPDB9	CNPDB8	CNPDB7	CNPDB6	CNPDB5	CNPDB4	CNPDB3	CNPDB2	CNPDB1	CNPDB0	0000
ANSELB	0E1E	—	—	—	—	—	—	—	ANSB8	—	—	—	—	ANSB3	ANSB2	ANSB1	ANSB0	010F

Legend: x = unknown value on Reset, — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

TABLE 4-48: PORTC REGISTER MAP FOR PIC24EPXXXGP/MC206 AND dsPIC33EPXXXGP/MC206/506 DEVICES ONLY

File Name	Addr.	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	All Resets
TRISC	0E20	TRISC15	—	TRISC13	TRISC12	TRISC11	TRISC10	TRISC9	TRISC8	TRISC7	TRISC6	TRISC5	TRISC4	TRISC3	TRISC2	TRISC1	TRISC0	BFFF
PORTC	0E22	RC15	—	RC13	RC12	RC11	RC10	RC9	RC8	RC7	RC6	RC5	RC4	RC3	RC2	RC1	RC0	xxxx
LATC	0E24	LATC15	—	LATC13	LATC12	LATC11	LATC10	LATC9	LATC8	LATC7	LATC6	LATC5	LATC4	LATC3	LATC2	LATC1	LATC0	xxxx
ODCC	0E26	ODCC15	—	ODCC13	ODCC12	ODCC11	ODCC10	ODCC9	ODCC8	ODCC7	ODCC6	ODCC5	ODCC4	ODCC3	ODCC2	ODCC1	ODCC0	0000
CNENC	0E28	CNIEC15	—	CNIEC13	CNIEC12	CNIEC11	CNIEC10	CNIEC9	CNIEC8	CNIEC7	CNIEC6	CNIEC5	CNIEC4	CNIEC3	CNIEC2	CNIEC1	CNIEC0	0000
CNPUC	0E2A	CNPUC15	—	CNPUC13	CNPUC12	CNPUC11	CNPUC10	CNPUC9	CNPUC8	CNPUC7	CNPUC6	CNPUC5	CNPUC4	CNPUC3	CNPUC2	CNPUC1	CNPUC0	0000
CNPDC	0E2C	CNPDC15	—	CNPDC13	CNPDC12	CNPDC11	CNPDC10	CNPDC9	CNPDC8	CNPDC7	CNPDC6	CNPDC5	CNPDC4	CNPDC3	CNPDC2	CNPDC1	CNPDC0	0000
ANSELC	0E2E	—	—	—	—	ANSC11	—	—	—	—	—	—	—	—	ANSC2	ANSC1	ANSC0	0807

Legend: x = unknown value on Reset, — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

TABLE 4-53: PORTA REGISTER MAP FOR PIC24EPXXXGP/MC204 AND dsPIC33EPXXXGP/MC204/504 DEVICES ONLY

File Name	Addr.	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	All Resets
TRISA	0E00	—	—	—	—	—	TRISA10	TRISA9	TRISA8	TRISA7	—	—	TRISA4	TRISA3	TRISA2	TRISA1	TRISA0	079F
PORTA	0E02	—	—	—	—	—	RA10	RA9	RA8	RA7	—	—	RA4	RA3	RA2	RA1	RA0	0000
LATA	0E04	—	—	—	—	—	LATA10	LATA9	LATA8	LATA7	—	—	LATA4	LATA3	LATA2	LA1TA1	LA0TA0	0000
ODCA	0E06	—	—	—	—	—	ODCA10	ODCA9	ODCA8	ODCA7	—	—	ODCA4	ODCA3	ODCA2	ODCA1	ODCA0	0000
CNENA	0E08	—	—	—	—	—	CNIEA10	CNIEA9	CNIEA8	CNIEA7	—	—	CNIEA4	CNIEA3	CNIEA2	CNIEA1	CNIEA0	0000
CNPUA	0E0A	—	—	—	—	—	CNPUA10	CNPUA9	CNPUA8	CNPUA7	—	—	CNPUA4	CNPUA3	CNPUA2	CNPUA1	CNPUA0	0000
CNPDA	0E0C	—	—	—	—	—	CNPDA10	CNPDA9	CNPDA8	CNPDA7	—	—	CNPDA4	CNPDA3	CNPDA2	CNPDA1	CNPDA0	0000
ANSELA	0E0E	—	—	—	—	—	—	—	—	—	—	—	ANSA4	—	—	ANSA1	ANSA0	0013

Legend: — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

TABLE 4-54: PORTB REGISTER MAP FOR PIC24EPXXXGP/MC204 AND dsPIC33EPXXXGP/MC204/504 DEVICES ONLY

File Name	Addr.	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	All Resets
TRISB	0E10	TRISB15	TRISB14	TRISB13	TRISB12	TRISB11	TRISB10	TRISB9	TRISB8	TRISB7	TRISB6	TRISB5	TRISB4	TRISB3	TRISB2	TRISB1	TRISB0	FFFF
PORTB	0E12	RB15	RB14	RB13	RB12	RB11	RB10	RB9	RB8	RB7	RB6	RB5	RB4	RB3	RB2	RB1	RB0	xxxx
LATB	0E14	LATB15	LATB14	LATB13	LATB12	LATB11	LATB10	LATB9	LATB8	LATB7	LATB6	LATB5	LATB4	LATB3	LATB2	LATB1	LATB0	xxxx
ODCB	0E16	ODCB15	ODCB14	ODCB13	ODCB12	ODCB11	ODCB10	ODCB9	ODCB8	ODCB7	ODCB6	ODCB5	ODCB4	ODCB3	ODCB2	ODCB1	ODCB0	0000
CNENB	0E18	CNIEB15	CNIEB14	CNIEB13	CNIEB12	CNIEB11	CNIEB10	CNIEB9	CNIEB8	CNIEB7	CNIEB6	CNIEB5	CNIEB4	CNIEB3	CNIEB2	CNIEB1	CNIEB0	0000
CNPUB	0E1A	CNPUB15	CNPUB14	CNPUB13	CNPUB12	CNPUB11	CNPUB10	CNPUB9	CNPUB8	CNPUB7	CNPUB6	CNPUB5	CNPUB4	CNPUB3	CNPUB2	CNPUB1	CNPUB0	0000
CNPDB	0E1C	CNPDB15	CNPDB14	CNPDB13	CNPDB12	CNPDB11	CNPDB10	CNPDB9	CNPDB8	CNPDB7	CNPDB6	CNPDB5	CNPDB4	CNPDB3	CNPDB2	CNPDB1	CNPDB0	0000
ANSELB	0E1E	—	—	—	—	—	—	—	ANSB8	—	—	—	—	ANSB3	ANSB2	ANSB1	ANSB0	010F

Legend: x = unknown value on Reset, — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

TABLE 4-55: PORTC REGISTER MAP FOR PIC24EPXXXGP/MC204 AND dsPIC33EPXXXGP/MC204/504 DEVICES ONLY

File Name	Addr.	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	All Resets
TRISC	0E20	—	—	—	—	—	—	TRISC9	TRISC8	TRISC7	TRISC6	TRISC5	TRISC4	TRISC3	TRISC2	TRISC1	TRISC0	03FF
PORTC	0E22	—	—	—	—	—	—	RC9	RC8	RC7	RC6	RC5	RC4	RC3	RC2	RC1	RC0	xxxx
LATC	0E24	—	—	—	—	—	—	LATC9	LATC8	LATC7	LATC6	LATC5	LATC4	LATC3	LATC2	LATC1	LATC0	xxxx
ODCC	0E26	—	—	—	—	—	—	ODCC9	ODCC8	ODCC7	ODCC6	ODCC5	ODCC4	ODCC3	ODCC2	ODCC1	ODCC0	0000
CNENC	0E28	—	—	—	—	—	—	CNIEC9	CNIEC8	CNIEC7	CNIEC6	CNIEC5	CNIEC4	CNIEC3	CNIEC2	CNIEC1	CNIEC0	0000
CNPUC	0E2A	—	—	—	—	—	—	CNPUC9	CNPUC8	CNPUC7	CNPUC6	CNPUC5	CNPUC4	CNPUC3	CNPUC2	CNPUC1	CNPUC0	0000
CNPDC	0E2C	—	—	—	—	—	—	CNPDC9	CNPDC8	CNPDC7	CNPDC6	CNPDC5	CNPDC4	CNPDC3	CNPDC2	CNPDC1	CNPDC0	0000
ANSELC	0E2E	—	—	—	—	—	—	—	—	—	—	—	—	—	ANSC2	ANSC1	ANSC0	0007

Legend: x = unknown value on Reset, — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

4.4.4 SOFTWARE STACK

The W15 register serves as a dedicated Software Stack Pointer (SSP) and is automatically modified by exception processing, subroutine calls and returns; however, W15 can be referenced by any instruction in the same manner as all other W registers. This simplifies reading, writing and manipulating of the Stack Pointer (for example, creating stack frames).

Note: To protect against misaligned stack accesses, W15<0> is fixed to '0' by the hardware.

W15 is initialized to 0x1000 during all Resets. This address ensures that the SSP points to valid RAM in all dsPIC33EPXXXGP50X, dsPIC33EPXXXMC20X/50X and PIC24EPXXXGP/MC20X devices, and permits stack availability for non-maskable trap exceptions. These can occur before the SSP is initialized by the user software. You can reprogram the SSP during initialization to any location within Data Space.

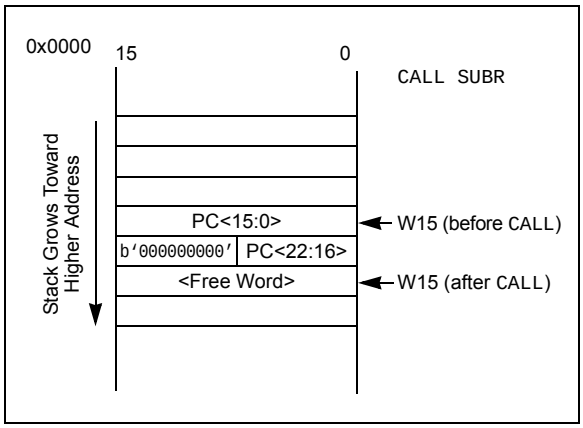
The Software Stack Pointer always points to the first available free word and fills the software stack working from lower toward higher addresses. Figure 4-19 illustrates how it pre-decrements for a stack pop (read) and post-increments for a stack push (writes).

When the PC is pushed onto the stack, PC<15:0> are pushed onto the first available stack word, then PC<22:16> are pushed into the second available stack location. For a PC push during any CALL instruction, the MSB of the PC is zero-extended before the push, as shown in Figure 4-19. During exception processing, the MSB of the PC is concatenated with the lower 8 bits of the CPU STATUS Register, SR. This allows the contents of SRL to be preserved automatically during interrupt processing.

Note 1: To maintain system Stack Pointer (W15) coherency, W15 is never subject to (EDS) paging, and is therefore restricted to an address range of 0x0000 to 0xFFFF. The same applies to the W14 when used as a Stack Frame Pointer (SFA = 1).

2: As the stack can be placed in, and can access X and Y spaces, care must be taken regarding its use, particularly with regard to local automatic variables in a C development environment

FIGURE 4-19: CALL STACK FRAME



REGISTER 6-1: RCON: RESET CONTROL REGISTER(1)

R/W-0	R/W-0	U-0	U-0	R/W-0	U-0	R/W-0	R/W-0
TRAPR	IOPUWR	—	—	VREGSF	—	CM	VREGS
bit 15							bit 8

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-1	R/W-1
EXTR	SWR	SWDTEN(2)	WDTO	SLEEP	IDLE	BOR	POR
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15 **TRAPR:** Trap Reset Flag bit
1 = A Trap Conflict Reset has occurred
0 = A Trap Conflict Reset has not occurred

bit 14 **IOPUWR:** Illegal Opcode or Uninitialized W Access Reset Flag bit
1 = An illegal opcode detection, an illegal address mode or Uninitialized W register used as an Address Pointer caused a Reset
0 = An illegal opcode or Uninitialized W register Reset has not occurred

bit 13-12 **Unimplemented:** Read as '0'

bit 11 **VREGSF:** Flash Voltage Regulator Standby During Sleep bit
1 = Flash voltage regulator is active during Sleep
0 = Flash voltage regulator goes into Standby mode during Sleep

bit 10 **Unimplemented:** Read as '0'

bit 9 **CM:** Configuration Mismatch Flag bit
1 = A Configuration Mismatch Reset has occurred.
0 = A Configuration Mismatch Reset has not occurred

bit 8 **VREGS:** Voltage Regulator Standby During Sleep bit
1 = Voltage regulator is active during Sleep
0 = Voltage regulator goes into Standby mode during Sleep

bit 7 **EXTR:** External Reset ($\overline{\text{MCLR}}$) Pin bit
1 = A Master Clear (pin) Reset has occurred
0 = A Master Clear (pin) Reset has not occurred

bit 6 **SWR:** Software RESET (Instruction) Flag bit
1 = A RESET instruction has been executed
0 = A RESET instruction has not been executed

bit 5 **SWDTEN:** Software Enable/Disable of WDT bit(2)
1 = WDT is enabled
0 = WDT is disabled

bit 4 **WDTO:** Watchdog Timer Time-out Flag bit
1 = WDT time-out has occurred
0 = WDT time-out has not occurred

Note 1: All of the Reset status bits can be set or cleared in software. Setting one of these bits in software does not cause a device Reset.

2: If the FWDTEN Configuration bit is '1' (unprogrammed), the WDT is always enabled, regardless of the SWDTEN bit setting.

REGISTER 8-3: DMAxSTAH: DMA CHANNEL x START ADDRESS REGISTER A (HIGH)

U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
—	—	—	—	—	—	—	—
bit 15							bit 8

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
STA<23:16>							
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 15-8 **Unimplemented:** Read as ‘0’

bit 7-0 **STA<23:16>:** Primary Start Address bits (source or destination)

REGISTER 8-4: DMAxSTAL: DMA CHANNEL x START ADDRESS REGISTER A (LOW)

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
STA<15:8>							
bit 15							bit 8

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
STA<7:0>							
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 15-0 **STA<15:0>:** Primary Start Address bits (source or destination)

REGISTER 9-1: OSCCON: OSCILLATOR CONTROL REGISTER(1) (CONTINUED)

bit 4 **Unimplemented:** Read as '0'

bit 3 **CF:** Clock Fail Detect bit(3)
- 1 = FSCM has detected clock failure
- 0 = FSCM has not detected clock failure

bit 2-1 **Unimplemented:** Read as '0'

bit 0 **OSWEN:** Oscillator Switch Enable bit
- 1 = Requests oscillator switch to selection specified by the NOSC<2:0> bits
- 0 = Oscillator switch is complete

Note 1: Writes to this register require an unlock sequence. Refer to **"Oscillator"** (DS70580) in the *"dsPIC33/PIC24 Family Reference Manual"* (available from the Microchip web site) for details.

2: Direct clock switches between any primary oscillator mode with PLL and FRCPLL mode are not permitted. This applies to clock switches in either direction. In these instances, the application must switch to FRC mode as a transitional clock source between the two PLL modes.

3: This bit should only be cleared in software. Setting the bit in software (= 1) will have the same effect as an actual oscillator failure and trigger an oscillator failure trap.

REGISTER 10-1: PMD1: PERIPHERAL MODULE DISABLE CONTROL REGISTER 1 (CONTINUED)

bit 3 **SPI1MD:** SPI1 Module Disable bit
1 = SPI1 module is disabled
0 = SPI1 module is enabled

bit 2 **Unimplemented:** Read as '0'

bit 1 **C1MD:** ECAN1 Module Disable bit(2)
1 = ECAN1 module is disabled
0 = ECAN1 module is enabled

bit 0 **AD1MD:** ADC1 Module Disable bit
1 = ADC1 module is disabled
0 = ADC1 module is enabled

Note 1: This bit is available on dsPIC33EPXXXMC20X/50X and PIC24EPXXXMC20X devices only.
2: This bit is available on dsPIC33EPXXXGP50X and dsPIC33EPXXXMC50X devices only.

REGISTER 11-2: RPINR1: PERIPHERAL PIN SELECT INPUT REGISTER 1

U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
—	—	—	—	—	—	—	—
bit 15							bit 8

U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
—	INT2R<6:0>						
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15-7 **Unimplemented:** Read as '0'

bit 6-0 **INT2R<6:0>:** Assign External Interrupt 2 (INT2) to the Corresponding RPn Pin bits (see Table 11-2 for input pin selection numbers)

1111001 = Input tied to RPI121
.
.
.
0000001 = Input tied to CMP1
0000000 = Input tied to Vss

REGISTER 11-3: RPINR3: PERIPHERAL PIN SELECT INPUT REGISTER 3

U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
—	—	—	—	—	—	—	—
bit 15							bit 8

U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
—	T2CKR<6:0>						
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15-7 **Unimplemented:** Read as '0'

bit 6-0 **T2CKR<6:0>:** Assign Timer2 External Clock (T2CK) to the Corresponding RPn pin bits (see Table 11-2 for input pin selection numbers)

1111001 = Input tied to RPI121
.
.
.
0000001 = Input tied to CMP1
0000000 = Input tied to Vss

REGISTER 11-12: RPINR22: PERIPHERAL PIN SELECT INPUT REGISTER 22

U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
—	SCK2INR<6:0>						
bit 15							bit 8

U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
—	SDI2R<6:0>						
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 15 **Unimplemented:** Read as ‘0’

bit 14-8 **SCK2INR<6:0>:** Assign SPI2 Clock Input (SCK2) to the Corresponding RPn Pin bits (see Table 11-2 for input pin selection numbers)

1111001 = Input tied to RPI121
.
.
.
0000001 = Input tied to CMP1
0000000 = Input tied to Vss

bit 7 **Unimplemented:** Read as ‘0’

bit 6-0 **SDI2R<6:0>:** Assign SPI2 Data Input (SDI2) to the Corresponding RPn Pin bits (see Table 11-2 for input pin selection numbers)

1111001 = Input tied to RPI121
.
.
.
0000001 = Input tied to CMP1
0000000 = Input tied to Vss

REGISTER 11-13: RPINR23: PERIPHERAL PIN SELECT INPUT REGISTER 23

U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
—	—	—	—	—	—	—	—
bit 15							bit 8

U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
—	SS2R<6:0>						
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 15-7 **Unimplemented:** Read as ‘0’

bit 6-0 **SS2R<6:0>:** Assign SPI2 Slave Select ($\overline{SS2}$) to the Corresponding RPn Pin bits (see Table 11-2 for input pin selection numbers)

1111001 = Input tied to RPI121
.
.
.
0000001 = Input tied to CMP1
0000000 = Input tied to Vss

REGISTER 11-14: RPINR26: PERIPHERAL PIN SELECT INPUT REGISTER 26 (dsPIC33EPXXXGP/MC50X DEVICES ONLY)

U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
—	—	—	—	—	—	—	—
bit 15							bit 8

U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
—	C1RXR<6:0>						
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 15-7 **Unimplemented:** Read as ‘0’

bit 6-0 **C1RXR<6:0>:** Assign CAN1 RX Input (CRX1) to the Corresponding RPn Pin bits (see Table 11-2 for input pin selection numbers)

1111001 = Input tied to RPI121
.
.
.
0000001 = Input tied to CMP1
0000000 = Input tied to Vss

REGISTER 17-2: QEI1IOC: QEI1 I/O CONTROL REGISTER

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
QCAPEN	FLTREN	QFDIV2	QFDIV1	QFDIV0	OUTFNC1	OUTFNC0	SWPAB
bit 15							bit 8

R/W-0	R/W-0	R/W-0	R/W-0	R-x	R-x	R-x	R-x
HOMPOL	IDXPOL	QEBPOL	QEAPOL	HOME	INDEX	QEB	QEA
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15 **QCAPEN:** QEI Position Counter Input Capture Enable bit
1 = Index match event triggers a position capture event
0 = Index match event does not trigger a position capture event

bit 14 **FLTREN:** QEAx/QEBx/INDXx/HOMEx Digital Filter Enable bit
1 = Input pin digital filter is enabled
0 = Input pin digital filter is disabled (bypassed)

bit 13-11 **QFDIV<2:0>:** QEAx/QEBx/INDXx/HOMEx Digital Input Filter Clock Divide Select bits
111 = 1:128 clock divide
110 = 1:64 clock divide
101 = 1:32 clock divide
100 = 1:16 clock divide
011 = 1:8 clock divide
010 = 1:4 clock divide
001 = 1:2 clock divide
000 = 1:1 clock divide

bit 10-9 **OUTFNC<1:0>:** QEI Module Output Function Mode Select bits
11 = The CTNCMPx pin goes high when QEI1LEC ≥ POS1CNT ≥ QEI1GEC
10 = The CTNCMPx pin goes high when POS1CNT ≤ QEI1LEC
01 = The CTNCMPx pin goes high when POS1CNT ≥ QEI1GEC
00 = Output is disabled

bit 8 **SWPAB:** Swap QEA and QEB Inputs bit
1 = QEAx and QEBx are swapped prior to quadrature decoder logic
0 = QEAx and QEBx are not swapped

bit 7 **HOMPOL:** HOMEx Input Polarity Select bit
1 = Input is inverted
0 = Input is not inverted

bit 6 **IDXPOL:** INDXx Input Polarity Select bit
1 = Input is inverted
0 = Input is not inverted

bit 5 **QEBPOL:** QEBx Input Polarity Select bit
1 = Input is inverted
0 = Input is not inverted

bit 4 **QEAPOL:** QEAx Input Polarity Select bit
1 = Input is inverted
0 = Input is not inverted

bit 3 **HOME:** Status of HOMEx Input Pin After Polarity Control
1 = Pin is at logic '1'
0 = Pin is at logic '0'

REGISTER 18-1: SPIxSTAT: SPIx STATUS AND CONTROL REGISTER (CONTINUED)

bit 1 **SPITBF:** SPIx Transmit Buffer Full Status bit

1 = Transmit not yet started, SPIxTXB is full
0 = Transmit started, SPIxTXB is empty

Standard Buffer mode:
Automatically set in hardware when core writes to the SPIxBUF location, loading SPIxTXB. Automatically cleared in hardware when SPIx module transfers data from SPIxTXB to SPIxSR.

Enhanced Buffer mode:
Automatically set in hardware when the CPU writes to the SPIxBUF location, loading the last available buffer location. Automatically cleared in hardware when a buffer location is available for a CPU write operation.

bit 0 **SPIRBF:** SPIx Receive Buffer Full Status bit

1 = Receive is complete, SPIxRXB is full
0 = Receive is incomplete, SPIxRXB is empty

Standard Buffer mode:
Automatically set in hardware when SPIx transfers data from SPIxSR to SPIxRXB. Automatically cleared in hardware when the core reads the SPIxBUF location, reading SPIxRXB.

Enhanced Buffer mode:
Automatically set in hardware when SPIx transfers data from SPIxSR to the buffer, filling the last unread buffer location. Automatically cleared in hardware when a buffer location is available for a transfer from SPIxSR.

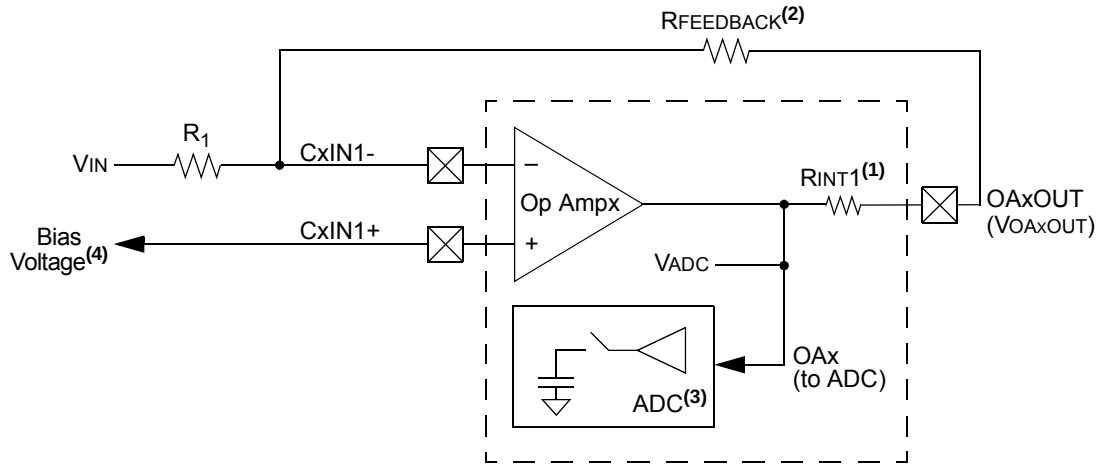
25.1 Op Amp Application Considerations

There are two configurations to take into consideration when designing with the op amp modules that are available in the dsPIC33EPXXXGP50X, dsPIC33EPXXXMC20X/50X and PIC24EPXXXGP/MC20X devices. Configuration A (see Figure 25-6) takes advantage of the internal connection to the ADC module to route the output of the op amp directly to the ADC for measurement. Configuration B (see Figure 25-7) requires that the designer externally route the output of the op amp (OAxOUT) to a separate analog input pin (ANy) on the device. Table 30-55 in **Section 30.0 "Electrical Characteristics"** describes the performance characteristics for the op amps, distinguishing between the two configuration types where applicable.

25.1.1 OP AMP CONFIGURATION A

Figure 25-6 shows a typical inverting amplifier circuit taking advantage of the internal connections from the op amp output to the input of the ADC. The advantage of this configuration is that the user does not need to consume another analog input (ANy) on the device, and allows the user to simultaneously sample all three op amps with the ADC module, if needed. However, the presence of the internal resistance, RINT1, adds an error in the feedback path. Since RINT1 is an internal resistance, in relation to the op amp output (VOAXOUT) and ADC internal connection (VADC), RINT1 must be included in the numerator term of the transfer function. See Table 30-53 in **Section 30.0 "Electrical Characteristics"** for the typical value of RINT1. Table 30-60 and Table 30-61 in **Section 30.0 "Electrical Characteristics"** describe the minimum sample time (TSAMP) requirements for the ADC module in this configuration. Figure 25-6 also defines the equations that should be used when calculating the expected voltages at points, VADC and VOAXOUT.

FIGURE 25-6: OP AMP CONFIGURATION A



$$V_{ADC} = \left(\frac{R_{FEEDBACK} + R_{INT1}}{R_1}\right)(\ Bias\ Voltage - V_{IN} \ )$$

$$V_{OAxOUT} = \left(\frac{R_{FEEDBACK}}{R_1}\right)(\ Bias\ Voltage - V_{IN} \ )$$

Note 1: See Table 30-53 for the Typical value.
2: See Table 30-53 for the Minimum value for the feedback resistor.
3: See Table 30-60 and Table 30-61 for the minimum sample time (TSAMP).
4: CVREF1O or CVREF2O are two options that are available for supplying bias voltage to the op amps.

REGISTER 25-5: CMxMSKCON: COMPARATOR x MASK GATING CONTROL REGISTER

R/W-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
HLMS	—	OCEN	OCNEN	OBEN	OBNEN	OAEN	OANEN
bit 15							bit 8

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
NAGS	PAGS	ACEN	ACNEN	ABEN	ABNEN	AAEN	AANEN
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15 **HLMS:** High or Low-Level Masking Select bits
1 = The masking (blanking) function will prevent any asserted ('0') comparator signal from propagating
0 = The masking (blanking) function will prevent any asserted ('1') comparator signal from propagating

bit 14 **Unimplemented:** Read as '0'

bit 13 **OCEN:** OR Gate C Input Enable bit
1 = MCI is connected to OR gate
0 = MCI is not connected to OR gate

bit 12 **OCNEN:** OR Gate C Input Inverted Enable bit
1 = Inverted MCI is connected to OR gate
0 = Inverted MCI is not connected to OR gate

bit 11 **OBEN:** OR Gate B Input Enable bit
1 = MBI is connected to OR gate
0 = MBI is not connected to OR gate

bit 10 **OBNEN:** OR Gate B Input Inverted Enable bit
1 = Inverted MBI is connected to OR gate
0 = Inverted MBI is not connected to OR gate

bit 9 **OAEN:** OR Gate A Input Enable bit
1 = MAI is connected to OR gate
0 = MAI is not connected to OR gate

bit 8 **OANEN:** OR Gate A Input Inverted Enable bit
1 = Inverted MAI is connected to OR gate
0 = Inverted MAI is not connected to OR gate

bit 7 **NAGS:** AND Gate Output Inverted Enable bit
1 = Inverted ANDI is connected to OR gate
0 = Inverted ANDI is not connected to OR gate

bit 6 **PAGS:** AND Gate Output Enable bit
1 = ANDI is connected to OR gate
0 = ANDI is not connected to OR gate

bit 5 **ACEN:** AND Gate C Input Enable bit
1 = MCI is connected to AND gate
0 = MCI is not connected to AND gate

bit 4 **ACNEN:** AND Gate C Input Inverted Enable bit
1 = Inverted MCI is connected to AND gate
0 = Inverted MCI is not connected to AND gate

26.3 Programmable CRC Registers

REGISTER 26-1: CRCCON1: CRC CONTROL REGISTER 1

R/W-0	U-0	R/W-0	R-0	R-0	R-0	R-0	R-0
CRCEN	—	CSIDL	VWORD4	VWORD3	VWORD2	VWORD1	VWORD0
bit 15							bit 8

R-0	R-1	R/W-0	R/W-0	R/W-0	U-0	U-0	U-0
CRCFUL	CRCMPT	CRCISEL	CRCGO	LENDIAN	—	—	—
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15 **CRCEN:** CRC Enable bit
1 = CRC module is enabled
0 = CRC module is disabled; all state machines, pointers and CRCWDAT/CRCDAT are reset, other SFRs are not reset

bit 14 **Unimplemented:** Read as '0'

bit 13 **CSIDL:** CRC Stop in Idle Mode bit
1 = Discontinues module operation when device enters Idle mode
0 = Continues module operation in Idle mode

bit 12-8 **VWORD<4:0>:** Pointer Value bits
Indicates the number of valid words in the FIFO. Has a maximum value of 8 when PLEN<4:0> > 7 or 16 when PLEN<4:0> ≤ 7.

bit 7 **CRCFUL**: CRC FIFO Full bit
1 = FIFO is full
0 = FIFO is not full

bit 6 **CRCMPT:** CRC FIFO Empty Bit
1 = FIFO is empty
0 = FIFO is not empty

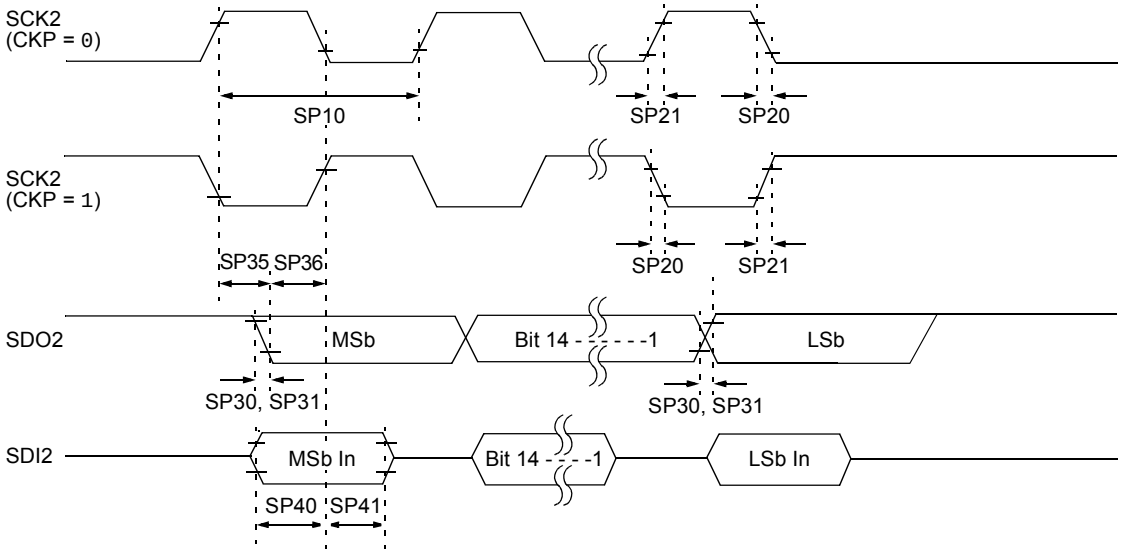
bit 5 **CRCISEL:** CRC Interrupt Selection bit
1 = Interrupt on FIFO is empty; final word of data is still shifting through CRC
0 = Interrupt on shift is complete and CRCWDAT results are ready

bit 4 **CRCGO:** Start CRC bit
1 = Starts CRC serial shifter
0 = CRC serial shifter is turned off

bit 3 **LENDIAN:** Data Word Little-Endian Configuration bit
1 = Data word is shifted into the CRC starting with the LSb (little endian)
0 = Data word is shifted into the CRC starting with the MSb (big endian)

bit 2-0 **Unimplemented:** Read as '0'

FIGURE 30-17: SPI2 MASTER MODE (FULL-DUPLEX, CKE = 0, CKP = x, SMP = 1) TIMING CHARACTERISTICS



Note: Refer to Figure 30-1 for load conditions.

TABLE 30-36: SPI2 MASTER MODE (FULL-DUPLEX, CKE = 0, CKP = x, SMP = 1) TIMING REQUIREMENTS

AC CHARACTERISTICS			Standard Operating Conditions: 3.0V to 3.6V (unless otherwise stated) Operating temperature -40°C ≤ TA ≤ +85°C for Industrial -40°C ≤ TA ≤ +125°C for Extended				
Param.	**Symbol**	**Characteristic(1)**	**Min.**	**Typ.(2)**	**Max.**	**Units**	**Conditions**
SP10	FscP	Maximum SCK2 Frequency	—	—	9	MHz	-40ºC to +125ºC **(Note 3)**
SP20	TscF	SCK2 Output Fall Time	—	—	—	ns	See Parameter DO32 **(Note 4)**
SP21	TscR	SCK2 Output Rise Time	—	—	—	ns	See Parameter DO31 **(Note 4)**
SP30	TdoF	SDO2 Data Output Fall Time	—	—	—	ns	See Parameter DO32 **(Note 4)**
SP31	TdoR	SDO2 Data Output Rise Time	—	—	—	ns	See Parameter DO31 **(Note 4)**
SP35	TscH2doV, TscL2doV	SDO2 Data Output Valid after SCK2 Edge	—	6	20	ns	
SP36	TdoV2scH, TdoV2scL	SDO2 Data Output Setup to First SCK2 Edge	30	—	—	ns	
SP40	TdiV2scH, TdiV2scL	Setup Time of SDI2 Data Input to SCK2 Edge	30	—	—	ns	
SP41	TscH2diL, TscL2diL	Hold Time of SDI2 Data Input to SCK2 Edge	30	—	—	ns	

Note 1: These parameters are characterized, but are not tested in manufacturing.

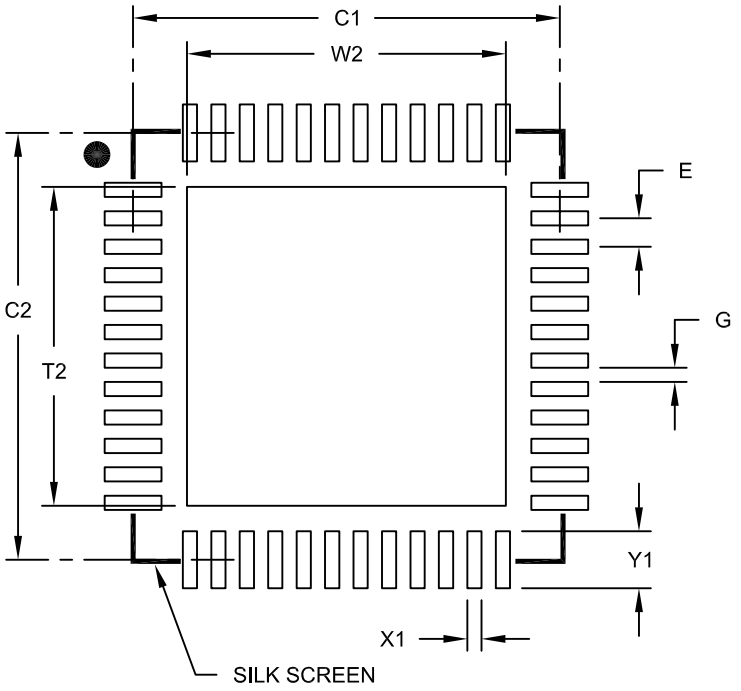
2: Data in "Typical" column is at 3.3V, +25°C unless otherwise stated.

3: The minimum clock period for SCK2 is 111 ns. The clock generated in Master mode must not violate this specification.

4: Assumes 50 pF load on all SPI2 pins.

48-Lead Ultra Thin Plastic Quad Flat, No Lead Package (MV) - 6x6 mm Body [UQFN]
With 0.40 mm Contact Length

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



RECOMMENDED LAND PATTERN

Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Contact Pitch	E		0.40 BSC	
Optional Center Pad Width	W2			4.45
Optional Center Pad Length	T2			4.45
Contact Pad Spacing	C1		6.00	
Contact Pad Spacing	C2		6.00	
Contact Pad Width (X28)	X1			0.20
Contact Pad Length (X28)	Y1			0.80
Distance Between Pads	G	0.20		

Notes:

1. Dimensioning and tolerancing per ASME Y14.5M

BSC: Basic Dimension. Theoretically exact value shown without tolerances.

Microchip Technology Drawing No. C04-2153A