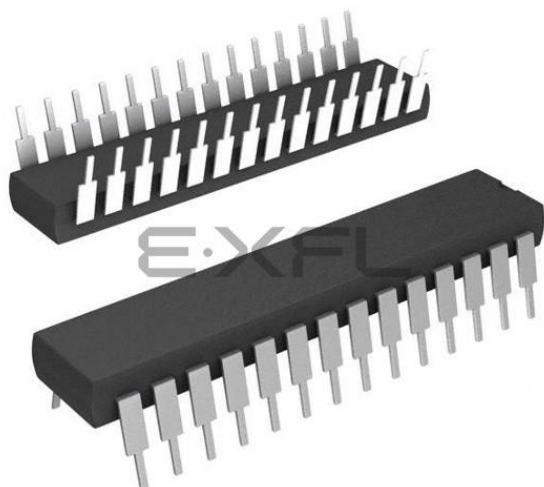




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Details

Product Status	Active
Core Processor	PIC
Core Size	16-Bit
Speed	60 MIPS
Connectivity	I ² C, IrDA, LINbus, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, DMA, POR, PWM, WDT
Number of I/O	21
Program Memory Size	512KB (170K x 24)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	24K x 16
Voltage - Supply (Vcc/Vdd)	3V ~ 3.6V
Data Converters	A/D 6x10b/12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 125°C (TA)
Mounting Type	Through Hole
Package / Case	28-DIP (0.300", 7.62mm)
Supplier Device Package	28-SPDIP
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/pic24ep512gp202-e-sp

TABLE 2: dsPIC33EPXXXMC20X/50X and PIC24EPXXXMC20X MOTOR CONTROL FAMILIES

Device	Page Erase Size (Instructions)	Program Flash Memory (Kbytes)	RAM (Kbytes)	Remappable Peripherals									I ² C™	CRC Generator	10-Bit/12-Bit ADC (Channels)	Op Amps/Comparators	CTMU	PTG	I/O Pins	Pins	Packages
				16-Bit/32-Bit Timers	Input Capture	Output Compare	Motor Control PWM ⁽⁴⁾ (Channels)	Quadrature Encoder Interface	UART	SPI ⁽²⁾	ECAN™ Technology	External Interrupts ⁽³⁾									
PIC24EP32MC202	512	32	4	5	4	4	6	1	2	2	—	3	2	1	6	2/3 ⁽¹⁾	Yes	Yes	21	28	SPDIP, SOIC, SSOP ⁽⁵⁾ , QFN-S
PIC24EP64MC202	1024	64	8																		
PIC24EP128MC202	1024	128	16																		
PIC24EP256MC202	1024	256	32																		
PIC24EP512MC202	1024	512	48	5	4	4	6	1	2	2	—	3	2	1	8	3/4	Yes	Yes	25	36	VTLA
PIC24EP32MC203	512	32	4																		
PIC24EP64MC203	1024	64	8																		
PIC24EP32MC204	512	32	4																		
PIC24EP64MC204	1024	64	8	5	4	4	6	1	2	2	—	3	2	1	9	3/4	Yes	Yes	35	44/48	VTLA ⁽⁵⁾ , TQFP, QFN, UQFN
PIC24EP128MC204	1024	128	16																		
PIC24EP256MC204	1024	256	32																		
PIC24EP512MC204	1024	512	48																		
PIC24EP64MC206	1024	64	8	5	4	4	6	1	2	2	—	3	2	1	16	3/4	Yes	Yes	53	64	TQFP, QFN
PIC24EP128MC206	1024	128	16																		
PIC24EP256MC206	1024	256	32																		
PIC24EP512MC206	1024	512	48																		
dsPIC33EP32MC202	512	32	4	5	4	4	6	1	2	2	—	3	2	1	6	2/3 ⁽¹⁾	Yes	Yes	21	28	SPDIP, SOIC, SSOP ⁽⁵⁾ , QFN-S
dsPIC33EP64MC202	1024	64	8																		
dsPIC33EP128MC202	1024	128	16																		
dsPIC33EP256MC202	1024	256	32																		
dsPIC33EP512MC202	1024	512	48	5	4	4	6	1	2	2	—	3	2	1	8	3/4	Yes	Yes	25	36	VTLA
dsPIC33EP32MC203	512	32	4																		
dsPIC33EP64MC203	1024	64	8																		
dsPIC33EP32MC204	512	32	4																		
dsPIC33EP64MC204	1024	64	8	5	4	4	6	1	2	2	—	3	2	1	9	3/4	Yes	Yes	35	44/48	VTLA ⁽⁵⁾ , TQFP, QFN, UQFN
dsPIC33EP128MC204	1024	128	16																		
dsPIC33EP256MC204	1024	256	32																		
dsPIC33EP512MC204	1024	512	48																		
dsPIC33EP64MC206	1024	64	8	5	4	4	6	1	2	2	—	3	2	1	16	3/4	Yes	Yes	53	64	TQFP, QFN
dsPIC33EP128MC206	1024	128	16																		
dsPIC33EP256MC206	1024	256	32																		
dsPIC33EP512MC206	1024	512	48																		
dsPIC33EP32MC502	512	32	4	5	4	4	6	1	2	2	1	3	2	1	6	2/3 ⁽¹⁾	Yes	Yes	21	28	SPDIP, SOIC, SSOP ⁽⁵⁾ , QFN-S
dsPIC33EP64MC502	1024	64	8																		
dsPIC33EP128MC502	1024	128	16																		
dsPIC33EP256MC502	1024	256	32																		
dsPIC33EP512MC502	1024	512	48	5	4	4	6	1	2	2	1	3	2	1	8	3/4	Yes	Yes	25	36	VTLA
dsPIC33EP32MC503	512	32	4																		
dsPIC33EP64MC503	1024	64	8																		

Note 1: On 28-pin devices, Comparator 4 does not have external connections. Refer to **Section 25.0 “Op Amp/Comparator Module”** for details.

2: Only SPI2 is remappable.

3: INT0 is not remappable.

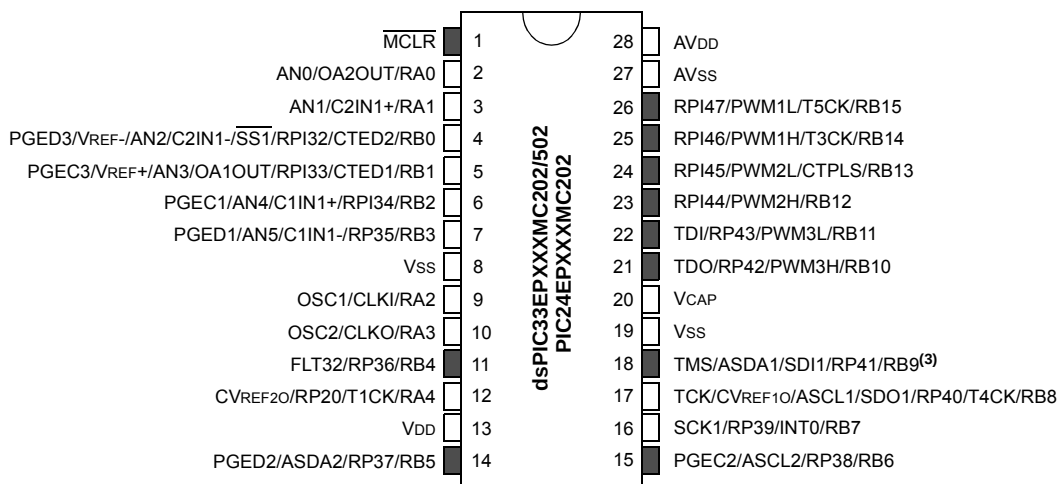
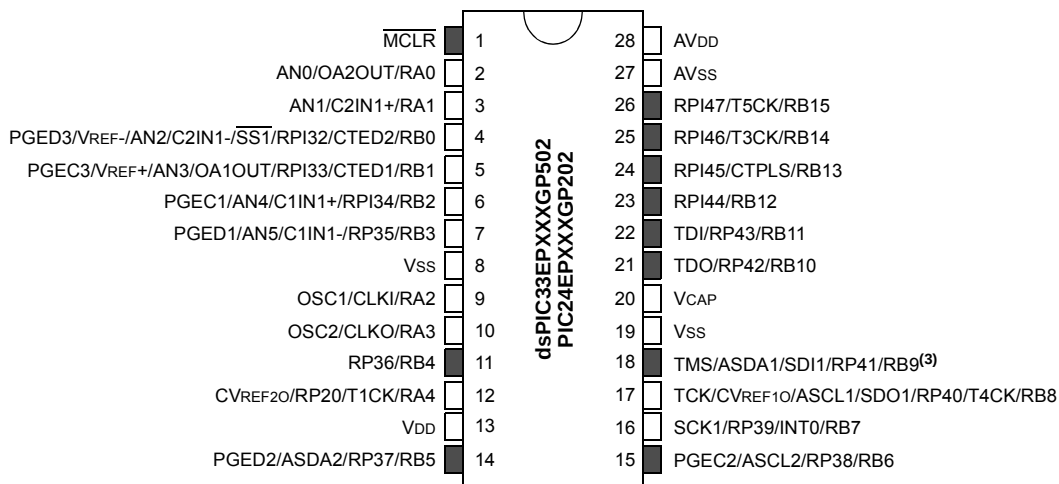
4: Only the PWM Faults are remappable.

5: The SSOP and VTLA packages are not available for devices with 512 Kbytes of memory.

Pin Diagrams

28-Pin SPDIP/SOIC/SSOP^(1,2)

■ = Pins are up to 5V tolerant

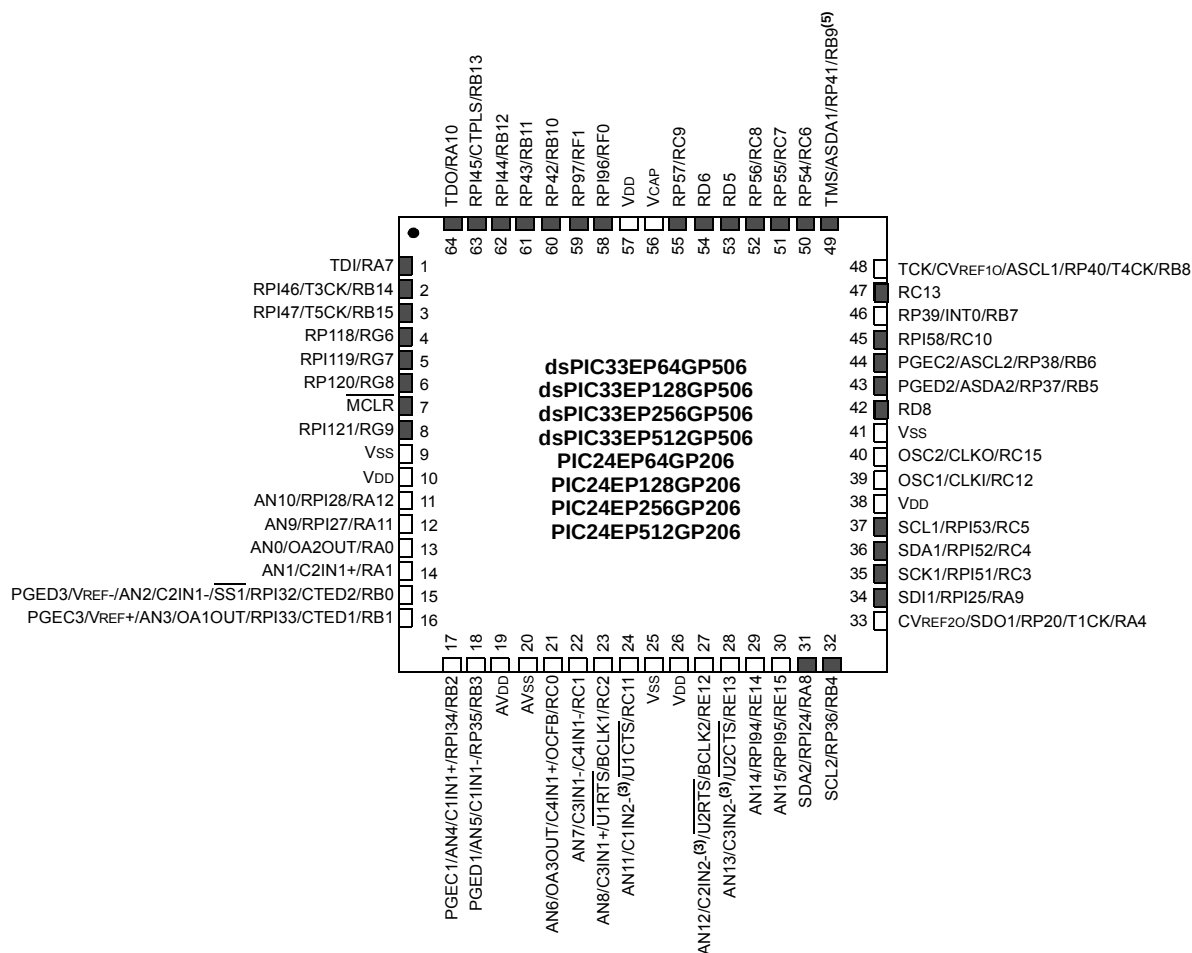


- Note 1:** The RPN/RPIn pins can be used by any remappable peripheral with some limitation. See **Section 11.4 “Peripheral Pin Select (PPS)”** for available peripherals and for information on limitations.
- Note 2:** Every I/O port pin (RAX-RGx) can be used as a Change Notification pin (CNAX-CNGx). See **Section 11.0 “I/O Ports”** for more information.
- Note 3:** There is an internal pull-up resistor connected to the TMS pin when the JTAG interface is active. See the JTAGEN bit field in Table 27-2.

Pin Diagrams (Continued)

64-Pin QFN^(1,2,3,4)

■ = Pins are up to 5V tolerant



- Note 1:** The RPN/RPIN pins can be used by any remappable peripheral with some limitation. See **Section 11.4 “Peripheral Pin Select (PPS)”** for available peripherals and for information on limitations.
- Note 2:** Every I/O port pin (RAX-RGX) can be used as a Change Notification pin (CNAX-CNGX). See **Section 11.0 “I/O Ports”** for more information.
- Note 3:** This pin is not available as an input when OPMODE (CMxCON<10>) = 1.
- Note 4:** The metal pad at the bottom of the device is not connected to any pins and is recommended to be connected to Vss externally.
- Note 5:** There is an internal pull-up resistor connected to the TMS pin when the JTAG interface is active. See the JTAGEN bit field in Table 27-2.

TABLE 1-1: PINOUT I/O DESCRIPTIONS (CONTINUED)

Pin Name ⁽⁴⁾	Pin Type	Buffer Type	PPS	Description
U2CTS	I	ST	No	UART2 Clear-To-Send.
U2RTS	O	—	No	UART2 Ready-To-Send.
U2RX	I	ST	Yes	UART2 receive.
U2TX	O	—	Yes	UART2 transmit.
BCLK2	O	ST	No	UART2 IrDA [®] baud clock output.
SCK1	I/O	ST	No	Synchronous serial clock input/output for SPI1.
SDI1	I	ST	No	SPI1 data in.
SDO1	O	—	No	SPI1 data out.
SS1	I/O	ST	No	SPI1 slave synchronization or frame pulse I/O.
SCK2	I/O	ST	Yes	Synchronous serial clock input/output for SPI2.
SDI2	I	ST	Yes	SPI2 data in.
SDO2	O	—	Yes	SPI2 data out.
SS2	I/O	ST	Yes	SPI2 slave synchronization or frame pulse I/O.
SCL1	I/O	ST	No	Synchronous serial clock input/output for I2C1.
SDA1	I/O	ST	No	Synchronous serial data input/output for I2C1.
ASCL1	I/O	ST	No	Alternate synchronous serial clock input/output for I2C1.
ASDA1	I/O	ST	No	Alternate synchronous serial data input/output for I2C1.
SCL2	I/O	ST	No	Synchronous serial clock input/output for I2C2.
SDA2	I/O	ST	No	Synchronous serial data input/output for I2C2.
ASCL2	I/O	ST	No	Alternate synchronous serial clock input/output for I2C2.
ASDA2	I/O	ST	No	Alternate synchronous serial data input/output for I2C2.
TMS ⁽⁵⁾	I	ST	No	JTAG Test mode select pin.
TCK	I	ST	No	JTAG test clock input pin.
TDI	I	ST	No	JTAG test data input pin.
TDO	O	—	No	JTAG test data output pin.
C1RX ⁽²⁾	I	ST	Yes	ECAN1 bus receive pin.
C1TX ⁽²⁾	O	—	Yes	ECAN1 bus transmit pin.
FLT1 ⁽¹⁾ , FLT2 ⁽¹⁾	I	ST	Yes	PWM Fault Inputs 1 and 2.
FLT3 ⁽¹⁾ , FLT4 ⁽¹⁾	I	ST	No	PWM Fault Inputs 3 and 4.
FLT32 ^(1,3)	I	ST	No	PWM Fault Input 32 (Class B Fault).
DTCMP1-DTCMP3 ⁽¹⁾	I	ST	Yes	PWM Dead-Time Compensation Inputs 1 through 3.
PWM1L-PWM3L ⁽¹⁾	O	—	No	PWM Low Outputs 1 through 3.
PWM1H-PWM3H ⁽¹⁾	O	—	No	PWM High Outputs 1 through 3.
SYNCl1 ⁽¹⁾	I	ST	Yes	PWM Synchronization Input 1.
SYNCO1 ⁽¹⁾	O	—	Yes	PWM Synchronization Output 1.
INDX1 ⁽¹⁾	I	ST	Yes	Quadrature Encoder Index1 pulse input.
HOME1 ⁽¹⁾	I	ST	Yes	Quadrature Encoder Home1 pulse input.
QEA1 ⁽¹⁾	I	ST	Yes	Quadrature Encoder Phase A input in QE11 mode. Auxiliary timer external clock/gate input in Timer mode.
QEB1 ⁽¹⁾	I	ST	Yes	Quadrature Encoder Phase B input in QE11 mode. Auxiliary timer external clock/gate input in Timer mode.
CNTCMP1 ⁽¹⁾	O	—	Yes	Quadrature Encoder Compare Output 1.

Legend: CMOS = CMOS compatible input or output Analog = Analog input P = Power
ST = Schmitt Trigger input with CMOS levels O = Output I = Input
PPS = Peripheral Pin Select TTL = TTL input buffer

- Note 1:** This pin is available on dsPIC33EPXXXMC20X/50X and PIC24EPXXXMC20X devices only.
- 2:** This pin is available on dsPIC33EPXXXGP/MC50X devices only.
- 3:** This is the default Fault on Reset for dsPIC33EPXXXMC20X/50X and PIC24EPXXXMC20X devices. See **Section 16.0 “High-Speed PWM Module (dsPIC33EPXXXMC20X/50X and PIC24EPXXXMC20X Devices Only)”** for more information.
- 4:** Not all pins are available in all packages variants. See the **“Pin Diagrams”** section for pin availability.
- 5:** There is an internal pull-up resistor connected to the TMS pin when the JTAG interface is active. See the JTAGEN bit field in Table 27-2.

TABLE 4-53: PORTA REGISTER MAP FOR PIC24EPXXXGP/MC204 AND dsPIC33EPXXXGP/MC204/504 DEVICES ONLY

File Name	Addr.	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	All Resets
TRISA	0E00	—	—	—	—	—	TRISA10	TRISA9	TRISA8	TRISA7	—	—	TRISA4	TRISA3	TRISA2	TRISA1	TRISA0	079F
PORTA	0E02	—	—	—	—	—	RA10	RA9	RA8	RA7	—	—	RA4	RA3	RA2	RA1	RA0	0000
LATA	0E04	—	—	—	—	—	LATA10	LATA9	LATA8	LATA7	—	—	LATA4	LATA3	LATA2	LA1TA1	LA0TA0	0000
ODCA	0E06	—	—	—	—	—	ODCA10	ODCA9	ODCA8	ODCA7	—	—	ODCA4	ODCA3	ODCA2	ODCA1	ODCA0	0000
CNENA	0E08	—	—	—	—	—	CNIEA10	CNIEA9	CNIEA8	CNIEA7	—	—	CNIEA4	CNIEA3	CNIEA2	CNIEA1	CNIEA0	0000
CNPUA	0E0A	—	—	—	—	—	CNPUA10	CNPUA9	CNPUA8	CNPUA7	—	—	CNPUA4	CNPUA3	CNPUA2	CNPUA1	CNPUA0	0000
CNPDA	0E0C	—	—	—	—	—	CNPDA10	CNPDA9	CNPDA8	CNPDA7	—	—	CNPDA4	CNPDA3	CNPDA2	CNPDA1	CNPDA0	0000
ANSELA	0E0E	—	—	—	—	—	—	—	—	—	—	—	ANSA4	—	—	ANSA1	ANSA0	0013

Legend: — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

TABLE 4-54: PORTB REGISTER MAP FOR PIC24EPXXXGP/MC204 AND dsPIC33EPXXXGP/MC204/504 DEVICES ONLY

File Name	Addr.	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	All Resets
TRISB	0E10	TRISB15	TRISB14	TRISB13	TRISB12	TRISB11	TRISB10	TRISB9	TRISB8	TRISB7	TRISB6	TRISB5	TRISB4	TRISB3	TRISB2	TRISB1	TRISB0	FFFF
PORTB	0E12	RB15	RB14	RB13	RB12	RB11	RB10	RB9	RB8	RB7	RB6	RB5	RB4	RB3	RB2	RB1	RB0	xxxx
LATB	0E14	LATB15	LATB14	LATB13	LATB12	LATB11	LATB10	LATB9	LATB8	LATB7	LATB6	LATB5	LATB4	LATB3	LATB2	LATB1	LATB0	xxxx
ODCB	0E16	ODCB15	ODCB14	ODCB13	ODCB12	ODCB11	ODCB10	ODCB9	ODCB8	ODCB7	ODCB6	ODCB5	ODCB4	ODCB3	ODCB2	ODCB1	ODCB0	0000
CNENB	0E18	CNIEB15	CNIEB14	CNIEB13	CNIEB12	CNIEB11	CNIEB10	CNIEB9	CNIEB8	CNIEB7	CNIEB6	CNIEB5	CNIEB4	CNIEB3	CNIEB2	CNIEB1	CNIEB0	0000
CNPUB	0E1A	CNPUB15	CNPUB14	CNPUB13	CNPUB12	CNPUB11	CNPUB10	CNPUB9	CNPUB8	CNPUB7	CNPUB6	CNPUB5	CNPUB4	CNPUB3	CNPUB2	CNPUB1	CNPUB0	0000
CNPDB	0E1C	CNPDB15	CNPDB14	CNPDB13	CNPDB12	CNPDB11	CNPDB10	CNPDB9	CNPDB8	CNPDB7	CNPDB6	CNPDB5	CNPDB4	CNPDB3	CNPDB2	CNPDB1	CNPDB0	0000
ANSELB	0E1E	—	—	—	—	—	—	—	ANSB8	—	—	—	—	ANSB3	ANSB2	ANSB1	ANSB0	010F

Legend: x = unknown value on Reset, — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

TABLE 4-55: PORTC REGISTER MAP FOR PIC24EPXXXGP/MC204 AND dsPIC33EPXXXGP/MC204/504 DEVICES ONLY

File Name	Addr.	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	All Resets
TRISC	0E20	—	—	—	—	—	—	TRISC9	TRISC8	TRISC7	TRISC6	TRISC5	TRISC4	TRISC3	TRISC2	TRISC1	TRISC0	03FF
PORTC	0E22	—	—	—	—	—	—	RC9	RC8	RC7	RC6	RC5	RC4	RC3	RC2	RC1	RC0	xxxx
LATC	0E24	—	—	—	—	—	—	LATC9	LATC8	LATC7	LATC6	LATC5	LATC4	LATC3	LATC2	LATC1	LATC0	xxxx
ODCC	0E26	—	—	—	—	—	—	ODCC9	ODCC8	ODCC7	ODCC6	ODCC5	ODCC4	ODCC3	ODCC2	ODCC1	ODCC0	0000
CNENC	0E28	—	—	—	—	—	—	CNIEC9	CNIEC8	CNIEC7	CNIEC6	CNIEC5	CNIEC4	CNIEC3	CNIEC2	CNIEC1	CNIEC0	0000
CNPUC	0E2A	—	—	—	—	—	—	CNPUC9	CNPUC8	CNPUC7	CNPUC6	CNPUC5	CNPUC4	CNPUC3	CNPUC2	CNPUC1	CNPUC0	0000
CNPDC	0E2C	—	—	—	—	—	—	CNPDC9	CNPDC8	CNPDC7	CNPDC6	CNPDC5	CNPDC4	CNPDC3	CNPDC2	CNPDC1	CNPDC0	0000
ANSELC	0E2E	—	—	—	—	—	—	—	—	—	—	—	—	—	ANSC2	ANSC1	ANSC0	0007

Legend: x = unknown value on Reset, — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

6.1 Reset Resources

Many useful resources are provided on the main product page of the Microchip web site for the devices listed in this data sheet. This product page, which can be accessed using this link, contains the latest updates and additional information.

Note:	In the event you are not able to access the product page using the link above, enter this URL in your browser: http://www.microchip.com/wwwproducts/Devices.aspx?dDocName=en555464
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6.1.1 KEY RESOURCES

- “Reset” (DS70602) in the “dsPIC33/PIC24 Family Reference Manual”
- Code Samples
- Application Notes
- Software Libraries
- Webinars
- All Related “dsPIC33/PIC24 Family Reference Manual” Sections
- Development Tools

9.1 CPU Clocking System

The dsPIC33EPXXXGP50X, dsPIC33EPXXXMC20X/50X and PIC24EPXXXGP/MC20X family of devices provides six system clock options:

- Fast RC (FRC) Oscillator
- FRC Oscillator with Phase Locked Loop (PLL)
- FRC Oscillator with Postscaler
- Primary (XT, HS or EC) Oscillator
- Primary Oscillator with PLL
- Low-Power RC (LPRC) Oscillator

Instruction execution speed or device operating frequency, F_{CY} , is given by Equation 9-1.

EQUATION 9-1: DEVICE OPERATING FREQUENCY

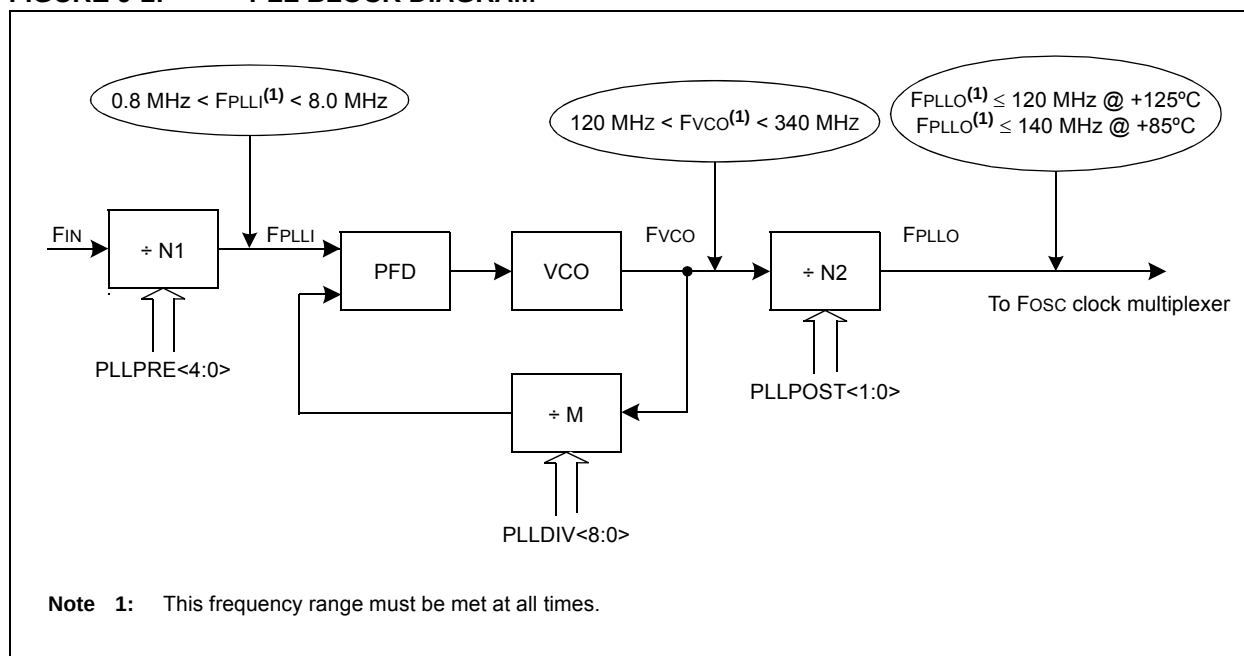
$$F_{CY} = F_{osc}/2$$

Figure 9-2 is a block diagram of the PLL module.

Equation 9-2 provides the relationship between input frequency (F_{IN}) and output frequency (F_{PLLO}). In clock modes S1 and S3, when the PLL output is selected, $F_{OSC} = F_{PLLO}$.

Equation 9-3 provides the relationship between input frequency (F_{IN}) and VCO frequency (F_{VCO}).

FIGURE 9-2: PLL BLOCK DIAGRAM



EQUATION 9-2: F_{PLLO} CALCULATION

$$F_{PLLO} = F_{IN} \times \left(\frac{M}{N1 \times N2} \right) = F_{IN} \times \left(\frac{(PLLDIV + 2)}{(PLLPRE + 2) \times 2(PLLPOST + 1)} \right)$$

Where:

$$N1 = PLLPRE + 2$$

$$N2 = 2 \times (PLLPOST + 1)$$

$$M = PLLDIV + 2$$

EQUATION 9-3: F_{VCO} CALCULATION

$$F_{VCO} = F_{IN} \times \left(\frac{M}{N1} \right) = F_{IN} \times \left(\frac{(PLLDIV + 2)}{(PLLPRE + 2)} \right)$$

REGISTER 10-5: PMD6: PERIPHERAL MODULE DISABLE CONTROL REGISTER 6

U-0	U-0	U-0	U-0	U-0	R/W-0	R/W-0	R/W-0
—	—	—	—	—	PWM3MD ⁽¹⁾	PWM2MD ⁽¹⁾	PWM1MD ⁽¹⁾
bit 15					bit 8		

U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
—	—	—	—	—	—	—	—
bit 7					bit 0		

Legend:

R = Readable bit

W = Writable bit

U = Unimplemented bit, read as '0'

-n = Value at POR

'1' = Bit is set

'0' = Bit is cleared

x = Bit is unknown

bit 15-11 **Unimplemented:** Read as '0'

bit 10 **PWM3MD:** PWM3 Module Disable bit⁽¹⁾

1 = PWM3 module is disabled

0 = PWM3 module is enabled

bit 9 **PWM2MD:** PWM2 Module Disable bit⁽¹⁾

1 = PWM2 module is disabled

0 = PWM2 module is enabled

bit 8 **PWM1MD:** PWM1 Module Disable bit⁽¹⁾

1 = PWM1 module is disabled

0 = PWM1 module is enabled

bit 7-0 **Unimplemented:** Read as '0'

Note 1: This bit is available on dsPIC33EPXXXMC50X/20X and PIC24EPXXXMC20X devices only.

- g) The TRISx registers control *only* the digital I/O output buffer. Any other dedicated or remappable active “output” will automatically override the TRIS setting. The TRISx register *does not* control the digital logic “input” buffer. Remappable digital “inputs” do not automatically override TRIS settings, which means that the TRISx bit must be set to input for pins with only remappable input function(s) assigned
- h) All analog pins are enabled by default after any Reset and the corresponding digital input buffer on the pin has been disabled. Only the Analog Pin Select registers control the digital input buffer, *not* the TRISx register. The user must disable the analog function on a pin using the Analog Pin Select registers in order to use any “digital input(s)” on a corresponding pin, no exceptions.

11.6 I/O Ports Resources

Many useful resources are provided on the main product page of the Microchip web site for the devices listed in this data sheet. This product page, which can be accessed using this link, contains the latest updates and additional information.

Note: In the event you are not able to access the product page using the link above, enter this URL in your browser:
<http://www.microchip.com/wwwproducts/Devices.aspx?dDocName=en555464>

11.6.1 KEY RESOURCES

- “I/O Ports” (DS70598) in the “*dsPIC33/PIC24 Family Reference Manual*”
- Code Samples
- Application Notes
- Software Libraries
- Webinars
- All Related “*dsPIC33/PIC24 Family Reference Manual*” Sections
- Development Tools

15.0 OUTPUT COMPARE

Note 1: This data sheet summarizes the features of the dsPIC33EPXXXGP50X, dsPIC33EPXXXMC20X/50X and PIC24EPXXXGP/MC20X families of devices. It is not intended to be a comprehensive reference source. To complement the information in this data sheet, refer to “**Output Compare**” (DS70358) in the “dsPIC33/PIC24 Family Reference Manual”, which is available from the Microchip web site (www.microchip.com).

2: Some registers and associated bits described in this section may not be available on all devices. Refer to **Section 4.0 “Memory Organization”** in this data sheet for device-specific register and bit information.

The output compare module can select one of seven available clock sources for its time base. The module compares the value of the timer with the value of one or two compare registers depending on the operating mode selected. The state of the output pin changes when the timer value matches the compare register value. The output compare module generates either a single output pulse or a sequence of output pulses, by changing the state of the output pin on the compare match events. The output compare module can also generate interrupts on compare match events and trigger DMA data transfers.

Note: See “**Output Compare**” (DS70358) in the “dsPIC33/PIC24 Family Reference Manual” for OCxR and OCxRS register restrictions.

FIGURE 15-1: OUTPUT COMPARE x MODULE BLOCK DIAGRAM

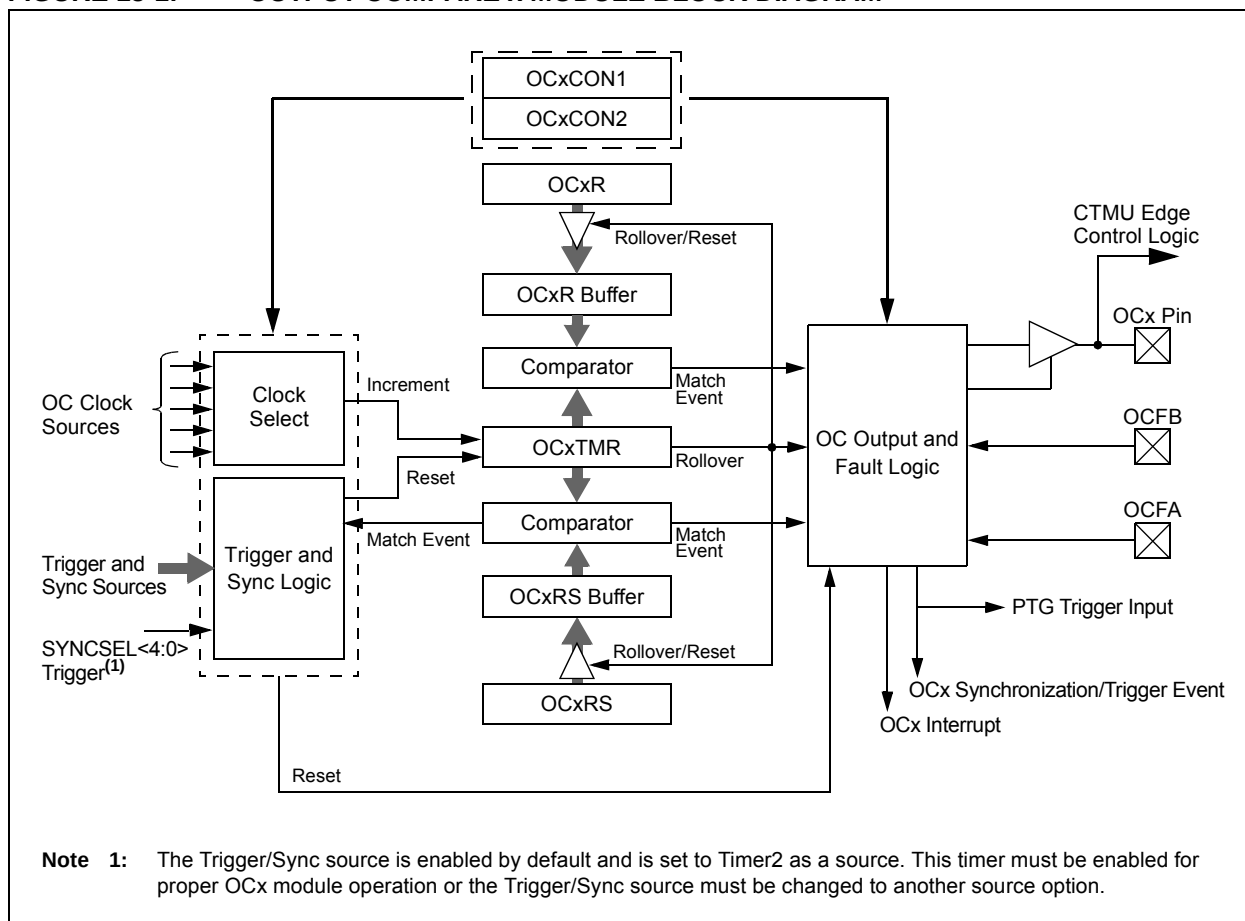
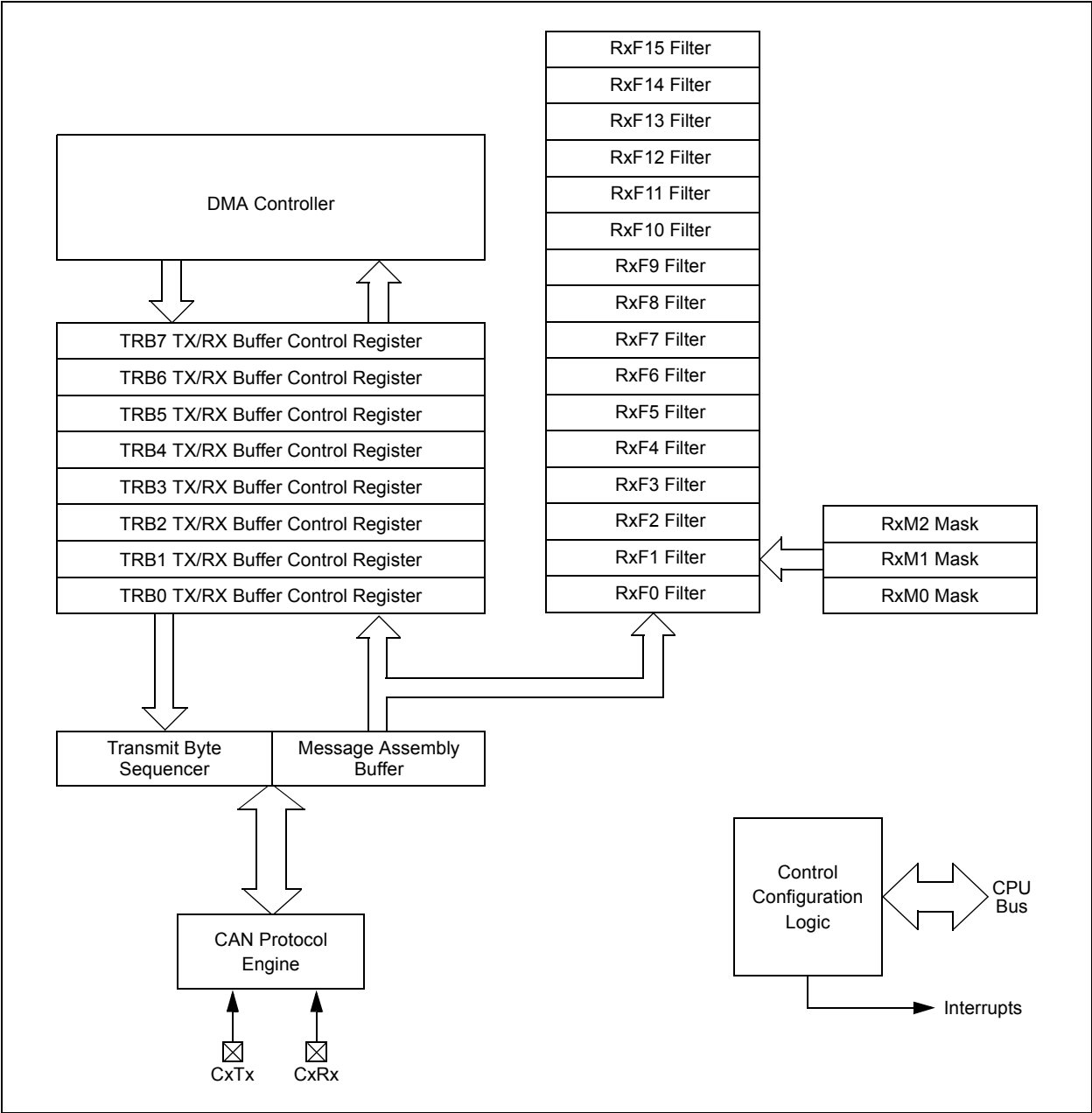


FIGURE 21-1: ECAN™ MODULE BLOCK DIAGRAM



BUFFER 21-5: ECAN™ MESSAGE BUFFER WORD 4

R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x
Byte 3							
bit 15							
bit 8							

R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x
Byte 2							
bit 7							
bit 0							

Legend:

R = Readable bit W = Writable bit U = Unimplemented bit, read as '0'
 -n = Value at POR '1' = Bit is set '0' = Bit is cleared x = Bit is unknown

bit 15-8 **Byte 3<15:8>**: ECAN Message Byte 3 bits

bit 7-0 **Byte 2<7:0>**: ECAN Message Byte 2 bits

BUFFER 21-6: ECAN™ MESSAGE BUFFER WORD 5

R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x
Byte 5							
bit 15							
bit 8							

R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x
Byte 4							
bit 7							
bit 0							

Legend:

R = Readable bit W = Writable bit U = Unimplemented bit, read as '0'
 -n = Value at POR '1' = Bit is set '0' = Bit is cleared x = Bit is unknown

bit 15-8 **Byte 5<15:8>**: ECAN Message Byte 5 bits

bit 7-0 **Byte 4<7:0>**: ECAN Message Byte 4 bits

REGISTER 24-2: PTGCON: PTG CONTROL REGISTER

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
PTGCLK2	PTGCLK1	PTGCLK0	PTGDIV4	PTGDIV3	PTGDIV2	PTGDIV1	PTGDIV0
bit 15							bit 8

R/W-0	R/W-0	R/W-0	R/W-0	U-0	R/W-0	R/W-0	R/W-0
PTGPWD3	PTGPWD2	PTGPWD1	PTGPWD0	—	PTGWDT2	PTGWDT1	PTGWDT0
bit 7							bit 0

Legend:

R = Readable bit W = Writable bit U = Unimplemented bit, read as '0'
 -n = Value at POR '1' = Bit is set '0' = Bit is cleared x = Bit is unknown

bit 15-13 **PTGCLK<2:0>:** Select PTG Module Clock Source bits

111 = Reserved
 110 = Reserved
 101 = PTG module clock source will be T3CLK
 100 = PTG module clock source will be T2CLK
 011 = PTG module clock source will be T1CLK
 010 = PTG module clock source will be TAD
 001 = PTG module clock source will be Fosc
 000 = PTG module clock source will be FP

bit 12-8 **PTGDIV<4:0>:** PTG Module Clock Prescaler (divider) bits

11111 = Divide-by-32
 11110 = Divide-by-31
 •
 •
 •
 00001 = Divide-by-2
 00000 = Divide-by-1

bit 7-4 **PTGPWD<3:0>:** PTG Trigger Output Pulse-Width bits

1111 = All trigger outputs are 16 PTG clock cycles wide
 1110 = All trigger outputs are 15 PTG clock cycles wide
 •
 •
 •
 0001 = All trigger outputs are 2 PTG clock cycles wide
 0000 = All trigger outputs are 1 PTG clock cycle wide

bit 3 **Unimplemented:** Read as '0'

bit 2-0 **PTGWDT<2:0>:** Select PTG Watchdog Timer Time-out Count Value bits

111 = Watchdog Timer will time-out after 512 PTG clocks
 110 = Watchdog Timer will time-out after 256 PTG clocks
 101 = Watchdog Timer will time-out after 128 PTG clocks
 100 = Watchdog Timer will time-out after 64 PTG clocks
 011 = Watchdog Timer will time-out after 32 PTG clocks
 010 = Watchdog Timer will time-out after 16 PTG clocks
 001 = Watchdog Timer will time-out after 8 PTG clocks
 000 = Watchdog Timer is disabled

TABLE 28-2: INSTRUCTION SET OVERVIEW (CONTINUED)

Base Instr #	Assembly Mnemonic	Assembly Syntax	Description	# of Words	# of Cycles ⁽²⁾	Status Flags Affected
52	MUL	MUL.SS Wb, Ws, Wnd	{Wnd + 1, Wnd} = signed(Wb) * signed(Ws)	1	1	None
		MUL.SS Wb, Ws, Acc ⁽¹⁾	Accumulator = signed(Wb) * signed(Ws)	1	1	None
		MUL.SU Wb, Ws, Wnd	{Wnd + 1, Wnd} = signed(Wb) * unsigned(Ws)	1	1	None
		MUL.SU Wb, Ws, Acc ⁽¹⁾	Accumulator = signed(Wb) * unsigned(Ws)	1	1	None
		MUL.SU Wb, #lit5, Acc ⁽¹⁾	Accumulator = signed(Wb) * unsigned(lit5)	1	1	None
		MUL.US Wb, Ws, Wnd	{Wnd + 1, Wnd} = unsigned(Wb) * signed(Ws)	1	1	None
		MUL.US Wb, Ws, Acc ⁽¹⁾	Accumulator = unsigned(Wb) * signed(Ws)	1	1	None
		MUL.UU Wb, Ws, Wnd	{Wnd + 1, Wnd} = unsigned(Wb) * unsigned(Ws)	1	1	None
		MUL.UU Wb, #lit5, Acc ⁽¹⁾	Accumulator = unsigned(Wb) * unsigned(lit5)	1	1	None
		MUL.UU Wb, Ws, Acc ⁽¹⁾	Accumulator = unsigned(Wb) * unsigned(Ws)	1	1	None
		MULW.SS Wb, Ws, Wnd	Wnd = signed(Wb) * signed(Ws)	1	1	None
		MULW.SU Wb, Ws, Wnd	Wnd = signed(Wb) * unsigned(Ws)	1	1	None
		MULW.US Wb, Ws, Wnd	Wnd = unsigned(Wb) * signed(Ws)	1	1	None
		MULW.UU Wb, Ws, Wnd	Wnd = unsigned(Wb) * unsigned(Ws)	1	1	None
		MUL.SU Wb, #lit5, Wnd	{Wnd + 1, Wnd} = signed(Wb) * unsigned(lit5)	1	1	None
		MUL.SU Wb, #lit5, Wnd	Wnd = signed(Wb) * unsigned(lit5)	1	1	None
		MUL.UU Wb, #lit5, Wnd	{Wnd + 1, Wnd} = unsigned(Wb) * unsigned(lit5)	1	1	None
		MUL.UU Wb, #lit5, Wnd	Wnd = unsigned(Wb) * unsigned(lit5)	1	1	None
		MUL f	W3:W2 = f * WREG	1	1	None

Note 1: These instructions are available in dsPIC33EPXXXMC20X/50X and PIC24EPXXXMC20X devices only.

2: Read and Read-Modify-Write (e.g., bit operations and logical operations) on non-CPU SFRs incur an additional instruction cycle.

TABLE 28-2: INSTRUCTION SET OVERVIEW (CONTINUED)

Base Instr #	Assembly Mnemonic	Assembly Syntax	Description	# of Words	# of Cycles ⁽²⁾	Status Flags Affected
53	NEG	NEG <i>Acc</i> ⁽¹⁾	Negate Accumulator	1	1	OA,OB,OAB,SA,SB,SAB
		NEG <i>f</i>	$f = \bar{f} + 1$	1	1	C,DC,N,OV,Z
		NEG <i>f</i> , WREG	WREG = $\bar{f} + 1$	1	1	C,DC,N,OV,Z
		NEG <i>Ws</i> , <i>Wd</i>	$Wd = \bar{Ws} + 1$	1	1	C,DC,N,OV,Z
54	NOP	NOP	No Operation	1	1	None
		NOPR	No Operation	1	1	None
55	POP	POP <i>f</i>	Pop <i>f</i> from Top-of-Stack (TOS)	1	1	None
		POP <i>Wdo</i>	Pop from Top-of-Stack (TOS) to <i>Wdo</i>	1	1	None
		POP.D <i>Wnd</i>	Pop from Top-of-Stack (TOS) to <i>W(nd):W(nd + 1)</i>	1	2	None
		POP.S	Pop Shadow Registers	1	1	All
56	PUSH	PUSH <i>f</i>	Push <i>f</i> to Top-of-Stack (TOS)	1	1	None
		PUSH <i>Wso</i>	Push <i>Wso</i> to Top-of-Stack (TOS)	1	1	None
		PUSH.D <i>Wns</i>	Push <i>W(ns):W(ns + 1)</i> to Top-of-Stack (TOS)	1	2	None
		PUSH.S	Push Shadow Registers	1	1	None
57	PWRSV	PWRSV <i>#lit1</i>	Go into Sleep or Idle mode	1	1	WDTO,Sleep
58	RCALL	RCALL <i>Expr</i>	Relative Call	1	4	SFA
		RCALL <i>Wn</i>	Computed Call	1	4	SFA
59	REPEAT	REPEAT <i>#lit15</i>	Repeat Next Instruction <i>lit15 + 1</i> times	1	1	None
		REPEAT <i>Wn</i>	Repeat Next Instruction (<i>Wn</i>) + 1 times	1	1	None
60	RESET	RESET	Software device Reset	1	1	None
61	RETFIE	RETFIE	Return from interrupt	1	6 (5)	SFA
62	RETLW	RETLW <i>#lit10, Wn</i>	Return with literal in <i>Wn</i>	1	6 (5)	SFA
63	RETURN	RETURN	Return from Subroutine	1	6 (5)	SFA
64	RLC	RLC <i>f</i>	$f = \text{Rotate Left through Carry } f$	1	1	C,N,Z
		RLC <i>f</i> , WREG	WREG = Rotate Left through Carry <i>f</i>	1	1	C,N,Z
		RLC <i>Ws</i> , <i>Wd</i>	$Wd = \text{Rotate Left through Carry } Ws$	1	1	C,N,Z
65	RLNC	RLNC <i>f</i>	$f = \text{Rotate Left (No Carry) } f$	1	1	N,Z
		RLNC <i>f</i> , WREG	WREG = Rotate Left (No Carry) <i>f</i>	1	1	N,Z
		RLNC <i>Ws</i> , <i>Wd</i>	$Wd = \text{Rotate Left (No Carry) } Ws$	1	1	N,Z
66	RRC	RRC <i>f</i>	$f = \text{Rotate Right through Carry } f$	1	1	C,N,Z
		RRC <i>f</i> , WREG	WREG = Rotate Right through Carry <i>f</i>	1	1	C,N,Z
		RRC <i>Ws</i> , <i>Wd</i>	$Wd = \text{Rotate Right through Carry } Ws$	1	1	C,N,Z
67	RRNC	RRNC <i>f</i>	$f = \text{Rotate Right (No Carry) } f$	1	1	N,Z
		RRNC <i>f</i> , WREG	WREG = Rotate Right (No Carry) <i>f</i>	1	1	N,Z
		RRNC <i>Ws</i> , <i>Wd</i>	$Wd = \text{Rotate Right (No Carry) } Ws$	1	1	N,Z
68	SAC	SAC <i>Acc, #Slit4, Wdo</i> ⁽¹⁾	Store Accumulator	1	1	None
		SAC.R <i>Acc, #Slit4, Wdo</i> ⁽¹⁾	Store Rounded Accumulator	1	1	None
69	SE	SE <i>Ws</i> , <i>Wnd</i>	<i>Wnd</i> = sign-extended <i>Ws</i>	1	1	C,N,Z
70	SETM	SETM <i>f</i>	$f = 0xFFFF$	1	1	None
		SETM WREG	WREG = 0xFFFF	1	1	None
		SETM <i>Ws</i>	$Ws = 0xFFFF$	1	1	None
71	SFTAC	SFTAC <i>Acc, Wn</i> ⁽¹⁾	Arithmetic Shift Accumulator by (<i>Wn</i>)	1	1	OA,OB,OAB,SA,SB,SAB
		SFTAC <i>Acc, #Slit6</i> ⁽¹⁾	Arithmetic Shift Accumulator by <i>Slit6</i>	1	1	OA,OB,OAB,SA,SB,SAB

Note 1: These instructions are available in dsPIC33EPXXXMC20X/50X and PIC24EPXXXMC20X devices only.

2: Read and Read-Modify-Write (e.g., bit operations and logical operations) on non-CPU SFRs incur an additional instruction cycle.

29.11 Demonstration/Development Boards, Evaluation Kits and Starter Kits

A wide variety of demonstration, development and evaluation boards for various PIC MCUs and dsPIC DSCs allows quick application development on fully functional systems. Most boards include prototyping areas for adding custom circuitry and provide application firmware and source code for examination and modification.

The boards support a variety of features, including LEDs, temperature sensors, switches, speakers, RS-232 interfaces, LCD displays, potentiometers and additional EEPROM memory.

The demonstration and development boards can be used in teaching environments, for prototyping custom circuits and for learning about various microcontroller applications.

In addition to the PICDEM™ and dsPICDEM™ demonstration/development board series of circuits, Microchip has a line of evaluation kits and demonstration software for analog filter design, KEELOQ® security ICs, CAN, IrDA®, PowerSmart battery management, SEEVAL® evaluation system, Sigma-Delta ADC, flow rate sensing, plus many more.

Also available are starter kits that contain everything needed to experience the specified device. This usually includes a single application and debug capability, all on one board.

Check the Microchip web page (www.microchip.com) for the complete list of demonstration, development and evaluation kits.

29.12 Third-Party Development Tools

Microchip also offers a great collection of tools from third-party vendors. These tools are carefully selected to offer good value and unique functionality.

- Device Programmers and Gang Programmers from companies, such as SoftLog and CCS
- Software Tools from companies, such as Gimpel and Trace Systems
- Protocol Analyzers from companies, such as Saleae and Total Phase
- Demonstration Boards from companies, such as MikroElektronika, Digilent® and Olimex
- Embedded Ethernet Solutions from companies, such as EZ Web Lynx, WIZnet and IPLogika®

FIGURE 30-2: EXTERNAL CLOCK TIMING

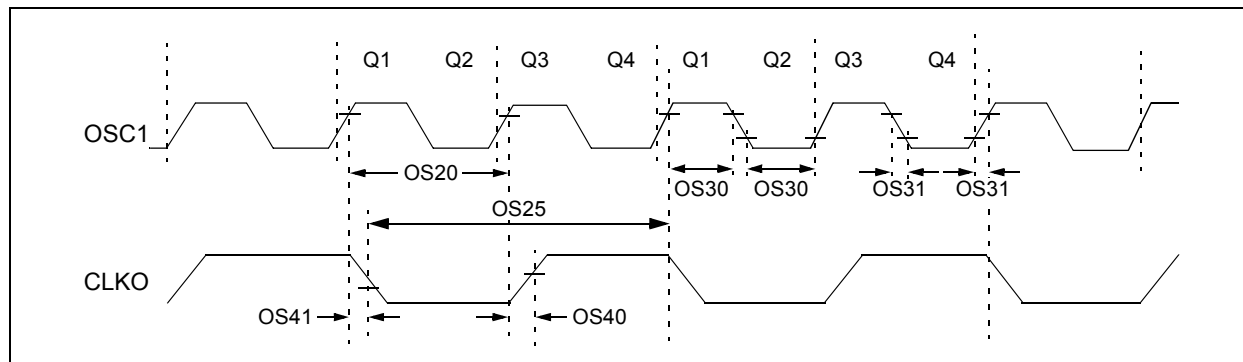


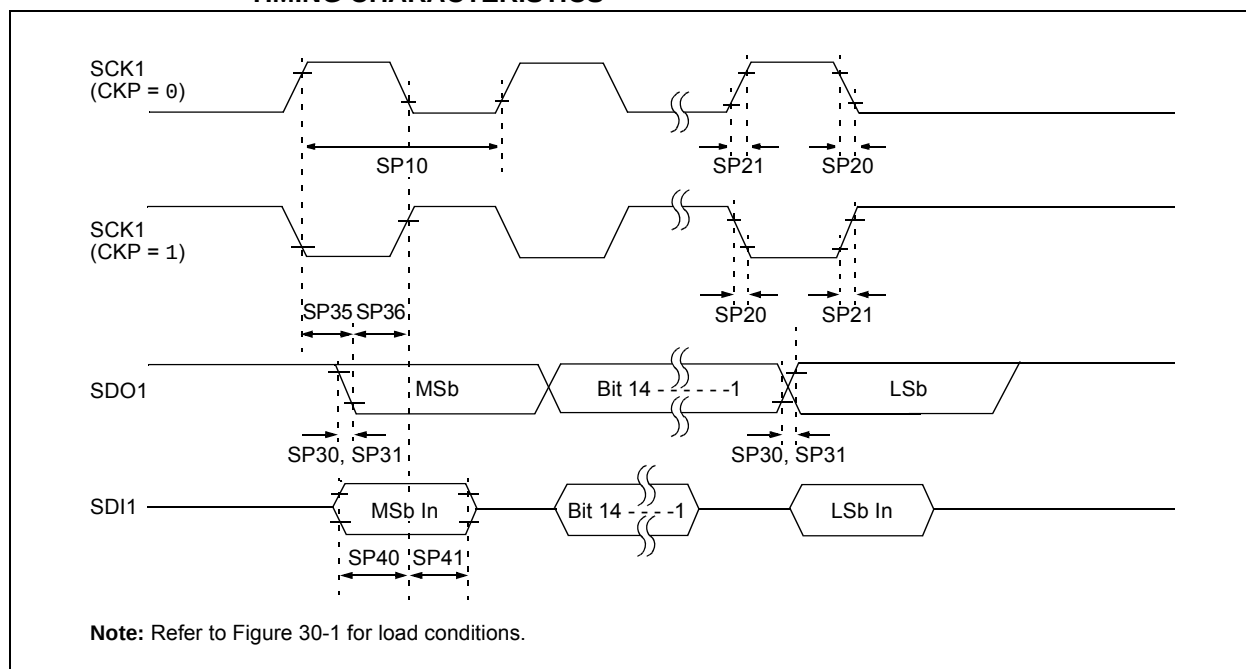
TABLE 30-17: EXTERNAL CLOCK TIMING REQUIREMENTS

AC CHARACTERISTICS			Standard Operating Conditions: 3.0V to 3.6V (unless otherwise stated) Operating temperature -40°C ≤ TA ≤ +85°C for Industrial -40°C ≤ TA ≤ +125°C for Extended				
Param No.	Symb	Characteristic	Min.	Typ. ⁽¹⁾	Max.	Units	Conditions
OS10	FIN	External CLKI Frequency (External clocks allowed only in EC and ECPLL modes)	DC	—	60	MHz	EC
		Oscillator Crystal Frequency	3.5 10	— —	10 25	MHz MHz	XT HS
OS20	Tosc	Tosc = 1/Fosc	8.33	—	DC	ns	+125°C
		Tosc = 1/Fosc	7.14	—	DC	ns	+85°C
OS25	Tcy	Instruction Cycle Time ⁽²⁾	16.67	—	DC	ns	+125°C
		Instruction Cycle Time ⁽²⁾	14.28	—	DC	ns	+85°C
OS30	TosL, TosH	External Clock in (OSC1) High or Low Time	0.45 x Tosc	—	0.55 x Tosc	ns	EC
OS31	TosR, TosF	External Clock in (OSC1) Rise or Fall Time	—	—	20	ns	EC
OS40	TckR	CLKO Rise Time ^(3,4)	—	5.2	—	ns	
OS41	TckF	CLKO Fall Time ^(3,4)	—	5.2	—	ns	
OS42	GM	External Oscillator Transconductance ⁽⁴⁾	—	12	—	mA/V	HS, VDD = 3.3V, TA = +25°C
			—	6	—	mA/V	XT, VDD = 3.3V, TA = +25°C

Note 1: Data in “Typical” column is at 3.3V, +25°C unless otherwise stated.

- 2:** Instruction cycle period (Tcy) equals two times the input oscillator time base period. All specified values are based on characterization data for that particular oscillator type under standard operating conditions with the device executing code. Exceeding these specified limits may result in an unstable oscillator operation and/or higher than expected current consumption. All devices are tested to operate at “Minimum” values with an external clock applied to the OSC1 pin. When an external clock input is used, the “Maximum” cycle time limit is “DC” (no clock) for all devices.
- 3:** Measurements are taken in EC mode. The CLKO signal is measured on the OSC2 pin.
- 4:** This parameter is characterized, but not tested in manufacturing.

**FIGURE 30-25: SPI1 MASTER MODE (FULL-DUPLEX, CKE = 0, CKP = x, SMP = 1)
TIMING CHARACTERISTICS**



**TABLE 30-44: SPI1 MASTER MODE (FULL-DUPLEX, CKE = 0, CKP = x, SMP = 1)
TIMING REQUIREMENTS**

AC CHARACTERISTICS			Standard Operating Conditions: 3.0V to 3.6V (unless otherwise stated) Operating temperature -40°C ≤ TA ≤ +85°C for Industrial -40°C ≤ TA ≤ +125°C for Extended				
Param.	Symbol	Characteristic ⁽¹⁾	Min.	Typ. ⁽²⁾	Max.	Units	Conditions
SP10	FscP	Maximum SCK1 Frequency	—	—	10	MHz	-40°C to +125°C (Note 3)
SP20	TscF	SCK1 Output Fall Time	—	—	—	ns	See Parameter DO32 (Note 4)
SP21	TscR	SCK1 Output Rise Time	—	—	—	ns	See Parameter DO31 (Note 4)
SP30	TdoF	SDO1 Data Output Fall Time	—	—	—	ns	See Parameter DO32 (Note 4)
SP31	TdoR	SDO1 Data Output Rise Time	—	—	—	ns	See Parameter DO31 (Note 4)
SP35	Tsch2doV, TscL2doV	SDO1 Data Output Valid after SCK1 Edge	—	6	20	ns	
SP36	TdoV2scH, TdoV2scL	SDO1 Data Output Setup to First SCK1 Edge	30	—	—	ns	
SP40	TdiV2scH, TdiV2scL	Setup Time of SDI1 Data Input to SCK1 Edge	30	—	—	ns	
SP41	Tsch2diL, TscL2diL	Hold Time of SDI1 Data Input to SCK1 Edge	30	—	—	ns	

Note 1: These parameters are characterized, but are not tested in manufacturing.

Note 2: Data in "Typical" column is at 3.3V, +25°C unless otherwise stated.

Note 3: The minimum clock period for SCK1 is 100 ns. The clock generated in Master mode must not violate this specification.

Note 4: Assumes 50 pF load on all SPI1 pins.

TABLE 30-53: OP AMP/COMPARATOR SPECIFICATIONS (CONTINUED)

DC CHARACTERISTICS			Standard Operating Conditions: 3.0V to 3.6V (unless otherwise stated) ⁽¹⁾ Operating temperature -40°C ≤ TA ≤ +85°C for Industrial -40°C ≤ TA ≤ +125°C for Extended				
Param No.	Symbol	Characteristic	Min.	Typ. ⁽²⁾	Max.	Units	Conditions
Op Amp DC Characteristics							
CM40	VCMR	Common-Mode Input Voltage Range	AVSS	—	AVDD	V	
CM41	CMRR	Common-Mode Rejection Ratio ⁽³⁾	—	40	—	db	VCM = AVDD/2
CM42	VOFFSET	Op Amp Offset Voltage ⁽³⁾	—	±5	—	mV	
CM43	VGAIN	Open-Loop Voltage Gain ⁽³⁾	—	90	—	db	
CM44	IOS	Input Offset Current	—	—	—	—	See pad leakage currents in Table 30-11
CM45	IB	Input Bias Current	—	—	—	—	See pad leakage currents in Table 30-11
CM46	IOUT	Output Current	—	—	420	μA	With minimum value of RFEEDBACK (CM48)
CM48	RFEEDBACK	Feedback Resistance Value	8	—	—	kΩ	
CM49a	VOADC	Output Voltage Measured at OAx Using ADC ^(3,4)	AVSS + 0.077 AVSS + 0.037 AVSS + 0.018	— — —	AVDD – 0.077 AVDD – 0.037 AVDD – 0.018	V V V	IOUT = 420 μA IOUT = 200 μA IOUT = 100 μA
CM49b	VOOUT	Output Voltage Measured at OAxOUT Pin ^(3,4,5)	AVSS + 0.210 AVSS + 0.100 AVSS + 0.050	— — —	AVDD – 0.210 AVDD – 0.100 AVDD – 0.050	V V V	IOUT = 420 μA IOUT = 200 μA IOUT = 100 μA
CM51	RINT1 ⁽⁶⁾	Internal Resistance 1 (Configuration A and B) ^(3,4,5)	198	264	317	Ω	Min = -40°C Typ = +25°C Max = +125°C

Note 1: Device is functional at VBORMIN < VDD < VDDMIN, but will have degraded performance. Device functionality is tested, but not characterized. Analog modules (ADC, op amp/comparator and comparator voltage reference) may have degraded performance. Refer to Parameter BO10 in Table 30-13 for the minimum and maximum BOR values.

2: Data in “Typ” column is at 3.3V, +25°C unless otherwise stated.

3: Parameter is characterized but not tested in manufacturing.

4: See Figure 25-6 for configuration information.

5: See Figure 25-7 for configuration information.

6: Resistances can vary by ±10% between op amps.