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### What is "[Embedded - Microcontrollers](#)"?

"[Embedded - Microcontrollers](#)" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

### Applications of "[Embedded - Microcontrollers](#)"

#### Details

Product Status	Active
Core Processor	PIC
Core Size	16-Bit
Speed	60 MIPS
Connectivity	I <sup>2</sup> C, IrDA, LINbus, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, DMA, POR, PWM, WDT
Number of I/O	21
Program Memory Size	512KB (170K x 24)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	24K x 16
Voltage - Supply (Vcc/Vdd)	3V ~ 3.6V
Data Converters	A/D 6x10b/12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 150°C (TA)
Mounting Type	Surface Mount
Package / Case	28-VQFN Exposed Pad
Supplier Device Package	28-QFN-S (6x6)
Purchase URL	<a href="https://www.e-xfl.com/product-detail/microchip-technology/pic24ep512gp202-h-mm">https://www.e-xfl.com/product-detail/microchip-technology/pic24ep512gp202-h-mm</a>

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**TABLE 4-24: CRC REGISTER MAP**

File Name	Addr.	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	All Resets
CRCCON1	0640	CRCEN	—	CSIDL	VWORD<4:0>					CRCFUL	CRCMPT	CRCISEL	CRCGO	LENDIAN	—	—	—	0000
CRCCON2	0642	—	—	—	DWIDTH<4:0>					—	—	—	PLEN<4:0>					0000
CRCXORL	0644	X<15:1>															—	0000
CRCXORH	0646	X<31:16>															0000	
CRCDATL	0648	CRC Data Input Low Word															0000	
CRCDATH	064A	CRC Data Input High Word															0000	
CRCWDATL	064C	CRC Result Low Word															0000	
CRCWDATH	064E	CRC Result High Word															0000	

**Legend:** — = unimplemented, read as '0'. Shaded bits are not used in the operation of the programmable CRC module.

**TABLE 4-25: PERIPHERAL PIN SELECT OUTPUT REGISTER MAP FOR dsPIC33EPXXXGP/MC202/502 AND PIC24EPXXXGP/MC202 DEVICES ONLY**

File Name	Addr.	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	All Resets
RPOR0	0680	—	—	RP35R<5:0>						—	—	RP20R<5:0>						0000
RPOR1	0682	—	—	RP37R<5:0>						—	—	RP36R<5:0>						0000
RPOR2	0684	—	—	RP39R<5:0>						—	—	RP38R<5:0>						0000
RPOR3	0686	—	—	RP41R<5:0>						—	—	RP40R<5:0>						0000
RPOR4	0688	—	—	RP43R<5:0>						—	—	RP42R<5:0>						0000

**Legend:** — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

**TABLE 4-26: PERIPHERAL PIN SELECT OUTPUT REGISTER MAP FOR dsPIC33EPXXXGP/MC203/503 AND PIC24EPXXXGP/MC203 DEVICES ONLY**

File Name	Addr.	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	All Resets
RPOR0	0680	—	—	RP35R<5:0>						—	—	RP20R<5:0>						0000
RPOR1	0682	—	—	RP37R<5:0>						—	—	RP36R<5:0>						0000
RPOR2	0684	—	—	RP39R<5:0>						—	—	RP38R<5:0>						0000
RPOR3	0686	—	—	RP41R<5:0>						—	—	RP40R<5:0>						0000
RPOR4	0688	—	—	RP43R<5:0>						—	—	RP42R<5:0>						0000
RPOR5	068A	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
RPOR6	068C	—	—	—	—	—	—	—	—	—	—	RP56R<5:0>						0000

**Legend:** — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

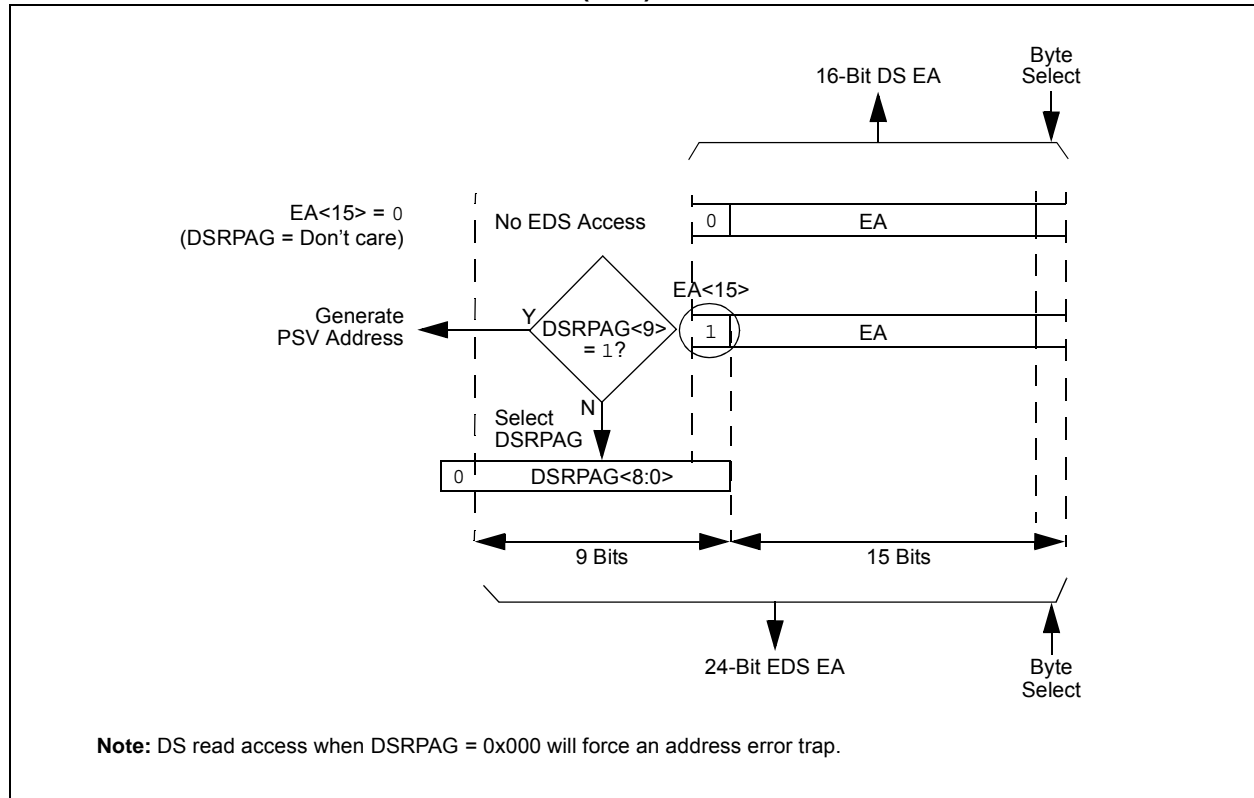
#### 4.4.1 PAGED MEMORY SCHEME

The dsPIC33EPXXXGP50X, dsPIC33EPXXXMC20X/50X and PIC24EPXXXGP/MC20X architecture extends the available Data Space through a paging scheme, which allows the available Data Space to be accessed using MOV instructions in a linear fashion for pre-modified and post-modified Effective Addresses (EA). The upper half of the base Data Space address is used in conjunction with the Data Space Page registers, the 10-bit Read Page register (DSRPAG) or the 9-bit Write Page register (DSWPAG), to form an Extended Data Space (EDS)

address or Program Space Visibility (PSV) address. The Data Space Page registers are located in the SFR space.

Construction of the EDS address is shown in Example 4-1. When DSRPAG<9> = 0 and the base address bit, EA<15> = 1, the DSRPAG<8:0> bits are concatenated onto EA<14:0> to form the 24-bit EDS read address. Similarly, when base address bit, EA<15> = 1, DSWPAG<8:0> are concatenated onto EA<14:0> to form the 24-bit EDS write address.

#### EXAMPLE 4-1: EXTENDED DATA SPACE (EDS) READ ADDRESS GENERATION



## 4.8 Interfacing Program and Data Memory Spaces

The dsPIC33EPXXXGP50X, dsPIC33EPXXXMC20X/50X and PIC24EPXXXGP/MC20X architecture uses a 24-bit-wide Program Space (PS) and a 16-bit-wide Data Space (DS). The architecture is also a modified Harvard scheme, meaning that data can also be present in the Program Space. To use this data successfully, it must be accessed in a way that preserves the alignment of information in both spaces.

Aside from normal execution, the architecture of the dsPIC33EPXXXGP50X, dsPIC33EPXXXMC20X/50X and PIC24EPXXXGP/MC20X devices provides two methods by which Program Space can be accessed during operation:

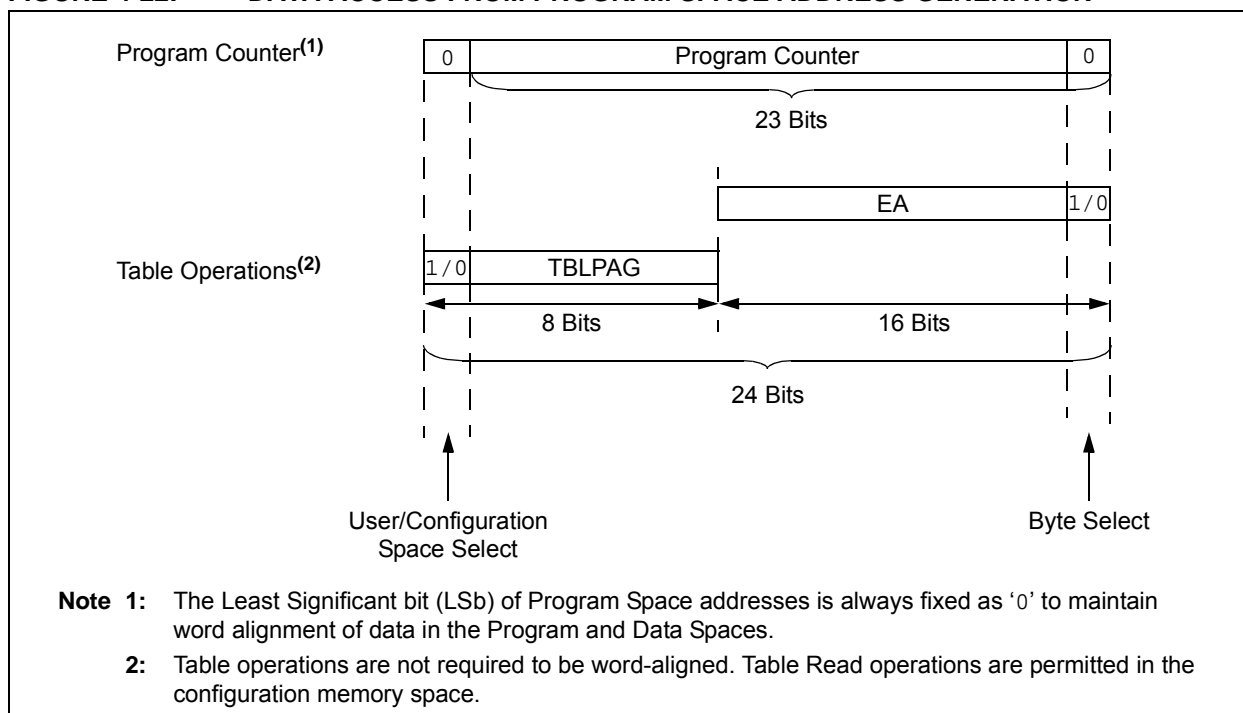
- Using table instructions to access individual bytes or words anywhere in the Program Space
- Remapping a portion of the Program Space into the Data Space (Program Space Visibility)

Table instructions allow an application to read or write to small areas of the program memory. This capability makes the method ideal for accessing data tables that need to be updated periodically. It also allows access to all bytes of the program word. The remapping method allows an application to access a large block of data on a read-only basis, which is ideal for look-ups from a large table of static data. The application can only access the least significant word of the program word.

**TABLE 4-65: PROGRAM SPACE ADDRESS CONSTRUCTION**

Access Type	Access Space	Program Space Address				
		<23>	<22:16>	<15>	<14:1>	<0>
Instruction Access (Code Execution)	User	0	PC<22:1>			0
		0xx   xxxx   xxxx   xxxx   xxxx   xxx0				
TBLRD/TBLWT (Byte/Word Read/Write)	User	TBLPAG<7:0>		Data EA<15:0>		
		0xxx   xxxx		xxxx   xxxx   xxxx   xxxx		
	Configuration	TBLPAG<7:0>		Data EA<15:0>		
		1xxx   xxxx		xxxx   xxxx   xxxx   xxxx		

**FIGURE 4-22: DATA ACCESS FROM PROGRAM SPACE ADDRESS GENERATION**



#### 4.8.1 DATA ACCESS FROM PROGRAM MEMORY USING TABLE INSTRUCTIONS

The **TBLRDH** and **TBLWTL** instructions offer a direct method of reading or writing the lower word of any address within the Program Space without going through Data Space. The **TBLRDH** and **TBLWTL** instructions are the only method to read or write the upper 8 bits of a Program Space word as data.

The PC is incremented by two for each successive 24-bit program word. This allows program memory addresses to directly map to Data Space addresses. Program memory can thus be regarded as two 16-bit-wide word address spaces, residing side by side, each with the same address range. **TBLRDH** and **TBLWTL** access the space that contains the least significant data word. **TBLRDH** and **TBLWTL** access the space that contains the upper data byte.

Two table instructions are provided to move byte or word-sized (16-bit) data to and from Program Space. Both function as either byte or word operations.

- **TBLRDH** (Table Read High):
  - In Word mode, this instruction maps the lower word of the Program Space location ( $P<15:0>$ ) to a data address ( $D<15:0>$ )

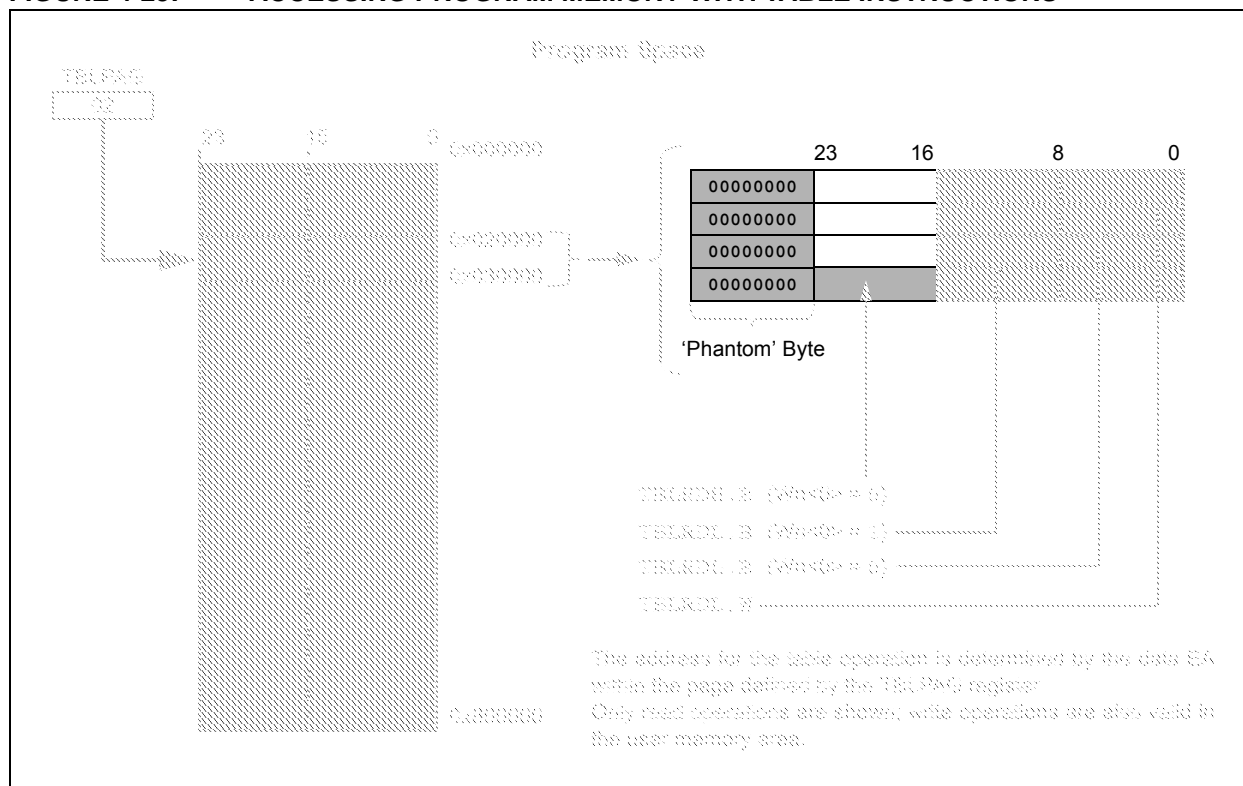
- In Byte mode, either the upper or lower byte of the lower program word is mapped to the lower byte of a data address. The upper byte is selected when Byte Select is '1'; the lower byte is selected when it is '0'.

- **TBLRDH** (Table Read High):
  - In Word mode, this instruction maps the entire upper word of a program address ( $P<23:16>$ ) to a data address. The 'phantom' byte ( $D<15:8>$ ) is always '0'.
  - In Byte mode, this instruction maps the upper or lower byte of the program word to  $D<7:0>$  of the data address in the **TBLRDH** instruction. The data is always '0' when the upper 'phantom' byte is selected (Byte Select = 1).

In a similar fashion, two table instructions, **TBLWTH** and **TBLWTL**, are used to write individual bytes or words to a Program Space address. The details of their operation are explained in **Section 5.0 "Flash Program Memory"**.

For all table operations, the area of program memory space to be accessed is determined by the Table Page register (**TBLPAG**). **TBLPAG** covers the entire program memory space of the device, including user application and configuration spaces. When **TBLPAG<7> = 0**, the table page is located in the user memory space. When **TBLPAG<7> = 1**, the page is located in configuration space.

**FIGURE 4-23: ACCESSING PROGRAM MEMORY WITH TABLE INSTRUCTIONS**



**REGISTER 5-1: NVMCON: NONVOLATILE MEMORY (NVM) CONTROL REGISTER**

R/SO-0 <sup>(1)</sup>	R/W-0 <sup>(1)</sup>	R/W-0 <sup>(1)</sup>	R/W-0	U-0	U-0	U-0	U-0
WR	WREN	WRERR	NVMSIDL <sup>(2)</sup>	—	—	—	—
bit 15				bit 8			

U-0	U-0	U-0	U-0	R/W-0 <sup>(1)</sup>	R/W-0 <sup>(1)</sup>	R/W-0 <sup>(1)</sup>	R/W-0 <sup>(1)</sup>
—	—	—	—	NVMOP3 <sup>(3,4)</sup>	NVMOP2 <sup>(3,4)</sup>	NVMOP1 <sup>(3,4)</sup>	NVMOP0 <sup>(3,4)</sup>
bit 7				bit 0			

<b>Legend:</b>	SO = Settable Only bit
R = Readable bit	W = Writable bit
U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set
	'0' = Bit is cleared
	x = Bit is unknown

- bit 15 **WR:** Write Control bit<sup>(1)</sup>  
 1 = Initiates a Flash memory program or erase operation; the operation is self-timed and the bit is cleared by hardware once the operation is complete  
 0 = Program or erase operation is complete and inactive
- bit 14 **WREN:** Write Enable bit<sup>(1)</sup>  
 1 = Enables Flash program/erase operations  
 0 = Inhibits Flash program/erase operations
- bit 13 **WRERR:** Write Sequence Error Flag bit<sup>(1)</sup>  
 1 = An improper program or erase sequence attempt or termination has occurred (bit is set automatically on any set attempt of the WR bit)  
 0 = The program or erase operation completed normally
- bit 12 **NVMSIDL:** NVM Stop in Idle Control bit<sup>(2)</sup>  
 1 = Flash voltage regulator goes into Standby mode during Idle mode  
 0 = Flash voltage regulator is active during Idle mode
- bit 11-4 **Unimplemented:** Read as '0'
- bit 3-0 **NVMOP<3:0>:** NVM Operation Select bits<sup>(1,3,4)</sup>  
 1111 = Reserved  
 1110 = Reserved  
 1101 = Reserved  
 1100 = Reserved  
 1011 = Reserved  
 1010 = Reserved  
 0011 = Memory page erase operation  
 0010 = Reserved  
 0001 = Memory double-word program operation<sup>(5)</sup>  
 0000 = Reserved

- Note 1:** These bits can only be reset on a POR.
- 2:** If this bit is set, there will be minimal power savings (IDLE) and upon exiting Idle mode, there is a delay (TVREG) before Flash memory becomes operational.
- 3:** All other combinations of NVMOP<3:0> are unimplemented.
- 4:** Execution of the PWRSAV instruction is ignored while any of the NVM operations are in progress.
- 5:** Two adjacent words on a 4-word boundary are programmed during execution of this operation.

**REGISTER 7-3: INTCON1: INTERRUPT CONTROL REGISTER 1 (CONTINUED)**

bit 4	<b>MATHERR:</b> Math Error Status bit 1 = Math error trap has occurred 0 = Math error trap has not occurred
bit 3	<b>ADDRERR:</b> Address Error Trap Status bit 1 = Address error trap has occurred 0 = Address error trap has not occurred
bit 2	<b>STKERR:</b> Stack Error Trap Status bit 1 = Stack error trap has occurred 0 = Stack error trap has not occurred
bit 1	<b>OSCFAIL:</b> Oscillator Failure Trap Status bit 1 = Oscillator failure trap has occurred 0 = Oscillator failure trap has not occurred
bit 0	<b>Unimplemented:</b> Read as '0'

**Note 1:** These bits are available on dsPIC33EPXXXMC20X/50X and dsPIC33EPXXXGP50X devices only.



**REGISTER 9-2: CLKDIV: CLOCK DIVISOR REGISTER (CONTINUED)**

bit 4-0      **PLLPRE<4:0>**: PLL Phase Detector Input Divider Select bits (also denoted as 'N1', PLL prescaler)

11111 = Input divided by 33

•

•

•

00001 = Input divided by 3

00000 = Input divided by 2 (default)

- Note 1:** The DOZE<2:0> bits can only be written to when the DOZEN bit is clear. If DOZEN = 1, any writes to DOZE<2:0> are ignored.
- 2:** This bit is cleared when the ROI bit is set and an interrupt occurs.
- 3:** The DOZEN bit cannot be set if DOZE<2:0> = 000. If DOZE<2:0> = 000, any attempt by user software to set the DOZEN bit is ignored.

### 10.2.1 SLEEP MODE

The following occurs in Sleep mode:

- The system clock source is shut down. If an on-chip oscillator is used, it is turned off.
- The device current consumption is reduced to a minimum, provided that no I/O pin is sourcing current.
- The Fail-Safe Clock Monitor does not operate, since the system clock source is disabled.
- The LPRC clock continues to run in Sleep mode if the WDT is enabled.
- The WDT, if enabled, is automatically cleared prior to entering Sleep mode.
- Some device features or peripherals can continue to operate. This includes items such as the Input Change Notification (ICN) on the I/O ports or peripherals that use an external clock input.
- Any peripheral that requires the system clock source for its operation is disabled.

The device wakes up from Sleep mode on any of these events:

- Any interrupt source that is individually enabled
- Any form of device Reset
- A WDT time-out

On wake-up from Sleep mode, the processor restarts with the same clock source that was active when Sleep mode was entered.

For optimal power savings, the internal regulator and the Flash regulator can be configured to go into Standby when Sleep mode is entered by clearing the VREGS (RCON<8>) and VREGSF (RCON<11>) bits (default configuration).

If the application requires a faster wake-up time, and can accept higher current requirements, the VREGS (RCON<8>) and VREGSF (RCON<11>) bits can be set to keep the internal regulator and the Flash regulator active during Sleep mode.

### 10.2.2 IDLE MODE

The following occurs in Idle mode:

- The CPU stops executing instructions.
- The WDT is automatically cleared.
- The system clock source remains active. By default, all peripheral modules continue to operate normally from the system clock source, but can also be selectively disabled (see **Section 10.4 “Peripheral Module Disable”**).
- If the WDT or FSCM is enabled, the LPRC also remains active.

The device wakes from Idle mode on any of these events:

- Any interrupt that is individually enabled
- Any device Reset
- A WDT time-out

On wake-up from Idle mode, the clock is reapplied to the CPU and instruction execution will begin (2-4 clock cycles later), starting with the instruction following the *PWRSV* instruction or the first instruction in the Interrupt Service Routine (ISR).

All peripherals also have the option to discontinue operation when Idle mode is entered to allow for increased power savings. This option is selectable in the control register of each peripheral; for example, the *TSIDL* bit in the Timer1 Control register (T1CON<13>).

### 10.2.3 INTERRUPTS COINCIDENT WITH POWER SAVE INSTRUCTIONS

Any interrupt that coincides with the execution of a *PWRSV* instruction is held off until entry into Sleep or Idle mode has completed. The device then wakes up from Sleep or Idle mode.

**REGISTER 10-5: PMD6: PERIPHERAL MODULE DISABLE CONTROL REGISTER 6**

U-0	U-0	U-0	U-0	U-0	R/W-0	R/W-0	R/W-0
—	—	—	—	—	PWM3MD <sup>(1)</sup>	PWM2MD <sup>(1)</sup>	PWM1MD <sup>(1)</sup>
bit 15					bit 8		

U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
—	—	—	—	—	—	—	—
bit 7					bit 0		

**Legend:**

R = Readable bit

W = Writable bit

U = Unimplemented bit, read as '0'

-n = Value at POR

'1' = Bit is set

'0' = Bit is cleared

x = Bit is unknown

bit 15-11 **Unimplemented:** Read as '0'

bit 10 **PWM3MD:** PWM3 Module Disable bit<sup>(1)</sup>

1 = PWM3 module is disabled

0 = PWM3 module is enabled

bit 9 **PWM2MD:** PWM2 Module Disable bit<sup>(1)</sup>

1 = PWM2 module is disabled

0 = PWM2 module is enabled

bit 8 **PWM1MD:** PWM1 Module Disable bit<sup>(1)</sup>

1 = PWM1 module is disabled

0 = PWM1 module is enabled

bit 7-0 **Unimplemented:** Read as '0'

**Note 1:** This bit is available on dsPIC33EPXXXMC50X/20X and PIC24EPXXXMC20X devices only.

## 13.2 Timer Control Registers

REGISTER 13-1: TxCON: (TIMER2 AND TIMER4) CONTROL REGISTER

R/W-0	U-0	R/W-0	U-0	U-0	U-0	U-0	U-0
TON	—	TSIDL	—	—	—	—	—
bit 15							bit 8

U-0	R/W-0	R/W-0	R/W-0	R/W-0	U-0	R/W-0	U-0
—	TGATE	TCKPS1	TCKPS0	T32	—	TCS	—
bit 7							bit 0

**Legend:**

R = Readable bit

W = Writable bit

U = Unimplemented bit, read as '0'

-n = Value at POR

'1' = Bit is set

'0' = Bit is cleared

x = Bit is unknown

bit 15 **TON:** Timerx On bit

When T32 = 1:

1 = Starts 32-bit Timerx/y

0 = Stops 32-bit Timerx/y

When T32 = 0:

1 = Starts 16-bit Timerx

0 = Stops 16-bit Timerx

bit 14 **Unimplemented:** Read as '0'

bit 13 **TSIDL:** Timerx Stop in Idle Mode bit

1 = Discontinues module operation when device enters Idle mode

0 = Continues module operation in Idle mode

bit 12-7 **Unimplemented:** Read as '0'

bit 6 **TGATE:** Timerx Gated Time Accumulation Enable bit

When TCS = 1:

This bit is ignored.

When TCS = 0:

1 = Gated time accumulation is enabled

0 = Gated time accumulation is disabled

bit 5-4 **TCKPS<1:0>:** Timerx Input Clock Prescale Select bits

11 = 1:256

10 = 1:64

01 = 1:8

00 = 1:1

bit 3 **T32:** 32-Bit Timer Mode Select bit

1 = Timerx and Timery form a single 32-bit timer

0 = Timerx and Timery act as two 16-bit timers

bit 2 **Unimplemented:** Read as '0'

bit 1 **TCS:** Timerx Clock Source Select bit

1 = External clock is from pin, TxCK (on the rising edge)

0 = Internal clock (Fp)

bit 0 **Unimplemented:** Read as '0'

**REGISTER 14-2: ICxCON2: INPUT CAPTURE x CONTROL REGISTER 2 (CONTINUED)**

bit 4-0 **SYNCSEL<4:0>**: Input Source Select for Synchronization and Trigger Operation bits<sup>(4)</sup>

11111 = No Sync or Trigger source for ICx  
 11110 = Reserved  
 11101 = Reserved  
 11100 = CTMU module synchronizes or triggers ICx  
 11011 = ADC1 module synchronizes or triggers ICx<sup>(5)</sup>  
 11010 = CMP3 module synchronizes or triggers ICx<sup>(5)</sup>  
 11001 = CMP2 module synchronizes or triggers ICx<sup>(5)</sup>  
 11000 = CMP1 module synchronizes or triggers ICx<sup>(5)</sup>  
 10111 = Reserved  
 10110 = Reserved  
 10101 = Reserved  
 10100 = Reserved  
 10011 = IC4 module synchronizes or triggers ICx  
 10010 = IC3 module synchronizes or triggers ICx  
 10001 = IC2 module synchronizes or triggers ICx  
 10000 = IC1 module synchronizes or triggers ICx  
 01111 = Timer5 synchronizes or triggers ICx  
 01110 = Timer4 synchronizes or triggers ICx  
 01101 = Timer3 synchronizes or triggers ICx **(default)**  
 01100 = Timer2 synchronizes or triggers ICx  
 01011 = Timer1 synchronizes or triggers ICx  
 01010 = PTGOx module synchronizes or triggers ICx<sup>(6)</sup>  
 01001 = Reserved  
 01000 = Reserved  
 00111 = Reserved  
 00110 = Reserved  
 00101 = Reserved  
 00100 = OC4 module synchronizes or triggers ICx  
 00011 = OC3 module synchronizes or triggers ICx  
 00010 = OC2 module synchronizes or triggers ICx  
 00001 = OC1 module synchronizes or triggers ICx  
 00000 = No Sync or Trigger source for ICx

- Note 1:** The IC32 bit in both the Odd and Even IC must be set to enable Cascade mode.
- 2:** The input source is selected by the SYNCSEL<4:0> bits of the ICxCON2 register.
- 3:** This bit is set by the selected input source (selected by SYNCSEL<4:0> bits). It can be read, set and cleared in software.
- 4:** Do not use the ICx module as its own Sync or Trigger source.
- 5:** This option should only be selected as a trigger source and not as a synchronization source.
- 6:** Each Input Capture x (ICx) module has one PTG input source. See **Section 24.0 “Peripheral Trigger Generator (PTG) Module”** for more information.
- PTGO8 = IC1  
 PTGO9 = IC2  
 PTGO10 = IC3  
 PTGO11 = IC4

**REGISTER 16-2: PTCON2: PWMx PRIMARY MASTER CLOCK DIVIDER SELECT REGISTER 2**

U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
—	—	—	—	—	—	—	—
bit 15							bit 8

U-0	U-0	U-0	U-0	U-0	R/W-0	R/W-0	R/W-0
—	—	—	—	—	PCLKDIV2 <sup>(1)</sup>	PCLKDIV1 <sup>(1)</sup>	PCLKDIV0 <sup>(1)</sup>
bit 7							bit 0

**Legend:**

R = Readable bit

W = Writable bit

U = Unimplemented bit, read as '0'

-n = Value at POR

'1' = Bit is set

'0' = Bit is cleared

x = Bit is unknown

bit 15-3 **Unimplemented:** Read as '0'

bit 2-0 **PCLKDIV<2:0>:** PWMx Input Clock Prescaler (Divider) Select bits<sup>(1)</sup>

111 = Reserved

110 = Divide-by-64

101 = Divide-by-32

100 = Divide-by-16

011 = Divide-by-8

010 = Divide-by-4

001 = Divide-by-2

000 = Divide-by-1, maximum PWMx timing resolution (power-on default)

**Note 1:** These bits should be changed only when PTEN = 0. Changing the clock selection during operation will yield unpredictable results.

## 20.1 UART Helpful Tips

1. In multi-node, direct-connect UART networks, UART receive inputs react to the complementary logic level defined by the URXINV bit (UxMODE<4>), which defines the Idle state, the default of which is logic high (i.e., URXINV = 0). Because remote devices do not initialize at the same time, it is likely that one of the devices, because the RX line is floating, will trigger a Start bit detection and will cause the first byte received, after the device has been initialized, to be invalid. To avoid this situation, the user should use a pull-up or pull-down resistor on the RX pin depending on the value of the URXINV bit.
  - a) If URXINV = 0, use a pull-up resistor on the RX pin.
  - b) If URXINV = 1, use a pull-down resistor on the RX pin.
2. The first character received on a wake-up from Sleep mode caused by activity on the UxRX pin of the UARTx module will be invalid. In Sleep mode, peripheral clocks are disabled. By the time the oscillator system has restarted and stabilized from Sleep mode, the baud rate bit sampling clock, relative to the incoming UxRX bit timing, is no longer synchronized, resulting in the first character being invalid; this is to be expected.

## 20.2 UART Resources

Many useful resources are provided on the main product page of the Microchip web site for the devices listed in this data sheet. This product page, which can be accessed using this link, contains the latest updates and additional information.

**Note:** In the event you are not able to access the product page using the link above, enter this URL in your browser:  
<http://www.microchip.com/wwwproducts/Devices.aspx?dDocName=en555464>

### 20.2.1 KEY RESOURCES

- “UART” (DS70582) in the “dsPIC33/PIC24 Family Reference Manual”
- Code Samples
- Application Notes
- Software Libraries
- Webinars
- All Related “dsPIC33/PIC24 Family Reference Manual” Sections
- Development Tools

**REGISTER 21-24: CxRXOVF1: ECANx RECEIVE BUFFER OVERFLOW REGISTER 1**

R/C-0	R/C-0	R/C-0	R/C-0	R/C-0	R/C-0	R/C-0	R/C-0
RXOVF15	RXOVF14	RXOVF13	RXOVF12	RXOVF11	RXOVF10	RXOVF9	RXOVF8
bit 15							bit 8

R/C-0	R/C-0	R/C-0	R/C-0	R/C-0	R/C-0	R/C-0	R/C-0
RXOVF7	RXOVF6	RXOVF5	RXOVF4	RXOVF3	RXOVF2	RXOVF1	RXOVF0
bit 7							bit 0

**Legend:** C = Writable bit, but only '0' can be written to clear the bit  
R = Readable bit W = Writable bit U = Unimplemented bit, read as '0'  
-n = Value at POR '1' = Bit is set '0' = Bit is cleared x = Bit is unknown

bit 15-0 **RXOVF<15:0>:** Receive Buffer n Overflow bits  
1 = Module attempted to write to a full buffer (set by module)  
0 = No overflow condition (cleared by user software)

**REGISTER 21-25: CxRXOVF2: ECANx RECEIVE BUFFER OVERFLOW REGISTER 2**

R/C-0	R/C-0	R/C-0	R/C-0	R/C-0	R/C-0	R/C-0	R/C-0
RXOVF31	RXOVF30	RXOVF29	RXOVF28	RXOVF27	RXOVF26	RXOVF25	RXOVF24
bit 15							bit 8

R/C-0	R/C-0	R/C-0	R/C-0	R/C-0	R/C-0	R/C-0	R/C-0
RXOVF23	RXOVF22	RXOVF21	RXOVF20	RXOVF19	RXOVF18	RXOVF17	RXOVF16
bit 7							bit 0

**Legend:** C = Writable bit, but only '0' can be written to clear the bit  
R = Readable bit W = Writable bit U = Unimplemented bit, read as '0'  
-n = Value at POR '1' = Bit is set '0' = Bit is cleared x = Bit is unknown

bit 15-0 **RXOVF<31:16>:** Receive Buffer n Overflow bits  
1 = Module attempted to write to a full buffer (set by module)  
0 = No overflow condition (cleared by user software)



**REGISTER 21-26: CxTRmnCON: ECANx TX/RX BUFFER mn CONTROL REGISTER**  
(m = 0,2,4,6; n = 1,3,5,7)

R/W-0	R-0	R-0	R-0	R/W-0	R/W-0	R/W-0	R/W-0
TXENn	TXABTn	TXLARBn	TXERRn	TXREQn	RTRENn	TXnPRI1	TXnPRI0
bit 15							bit 8

R/W-0	R-0	R-0	R-0	R/W-0	R/W-0	R/W-0	R/W-0
TXENm	TXABTm <sup>(1)</sup>	TXLARBm <sup>(1)</sup>	TXERRm <sup>(1)</sup>	TXREQm	RTRENm	TXmPRI1	TXmPRI0
bit 7							bit 0

**Legend:**

R = Readable bit                      W = Writable bit                      U = Unimplemented bit, read as '0'  
-n = Value at POR                      '1' = Bit is set                      '0' = Bit is cleared                      x = Bit is unknown

bit 15-8                      See Definition for bits<7:0>, Controls Buffer n

bit 7                      **TXENm:** TX/RX Buffer Selection bit

1 = Buffer TRBn is a transmit buffer

0 = Buffer TRBn is a receive buffer

bit 6                      **TXABTm:** Message Aborted bit<sup>(1)</sup>

1 = Message was aborted

0 = Message completed transmission successfully

bit 5                      **TXLARBm:** Message Lost Arbitration bit<sup>(1)</sup>

1 = Message lost arbitration while being sent

0 = Message did not lose arbitration while being sent

bit 4                      **TXERRm:** Error Detected During Transmission bit<sup>(1)</sup>

1 = A bus error occurred while the message was being sent

0 = A bus error did not occur while the message was being sent

bit 3                      **TXREQm:** Message Send Request bit

1 = Requests that a message be sent; the bit automatically clears when the message is successfully sent

0 = Clearing the bit to '0' while set requests a message abort

bit 2                      **RTRENm:** Auto-Remote Transmit Enable bit

1 = When a remote transmit is received, TXREQ will be set

0 = When a remote transmit is received, TXREQ will be unaffected

bit 1-0                      **TXmPRI<1:0>:** Message Transmission Priority bits

11 = Highest message priority

10 = High intermediate message priority

01 = Low intermediate message priority

00 = Lowest message priority

**Note 1:** This bit is cleared when TXREQ is set.

**Note:** The buffers, SID, EID, DLC, Data Field, and Receive Status registers are located in DMA RAM.

**REGISTER 22-2: CTMUCON2: CTMU CONTROL REGISTER 2**

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
EDG1MOD	EDG1POL	EDG1SEL3	EDG1SEL2	EDG1SEL1	EDG1SEL0	EDG2STAT	EDG1STAT
bit 15							bit 8

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	U-0	U-0
EDG2MOD	EDG2POL	EDG2SEL3	EDG2SEL2	EDG2SEL1	EDG2SEL0	—	—
bit 7							bit 0

**Legend:**

R = Readable bit                      W = Writable bit                      U = Unimplemented bit, read as '0'  
-n = Value at POR                      '1' = Bit is set                      '0' = Bit is cleared                      x = Bit is unknown

- bit 15            **EDG1MOD:** Edge 1 Edge Sampling Mode Selection bit  
1 = Edge 1 is edge-sensitive  
0 = Edge 1 is level-sensitive
- bit 14            **EDG1POL:** Edge 1 Polarity Select bit  
1 = Edge 1 is programmed for a positive edge response  
0 = Edge 1 is programmed for a negative edge response
- bit 13-10        **EDG1SEL<3:0>:** Edge 1 Source Select bits  
1xxx = Reserved  
01xx = Reserved  
0011 = CTED1 pin  
0010 = CTED2 pin  
0001 = OC1 module  
0000 = Timer1 module
- bit 9            **EDG2STAT:** Edge 2 Status bit  
Indicates the status of Edge 2 and can be written to control the edge source.  
1 = Edge 2 has occurred  
0 = Edge 2 has not occurred
- bit 8            **EDG1STAT:** Edge 1 Status bit  
Indicates the status of Edge 1 and can be written to control the edge source.  
1 = Edge 1 has occurred  
0 = Edge 1 has not occurred
- bit 7            **EDG2MOD:** Edge 2 Edge Sampling Mode Selection bit  
1 = Edge 2 is edge-sensitive  
0 = Edge 2 is level-sensitive
- bit 6            **EDG2POL:** Edge 2 Polarity Select bit  
1 = Edge 2 is programmed for a positive edge response  
0 = Edge 2 is programmed for a negative edge response
- bit 5-2        **EDG2SEL<3:0>:** Edge 2 Source Select bits  
1111 = Reserved  
01xx = Reserved  
0100 = CMP1 module  
0011 = CTED2 pin  
0010 = CTED1 pin  
0001 = OC1 module  
0000 = IC1 module
- bit 1-0        **Unimplemented:** Read as '0'

**REGISTER 23-5: AD1CHS123: ADC1 INPUT CHANNEL 1, 2, 3 SELECT REGISTER (CONTINUED)**

bit 0

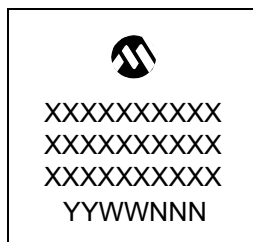
**CH123SA:** Channel 1, 2, 3 Positive Input Select for Sample MUXA bitIn 12-bit mode (AD21B = 1), CH123SA is Unimplemented and is Read as '0':

Value	ADC Channel		
	CH1	CH2	CH3
1 <sup>(2)</sup>	OA1/AN3	OA2/AN0	OA3/AN6
0 <sup>(1,2)</sup>	OA2/AN0	AN1	AN2

- Note 1:** AN0 through AN7 are repurposed when comparator and op amp functionality is enabled. See Figure 23-1 to determine how enabling a particular op amp or comparator affects selection choices for Channels 1, 2 and 3.
- 2:** The OAx input is used if the corresponding op amp is selected (OPMODE (CMxCON<10>) = 1); otherwise, the ANx input is used.

### 33.1 Package Marking Information (Continued)

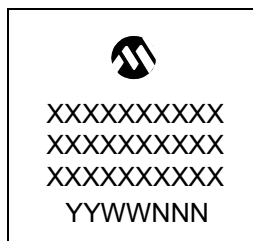
36-Lead VTLA (TLA)



Example



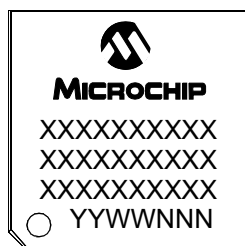
44-Lead VTLA (TLA)



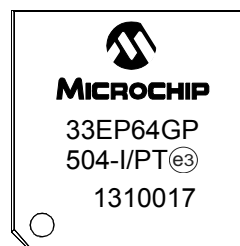
Example



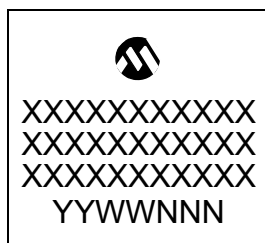
44-Lead TQFP



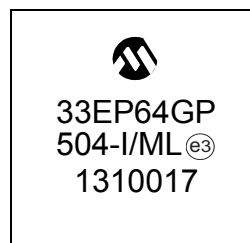
Example



44-Lead QFN (8x8x0.9 mm)



Example



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