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#### Details

Product Status	Active
Core Processor	PIC
Core Size	16-Bit
Speed	60 MIPs
Connectivity	I <sup>2</sup> C, IrDA, LINbus, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, DMA, POR, PWM, WDT
Number of I/O	21
Program Memory Size	512KB (170K x 24)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	24K x 16
Voltage - Supply (Vcc/Vdd)	3V ~ 3.6V
Data Converters	A/D 6x10b/12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 150°C (TA)
Mounting Type	Through Hole
Package / Case	28-DIP (0.300", 7.62mm)
Supplier Device Package	28-SPDIP
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/pic24ep512gp202-h-sp

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## **Pin Diagrams (Continued)**



### Pin Diagrams (Continued)



## Pin Diagrams (Continued)



Pin Name <sup>(4)</sup>	Pin Type	Buffer Type	PPS	Description						
U2CTS	1	ST	No	UART2 Clear-To-Send.						
U2RTS	0		No	UART2 Ready-To-Send.						
U2RX	I.	ST	Yes	UART2 receive.						
U2TX	Ó	_	Yes	UART2 transmit.						
BCLK2	Ō	ST	No	UART2 IrDA <sup>®</sup> baud clock output.						
SCK1	I/O	ST	No	Synchronous serial clock input/output for SPI1.						
SDI1	I	ST	No	SPI1 data in.						
SDO1	0	—	No	SPI1 data out.						
SS1	I/O	ST	No	SPI1 slave synchronization or frame pulse I/O.						
SCK2	I/O	ST	Yes	Synchronous serial clock input/output for SPI2.						
SDI2	I	ST	Yes	SPI2 data in.						
SDO2	0	—	Yes	SPI2 data out.						
SS2	I/O	ST	Yes	SPI2 slave synchronization or frame pulse I/O.						
SCL1	I/O	ST	No	Synchronous serial clock input/output for I2C1.						
SDA1	I/O	ST	No	Synchronous serial data input/output for I2C1.						
ASCL1	I/O	ST	No	Alternate synchronous serial clock input/output for I2C1.						
ASDA1	I/O	ST	No	Alternate synchronous serial data input/output for I2C1.						
SCL2	I/O	ST	No	Synchronous serial clock input/output for I2C2.						
SDA2	I/O	ST	No	Synchronous serial data input/output for I2C2.						
ASCL2	I/O	ST	No	Alternate synchronous serial clock input/output for I2C2.						
ASDA2	I/O	ST	No	Alternate synchronous serial data input/output for I2C2.						
TMS <sup>(5)</sup>	Ι	ST	No	JTAG Test mode select pin.						
TCK	I	ST	No	JTAG test clock input pin.						
TDI	I	ST	No	JTAG test data input pin.						
TDO	0	_	No	JTAG test data output pin.						
C1RX <sup>(2)</sup>	I	ST	Yes	ECAN1 bus receive pin.						
C1TX <sup>(2)</sup>	0	_	Yes	ECAN1 bus transmit pin.						
FLT1 <sup>(1)</sup> , FLT2 <sup>(1)</sup>	I	ST	Yes	PWM Fault Inputs 1 and 2.						
FLT3 <sup>(1)</sup> , FLT4 <sup>(1)</sup>	I	ST	No	PWM Fault Inputs 3 and 4.						
FLT32 <sup>(1,3)</sup>	I	ST	No	PWM Fault Input 32 (Class B Fault).						
DTCMP1-DTCMP3 <sup>(1)</sup>	I	ST	Yes	PWM Dead-Time Compensation Inputs 1 through 3.						
PWM1L-PWM3L <sup>(1)</sup>	0	—	No	PWM Low Outputs 1 through 3.						
PWM1H-PWM3H <sup>(1)</sup>	0	—	No	PWM High Outputs 1 through 3.						
SYNCI1 <sup>(1)</sup>	I	ST	Yes	PWM Synchronization Input 1.						
SYNCO1 <sup>(1)</sup>	0	—	Yes	PWM Synchronization Output 1.						
INDX1 <sup>(1)</sup>	Ι	ST	Yes	Quadrature Encoder Index1 pulse input.						
HOME1 <sup>(1)</sup>	I	ST	Yes	Quadrature Encoder Home1 pulse input.						
QEA1 <sup>(1)</sup>	I	ST	Yes	Quadrature Encoder Phase A input in QEI1 mode. Auxiliary timer						
(4)				external clock/gate input in Timer mode.						
QEB1 <sup>(1)</sup>	I	ST	Yes	Quadrature Encoder Phase B input in QEI1 mode. Auxiliary timer						
				external clock/gate input in Timer mode.						
CNTCMP1''	υ	—	Yes	Quadrature Encoder Compare Output 1.						

## TABLE 1-1: PINOUT I/O DESCRIPTIONS (CONTINUED)

 Legend:
 CMOS = CMOS compatible input or output
 Analog = Analog input

 ST = Schmitt Trigger input with CMOS levels
 O = Output

 PPS = Peripheral Pin Select
 TTL = TTL input buffer

P = Power I = Input

Note 1: This pin is available on dsPIC33EPXXXMC20X/50X and PIC24EPXXXMC20X devices only.

2: This pin is available on dsPIC33EPXXXGP/MC50X devices only.

3: This is the default Fault on Reset for dsPIC33EPXXXMC20X/50X and PIC24EPXXXMC20X devices. See Section 16.0 "High-Speed PWM Module (dsPIC33EPXXXMC20X/50X and PIC24EPXXXMC20X Devices Only)" for more information.

4: Not all pins are available in all packages variants. See the "Pin Diagrams" section for pin availability.

5: There is an internal pull-up resistor connected to the TMS pin when the JTAG interface is active. See the JTAGEN bit field in Table 27-2.

## 3.0 CPU

- Note 1: This data sheet summarizes the features of the dsPIC33EPXXXGP50X. dsPIC33EPXXXMC20X/50X and PIC24EPXXXGP/MC20X families of devices. It is not intended to be a comprehensive reference source. To complement the information in this data sheet, refer to "CPU" (DS70359) in the "dsPIC33/PIC24 Family Reference Manual', which is available from the Microchip web site (www.microchip.com).
  - 2: Some registers and associated bits described in this section may not be available on all devices. Refer to Section 4.0 "Memory Organization" in this data sheet for device-specific register and bit information.

The dsPIC33EPXXXGP50X, dsPIC33EPXXXMC20X/ 50X and PIC24EPXXXGP/MC20X CPU has a 16-bit (data) modified Harvard architecture with an enhanced instruction set, including significant support for digital signal processing. The CPU has a 24-bit instruction word with a variable length opcode field. The Program Counter (PC) is 23 bits wide and addresses up to 4M x 24 bits of user program memory space.

An instruction prefetch mechanism helps maintain throughput and provides predictable execution. Most instructions execute in a single-cycle effective execution rate, with the exception of instructions that change the program flow, the double-word move (MOV.D) instruction, PSV accesses and the table instructions. Overhead-free program loop constructs are supported using the DO and REPEAT instructions, both of which are interruptible at any point.

## 3.1 Registers

The dsPIC33EPXXXGP50X, dsPIC33EPXXXMC20X/ 50X and PIC24EPXXXGP/MC20X devices have sixteen, 16-bit working registers in the programmer's model. Each of the working registers can act as a data, address or address offset register. The 16th working register (W15) operates as a Software Stack Pointer for interrupts and calls.

## 3.2 Instruction Set

The instruction set for dsPIC33EPXXXGP50X and dsPIC33EPXXXMC20X/50X devices has two classes of instructions: the MCU class of instructions and the DSP class of instructions. The instruction set for PIC24EPXXXGP/MC20X devices has the MCU class of instructions only and does not support DSP instructions. These two instruction classes are seamlessly integrated into the architecture and execute from a single execution unit. The instruction set includes many addressing modes and was designed for optimum C compiler efficiency.

## 3.3 Data Space Addressing

The base Data Space can be addressed as 64 Kbytes (32K words).

The Data Space includes two ranges of memory, referred to as X and Y data memory. Each memory range is accessible through its own independent Address Generation Unit (AGU). The MCU class of instructions operates solely through the X memory AGU, which accesses the entire memory map as one linear Data Space. On dsPIC33EPXXXMC20X/50X and dsPIC33EPXXXGP50X devices, certain DSP instructions operate through the X and Y AGUs to support dual operand reads, which splits the data address space into two parts. The X and Y Data Spaces have memory locations that are device-specific, and are described further in the data memory maps in **Section 4.2 "Data Address Space"**.

The upper 32 Kbytes of the Data Space memory map can optionally be mapped into Program Space (PS) at any 32-Kbyte aligned program word boundary. The Program-to-Data Space mapping feature, known as Program Space Visibility (PSV), lets any instruction access Program Space as if it were Data Space. Moreover, the Base Data Space address is used in conjunction with a Read or Write Page register (DSRPAG or DSWPAG) to form an Extended Data Space (EDS) address. The EDS can be addressed as 8M words or 16 Mbytes. Refer to the "**Data Memory**" (DS70595) and "**Program Memory**" (DS70613) sections in the "*dsPIC33/PIC24 Family Reference Manual*" for more details on EDS, PSV and table accesses.

On the dsPIC33EPXXXMC20X/50X and dsPIC33EPXXXGP50X devices, overhead-free circular buffers (Modulo Addressing) are supported in both X and Y address spaces. The Modulo Addressing removes the software boundary checking overhead for DSP algorithms. The X AGU Circular Addressing can be used with any of the MCU class of instructions. The X AGU also supports Bit-Reversed Addressing to greatly simplify input or output data re-ordering for radix-2 FFT algorithms. PIC24EPXXXGP/MC20X devices do not support Modulo and Bit-Reversed Addressing.

## 3.4 Addressing Modes

The CPU supports these addressing modes:

- Inherent (no operand)
- Relative
- Literal
- · Memory Direct
- Register Direct
- Register Indirect

Each instruction is associated with a predefined addressing mode group, depending upon its functional requirements. As many as six addressing modes are supported for each instruction.

File Name	Addr.	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	All Resets
IFS0	0800	—	DMA1IF	AD1IF	U1TXIF	U1RXIF	SPI1IF	SPI1EIF	T3IF	T2IF	OC2IF	IC2IF	DMA0IF	T1IF	OC1IF	IC1IF	<b>INT0IF</b>	0000
IFS1	0802	U2TXIF	U2RXIF	INT2IF	T5IF	T4IF	OC4IF	OC3IF	DMA2IF	_	—	—	INT1IF	CNIF	CMIF	MI2C1IF	SI2C1IF	0000
IFS2	0804	—	—		—		_	—	—	-	IC4IF	IC3IF	DMA3IF	C1IF	C1RXIF	SPI2IF	SPI2EIF	0000
IFS3	0806	—	_		—		QEI1IF	PSEMIF	—		—		—		MI2C2IF	SI2C2IF		0000
IFS4	0808	_	-	CTMUIF	_		—	_	_		C1TXIF		_	CRCIF	U2EIF	U1EIF		0000
IFS5	080A	PWM2IF	PWM1IF	—	—	—	—	—	—	_	—	—	—	_	—	—	_	0000
IFS6	080C	—	—	—	—	—	—	—	—	_	—	—	—	_	—	—	PWM3IF	0000
IFS8	0810	JTAGIF	ICDIF		_		—	_	_		_		_		—	—		0000
IFS9	0812	_	_		_		—	_	_		PTG3IF	PTG2IF	PTG1IF	PTG0IF	PTGWDTIF	PTGSTEPIF		0000
IEC0	0820	—	DMA1IE	AD1IE	U1TXIE	U1RXIE	SPI1IE	SPI1EIE	T3IE	T2IE	OC2IE	IC2IE	DMA0IE	T1IE	OC1IE	IC1IE	INT0IE	0000
IEC1	0822	U2TXIE	U2RXIE	INT2IE	T5IE	T4IE	OC4IE	OC3IE	DMA2IE	_	—	—	INT1IE	CNIE	CMIE	MI2C1IE	SI2C1IE	0000
IEC2	0824	—	—	—	—	—	—	—	—	_	IC4IE	IC3IE	<b>DMA3IE</b>	C1IE	C1RXIE	SPI2IE	SPI2EIE	0000
IEC3	0826	—	—	—	—	—	QEI1IE	PSEMIE	—	_	—	—	—	_	MI2C2IE	SI2C2IE	_	0000
IEC4	0828	—	—	CTMUIE	—	—	—	—	—	_	C1TXIE	—	—	CRCIE	U2EIE	U1EIE	_	0000
IEC5	082A	PWM2IE	PWM1IE	_	—	_	—	—	—	_	—	_	—	_	_	—	_	0000
IEC6	082C	—	—	_	—	_	—	—	—	_	—	_	—	_	_	—	PWM3IE	0000
IEC7	082E	—	—	_	—	_	—	—	—	_	—	_	—	_	—	—	_	0000
IEC8	0830	JTAGIE	ICDIE	_	—	_	—	—	—	_	—	_	—	_	—	—	_	0000
IEC9	0832	—	—	_	—	_	—		—	_	PTG3IE	PTG2IE	PTG1IE	PTG0IE	PTGWDTIE	PTGSTEPIE	_	0000
IPC0	0840	—		T1IP<2:0>		_	OC1IP<2:0>		_	IC1IP<2:0>		_	INT0IP<2:0>			4444		
IPC1	0842	—		T2IP<2:0>		_		OC2IP<2:0	)>	_		IC2IP<2:0>		_	1	DMA0IP<2:0>		4444
IPC2	0844	—		U1RXIP<2:0	)>	_		SPI1IP<2:0	)>	_		SPI1EIP<2:0	>	_		T3IP<2:0>		4444
IPC3	0846	—	—	_	—	_	0	)MA1IP<2:	0>	_		AD1IP<2:0>		_		U1TXIP<2:0>		0444
IPC4	0848			CNIP<2:0>		_		CMIP<2:0	>			MI2C1IP<2:0	>	_	:	SI2C1IP<2:0>		4444
IPC5	084A	—	—	_	—	_	—		—	_	—	_	—	_		INT1IP<2:0>		0004
IPC6	084C	—		T4IP<2:0>		_		OC4IP<2:0	)>	_		OC3IP<2:0>		_	1	DMA2IP<2:0>		4444
IPC7	084E	—		U2TXIP<2:0	>	_	ι	J2RXIP<2:(	0>	_		INT2IP<2:0>		_		T5IP<2:0>		4444
IPC8	0850	—		C1IP<2:0>	-	_	0	C1RXIP<2:(	0>	_		SPI2IP<2:0>		_		SPI2EIP<2:0>		4444
IPC9	0852	—	—	_	—	_		IC4IP<2:0	>	_		IC3IP<2:0>		_	1	DMA3IP<2:0>		0444
IPC12	0858	—	—	_	—	_	N	112C2IP<2:	0>	_		SI2C2IP<2:0	>	_	—	—	_	0440
IPC14	085C	—	_	—	—	—	(	QEI1IP<2:0	)>	_		PSEMIP<2:0	>	—	—	—	—	0440
IPC16	0860	_		CRCIP<2:0	>	_		U2EIP<2:0	>	_		U1EIP<2:0>		_	_	_	_	4440
IPC17	0862	_	—	_	—	_	(	C1TXIP<2:0	0>	_	—	—	—	_	_	_	_	0400
IPC19	0866	—	—	_	—	_	—	—	—	_		CTMUIP<2:0	>	_	—	—	—	0040

## TABLE 4-7: INTERRUPT CONTROLLER REGISTER MAP FOR dsPIC33EPXXXMC50X DEVICES ONLY

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TABLE 4-33:	: PERIPHERAL PIN SELECT INPUT REGISTER MAP FOR dsPIC33EPXXXMC20X DEVIC	ES ONLY
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File Name	Addr.	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	All Resets
RPINR0	06A0	—		INT1R<6:0>							_	—	—	—	—	—	_	0000
RPINR1	06A2	_	_							_				INT2R<6:0>	<b>`</b>			0000
RPINR3	06A6	_								_			-	[2CKR<6:0	>			0000
RPINR7	06AE	_				IC2R<6:0>				_	- IC1R<6:0>							0000
RPINR8	06B0	_		IC4R<6:0>										IC3R<6:0>				0000
RPINR11	06B6	_	_	—	—	—	—	_	—	_	- OCFAR<6:0>							0000
RPINR12	06B8	_		FLT2R<6:0>						_				FLT1R<6:0>	>			0000
RPINR14	06BC	_			(	QEB1R<6:0	>			_			(	QEA1R<6:0	>			0000
RPINR15	06BE	_			Н	OME1R<6:0	)>			_			I	NDX1R<6:0	>			0000
RPINR18	06C4	_	_	_	_	_	_	_	_	_			ι	J1RXR<6:0	>			0000
RPINR19	06C6	_	_	_	_	_	_	_	—	_			ι	J2RXR<6:0	>			0000
RPINR22	06CC	_		•	S	CK2INR<6:0	)>	•	•	_				SDI2R<6:0>	>			0000
RPINR23	06CE	_	_	—	—	—	—	_	—	_				SS2R<6:0>				0000
RPINR37	06EA	_		•	S	YNCI1R<6:0	)>	•	•		—			_	_			0000
RPINR38	06EC	_			D	CMP1R<6:	0>			_	—	_	_	_	_	_	_	0000
RPINR39	06EE	_			D	CMP3R<6:	0>				DTCMP2R<6:0>							0000

**Legend:** — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

REGISTER 5-2: NV	MADRH: NONVOLATILE MEMORY ADDRESS REGISTER HIGH
------------------	---

U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0			
—	—	—	—	—	—	—	_			
bit 15			•	•	•		bit 8			
R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x			
			NVMAD	R<23:16>						
bit 7							bit 0			
Legend:										
R = Readable	bit	W = Writable	bit	U = Unimplemented bit, read as '0'						
-n = Value at F	POR	'1' = Bit is set		'0' = Bit is cle	eared	x = Bit is unknown				
L										

bit 15-8 Unimplemented: Read as '0'

bit 7-0 **NVMADR<23:16>:** Nonvolatile Memory Write Address High bits Selects the upper 8 bits of the location to program or erase in program Flash memory. This register may be read or written by the user application.

#### REGISTER 5-3: NVMADRL: NONVOLATILE MEMORY ADDRESS REGISTER LOW

R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x
			NVMA	DR<15:8>			
bit 15							bit 8
R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x
			NVMA	DR<7:0>			
bit 7							bit 0
Legend:							
R = Readable	bit	W = Writable b	oit	U = Unimpler	mented bit, rea	id as '0'	
-n = Value at F	POR	'1' = Bit is set		'0' = Bit is cle	ared	x = Bit is unkr	nown

bit 15-0 NVMADR<15:0>: Nonvolatile Memory Write Address Low bits

Selects the lower 16 bits of the location to program or erase in program Flash memory. This register may be read or written by the user application.

#### REGISTER 5-4: NVMKEY: NONVOLATILE MEMORY KEY

U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
—	—	—	—	—	—	—	—
bit 15							bit 8
W-0	W-0	W-0	W-0	W-0	W-0	W-0	W-0
			NVMK	EY<7:0>			
bit 7							bit 0
Legend:							
R = Readable	bit	W = Writable	bit	U = Unimple	mented bit, rea	d as '0'	
-n = Value at POR '1' = Bit is set '0' = Bit is cleared x = Bit is unknown							

bit 15-8 Unimplemented: Read as '0'

bit 7-0 **NVMKEY<7:0>:** Key Register (write-only) bits

## 6.0 RESETS

- Note 1: This data sheet summarizes the features of the dsPIC33EPXXXGP50X, dsPIC33EPXXXMC20X/50X and PIC24EPXXXGP/MC20X families of devices. It is not intended to be a comprehensive reference source. To complement the information in this data sheet, refer to "Reset" (DS70602) in the "dsPIC33/PIC24 Family Reference Manual", which is available from the Microchip web site (www.microchip.com).
  - 2: Some registers and associated bits described in this section may not be available on all devices. Refer to Section 4.0 "Memory Organization" in this data sheet for device-specific register and bit information.

The Reset module combines all Reset sources and controls the device Master Reset Signal, SYSRST. The following is a list of device Reset sources:

- · POR: Power-on Reset
- · BOR: Brown-out Reset
- MCLR: Master Clear Pin Reset
- SWR: RESET Instruction
- WDTO: Watchdog Timer Time-out Reset
- CM: Configuration Mismatch Reset
- TRAPR: Trap Conflict Reset
- IOPUWR: Illegal Condition Device Reset
- Illegal Opcode Reset
- Uninitialized W Register Reset
- Security Reset

FIGURE 6-1: RESET SYSTEM BLOCK DIAGRAM

A simplified block diagram of the Reset module is shown in Figure 6-1.

Any active source of Reset will make the SYSRST signal active. On system Reset, some of the registers associated with the CPU and peripherals are forced to a known Reset state and some are unaffected.

Note: Refer to the specific peripheral section or Section 4.0 "Memory Organization" of this manual for register Reset states.

All types of device Reset set a corresponding status bit in the RCON register to indicate the type of Reset (see Register 6-1).

A POR clears all the bits, except for the POR and BOR bits (RCON<1:0>), that are set. The user application can set or clear any bit at any time during code execution. The RCON bits only serve as status bits. Setting a particular Reset status bit in software does not cause a device Reset to occur.

The RCON register also has other bits associated with the Watchdog Timer and device power-saving states. The function of these bits is discussed in other sections of this manual.

**Note:** The status bits in the RCON register should be cleared after they are read so that the next RCON register value after a device Reset is meaningful.

For all Resets, the default clock source is determined by the FNOSC<2:0> bits in the FOSCSEL Configuration register. The value of the FNOSC<2:0> bits is loaded into NOSC<2:0> (OSCCON<10:8>) on Reset, which in turn, initializes the system clock.



# **REGISTER 6-1: RCON: RESET CONTROL REGISTER<sup>(1)</sup> (CONTINUED)**

bit 3	<b>SLEEP:</b> Wake-up from Sleep Flag bit 1 = Device has been in Sleep mode 0 = Device has not been in Sleep mode
bit 2	IDLE: Wake-up from Idle Flag bit
	<ul><li>1 = Device was in Idle mode</li><li>0 = Device was not in Idle mode</li></ul>
bit 1	<b>BOR:</b> Brown-out Reset Flag bit 1 = A Brown-out Reset has occurred 0 = A Brown-out Reset has not occurred
bit 0	<b>POR:</b> Power-on Reset Flag bit 1 = A Power-on Reset has occurred 0 = A Power-on Reset has not occurred

- **Note 1:** All of the Reset status bits can be set or cleared in software. Setting one of these bits in software does not cause a device Reset.
  - 2: If the FWDTEN Configuration bit is '1' (unprogrammed), the WDT is always enabled, regardless of the SWDTEN bit setting.

## dsPIC33EPXXXGP50X, dsPIC33EPXXXMC20X/50X AND PIC24EPXXXGP/MC20X

REGISTER 7-5	INTCON3 INTERRUPT CONTROL REGISTER 3	

U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0				
—	—	—	—	—	—	—	—				
bit 15			•				bit 8				
U-0	U-0	R/W-0	R/W-0	U-0	U-0	U-0	U-0				
	—	DAE	DOOVR	—	—	—	—				
bit 7 bit 0											
Legend:											
R = Readable	bit	W = Writable	bit	U = Unimplemented bit, read as '0'							
-n = Value at I	POR	'1' = Bit is set	:	'0' = Bit is cle	ared	x = Bit is unknown					
bit 15-6	Unimplemen	ted: Read as	'0'								
bit 5	DAE: DMA A	ddress Error S	oft Trap Status	s bit							
	1 = DMA add	ress error soft	trap has occur	red							
	0 = DMA add	ress error soft	trap has not o	ccurred							
bit 4	DOOVR: DO	Stack Overflow	/ Soft Trap Stat	tus bit							
1 = DO stack overflow soft trap has occurred											

	0 = DO stack overflow soft trap has not occurred
~ ~	

## REGISTER 7-6: INTCON4: INTERRUPT CONTROL REGISTER 4

U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
—	—	—	—	—	—	—	_
bit 15							bit 8
U-0	U-0	U-0	U-0	U-0	U-0	U-0	R/W-0
—	—	—	—	—	—	—	SGHT
bit 7							bit 0
Legend:							

R = Readable bit	W = Writable bit	U = Unimplemented bit, read	as '0'
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 0

SGHT: Software Generated Hard Trap Status bit

1 = Software generated hard trap has occurred

0 = Software generated hard trap has not occurred

## dsPIC33EPXXXGP50X, dsPIC33EPXXXMC20X/50X AND PIC24EPXXXGP/MC20X

U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	
_				IC2R<6:0>				
bit 15							bit 8	
U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	
				IC1R<6:0>				
bit 7							bit 0	
Legend:								
R = Readable	bit	W = Writable	bit	U = Unimpler	mented bit, rea	ad as '0'		
-n = Value at F	POR	'1' = Bit is set		'0' = Bit is cle	ared	x = Bit is unknown		
bit 15	Unimplemen	ted: Read as '	0'					
bit 14-8	IC2R<6:0>: A (see Table 11	Assign Input Ca -2 for input pin	pture 2 (IC2) selection nur	to the Correspondent	onding RPn P	in bits		
	1111001 <b>= I</b> r	nput tied to RPI	121					
	0000001 = lr	nput tied to CM	P1					
	nl = 0000000	nput tied to Vss	;					
bit 7	Unimplemen	ted: Read as '	0'					
bit 6-0	IC1R<6:0>: Assign Input Capture 1 (IC1) to the Corresponding RPn Pin bits (see Table 11-2 for input pin selection numbers)							
	1111001 <b>= I</b> r	nput tied to RPI	121					
	•							
	0000001 = lr	nput tied to CM	P1					
	nl = 0000000	nput tied to Vss	;					

#### REGISTER 11-4: RPINR7: PERIPHERAL PIN SELECT INPUT REGISTER 7

NOTES:

NOTES:

#### REGISTER 17-2: QEI1IOC: QEI1 I/O CONTROL REGISTER (CONTINUED)

- bit 2 INDEX: Status of INDXx Input Pin After Polarity Control
  - 1 = Pin is at logic '1'
  - 0 = Pin is at logic '0'
- bit 1 QEB: Status of QEBx Input Pin After Polarity Control And SWPAB Pin Swapping 1 = Pin is at logic '1' 0 = Pin is at logic '0'
- bit 0 **QEA:** Status of QEAx Input Pin After Polarity Control And SWPAB Pin Swapping 1 = Pin is at logic '1'
  - 0 = Pin is at logic '0'

R/W-0	R/W-0	R/W-0	U-0	U-0	U-0	U-0	U-0		
FRMEN	SPIFSD	FRMPOL	—	—	_	—	—		
bit 15							bit 8		
U-0	U-0	U-0	U-0	U-0	U-0	R/W-0	R/W-0		
			_		—	FRMDLY	SPIBEN		
bit 7							bit 0		
Legend:									
R = Readable	e bit	W = Writable I	bit	U = Unimplei	mented bit, reac	l as '0'			
-n = Value at	POR	'1' = Bit is set		'0' = Bit is cle	eared	x = Bit is unkr	nown		
bit 15	FRMEN: Fran	med SPIx Supp	ort bit						
	1 = Framed S 0 = Framed S	<ul> <li>1 = Framed SPIx support is enabled (SSx pin is used as Frame Sync pulse input/output)</li> <li>0 = Framed SPIx support is disabled</li> </ul>							
bit 14	SPIFSD: Fran	me Sync Pulse	Direction Cor	ntrol bit					
	1 = Frame Sy 0 = Frame Sy	/nc pulse input ( /nc pulse outpu	(slave) t (master)						
bit 13	FRMPOL: Fra	ame Sync Pulse	e Polarity bit						
	1 = Frame Sy	/nc pulse is acti	ve-high						
	0 = Frame Sy	/nc pulse is acti	ve-low						
bit 12-2	Unimplemen	ted: Read as 'o	)'						
bit 1 FRMDLY: Frame Sync Pulse Edge Select bit									
	1 = Frame Sy 0 = Frame Sy	/nc pulse coinci /nc pulse prece	des with first des first bit cl	bit clock ock					
bit 0	SPIBEN: Enhanced Buffer Enable bit								
	1 = Enhanceo 0 = Enhanceo	d buffer is enab d buffer is disab	led led (Standard	d mode)					

#### REGISTER 18-3: SPIxCON2: SPIx CONTROL REGISTER 2

NOTES:

## 24.2 PTG Resources

Many useful resources are provided on the main product page of the Microchip web site for the devices listed in this data sheet. This product page, which can be accessed using this link, contains the latest updates and additional information.

Note:	In the event you are not able to access the
	product page using the link above, enter
	this URL in your browser:
	http://www.microchip.com/wwwproducts/
	Devices.aspx?dDocName=en555464

#### 24.2.1 KEY RESOURCES

- "Peripheral Trigger Generator" (DS70669) in the "dsPIC33/PIC24 Family Reference Manual"
- Code Samples
- Application Notes
- · Software Libraries
- Webinars
- All Related "dsPIC33/PIC24 Family Reference Manual" Sections
- Development Tools

DC CHARACTERISTICS			Standard Operating Conditions: 3.0V to 3.6V(unless otherwise stated)Operating temperature $-40^{\circ}C \le TA \le +85^{\circ}C$ for Industrial $-40^{\circ}C \le TA \le +125^{\circ}C$ for Extended						
Param No.	Symbol	Characteristic	Min. Typ. Max. Units Conditions						
DI60a	licl	Input Low Injection Current	0	_	<sub>-5</sub> (4,7)	mA	All pins except VDD, VSS, AVDD, AVSS, MCLR, VCAP and RB7		
DI60b	Іісн	Input High Injection Current	0	_	+5 <sup>(5,6,7)</sup>	mA	All pins except VDD, VSS, AVDD, AVSS, MCLR, VCAP, RB7 and all 5V tolerant pins <sup>(6)</sup>		
DI60c	∑lict	Total Input Injection Current (sum of all I/O and control pins)	-20 <sup>(8)</sup>	_	+20(8)	mA	Absolute instantaneous sum of all $\pm$ input injection cur- rents from all I/O pins (   IICL +   IICH   ) $\leq \sum$ IICT		

## TABLE 30-11: DC CHARACTERISTICS: I/O PIN INPUT SPECIFICATIONS (CONTINUED)

**Note 1:** The leakage current on the MCLR pin is strongly dependent on the applied voltage level. The specified levels represent normal operating conditions. Higher leakage current can be measured at different input voltages.

2: Negative current is defined as current sourced by the pin.

3: See the "Pin Diagrams" section for the 5V tolerant I/O pins.

4: VIL source < (Vss – 0.3). Characterized but not tested.

5: Non-5V tolerant pins VIH source > (VDD + 0.3), 5V tolerant pins VIH source > 5.5V. Characterized but not tested.

6: Digital 5V tolerant pins cannot tolerate any "positive" input injection current from input sources > 5.5V.

7: Non-zero injection currents can affect the ADC results by approximately 4-6 counts.

8: Any number and/or combination of I/O pins not excluded under IICL or IICH conditions are permitted provided the mathematical "absolute instantaneous" sum of the input injection currents from all pins do not exceed the specified limit. Characterized but not tested.

# 36-Terminal Very Thin Thermal Leadless Array Package (TL) – 5x5x0.9 mm Body with Exposed Pad [VTLA]

**Note:** For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



Microchip Technology Drawing C04-187C Sheet 1 of 2