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Details

Product Status	Active
Core Processor	PIC
Core Size	16-Bit
Speed	60 MIPs
Connectivity	I ² C, IrDA, LINbus, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, DMA, POR, PWM, WDT
Number of I/O	35
Program Memory Size	512KB (170K x 24)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	24К х 16
Voltage - Supply (Vcc/Vdd)	3V ~ 3.6V
Data Converters	A/D 9x10b/12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 150°C (TA)
Mounting Type	Surface Mount
Package / Case	44-VFTLA Exposed Pad
Supplier Device Package	44-VTLA (6x6)
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TABLE 4-3: INTERRUPT CONTROLLER REGISTER MAP FOR PIC24EPXXXGP20X DEVICES ONLY

File Name	Addr.	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	All Resets
IFS0	0800	—	DMA1IF	AD1IF	U1TXIF	U1RXIF	SPI1IF	SPI1EIF	T3IF	T2IF	OC2IF	IC2IF	DMA0IF	T1IF	OC1IF	IC1IF	INT0IF	0000
IFS1	0802	U2TXIF	U2RXIF	INT2IF	T5IF	T4IF	OC4IF	OC3IF	DMA2IF	-	—	_	INT1IF	CNIF	CMIF	MI2C1IF	SI2C1IF	0000
IFS2	0804	—	—	—		—	_	_	_		IC4IF	IC3IF	DMA3IF	_	—	SPI2IF	SPI2EIF	0000
IFS3	0806	—	—	—		—	—	_	_		—	—	_	—	MI2C2IF	SI2C2IF	—	0000
IFS4	0808	_	_	CTMUIF		_	_	_	_		—	_	_	CRCIF	U2EIF	U1EIF	_	0000
IFS8	0810	JTAGIF	ICDIF	—	_	—	—	—	—	_	—	—	—	—	—	—	—	0000
IFS9	0812	—	—	—	_	—	—	—	—	_	PTG3IF	PTG2IF	PTG1IF	PTG0IF	PTGWDTIF	PTGSTEPIF	—	0000
IEC0	0820	—	DMA1IE	AD1IE	U1TXIE	U1RXIE	SPI1IE	SPI1EIE	T3IE	T2IE	OC2IE	IC2IE	DMA0IE	T1IE	OC1IE	IC1IE	INT0IE	0000
IEC1	0822	U2TXIE	U2RXIE	INT2IE	T5IE	T4IE	OC4IE	OC3IE	DMA2IE	_	—	—	INT1IE	CNIE	CMIE	MI2C1IE	SI2C1IE	0000
IEC2	0824	—	—	—	_	—	—	—	—	_	IC4IE	IC3IE	DMA3IE	—	—	SPI2IE	SPI2EIE	0000
IEC3	0826	—	—	—	_	—	—	—	—		—	_	—	—	MI2C2IE	SI2C2IE	—	0000
IEC4	0828	—	—	CTMUIE	_	—	—	—	—	_	—	—	—	CRCIE	U2EIE	U1EIE	—	0000
IEC8	0830	JTAGIE	ICDIE	—	_	—	—	—	—		—	_	—	—	—	—	—	0000
IEC9	0832	—	—	—	_	—	—	—	_	_	PTG3IE	PTG2IE	PTG1IE	PTG0IE	PTGWDTIE	PTGSTEPIE	—	0000
IPC0	0840	—		T1IP<2:0>		—		OC1IP<2:0)>	_		IC1IP<2:0>		—		INT0IP<2:0>		4444
IPC1	0842	—		T2IP<2:0>		—		OC2IP<2:0)>			IC2IP<2:0>	C2IP<2:0> — DMA0IP<2:0>			4444		
IPC2	0844	—	ι	J1RXIP<2:0	>	—	:	SPI1IP<2:0)>	_	- SPI1EIP<2:0> T3IP<2:0>		T3IP<2:0>		4444			
IPC3	0846	—	—	—	—	—	0)MA1IP<2:	0>			AD1IP<2:0>	•	—	ι	J1TXIP<2:0>		0444
IPC4	0848	—		CNIP<2:0>		—		CMIP<2:0	>	_		MI2C1IP<2:0	>	—	5	SI2C1IP<2:0>		4444
IPC5	084A	—	—	—	_	—	—	—	—	_	—	—	—	—		INT1IP<2:0>		0004
IPC6	084C	—		T4IP<2:0>		—		OC4IP<2:0)>	_		OC3IP<2:0>	•	—	0	0MA2IP<2:0>		4444
IPC7	084E	—	l	J2TXIP<2:0	>	—	ι	J2RXIP<2:	0>	_		INT2IP<2:0>	>	—		T5IP<2:0>		4444
IPC8	0850	—	—	—	_	—	—	—	—	_		SPI2IP<2:0>	>	—	S	SPI2EIP<2:0>		0044
IPC9	0852	—	—	—	_	—		IC4IP<2:0	>	_		IC3IP<2:0>		—	0	0MA3IP<2:0>		0444
IPC12	0858	—	—	—	_	—	N	112C2IP<2:	0>	_		SI2C2IP<2:0	>	—	—	—	—	0440
IPC16	0860	—		CRCIP<2:0	>	—		U2EIP<2:0	>	_		U1EIP<2:0>		—	—	—	—	4440
IPC19	0866	—	—	—	_	—	—	—	—	_		CTMUIP<2:0	>	—	—	—	—	0040
IPC35	0886	—		JTAGIP<2:0	>	—		ICDIP<2:0	>	_	—	—	—	—	—	—	—	4400
IPC36	0888	—	F	PTG0IP<2:0	>	—	PT	GWDTIP<	2:0>	_	P	TGSTEPIP<2	2:0>	—	—	—	—	4440
IPC37	088A	—	—	—		—	F	PTG3IP<2:	0>			PTG2IP<2:0	>	—	F	PTG1IP<2:0>		0444
INTCON1	08C0	NSTDIS	OVAERR	OVBERR	_	—	—	—	—	_	DIV0ERR	DMACERR	MATHERR	ADDRERR	STKERR	OSCFAIL	—	0000
INTCON2	08C2	GIE	DISI	SWTRAP	_	—	_	—	—	_	—	_	_	—	INT2EP	INT1EP	INT0EP	8000
INTCON3	08C4	_	—	—	_	—	_	—	—	_	—	DAE	DOOVR	—	_	—	—	0000
INTCON4	08C6	—	—	—	—	—	—	—	—	_	—	—	—	—	—	—	SGHT	0000
INTTREG	08C8	_	_	_	—		ILR<	3:0>		VECNUM<7:0>						0000		

- = unimplemented, read as '0'. Reset values are shown in hexadecimal. Legend:

TABLE 4-53: PORTA REGISTER MAP FOR PIC24EPXXXGP/MC204 AND dsPIC33EPXXXGP/MC204/504 DEVICES ONLY

File Name	Addr.	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	All Resets
TRISA	0E00		—	—			TRISA10	TRISA9	TRISA8	TRISA7			TRISA4	TRISA3	TRISA2	TRISA1	TRISA0	079F
PORTA	0E02		—	_			RA10	RA9	RA8	RA7			RA4	RA3	RA2	RA1	RA0	0000
LATA	0E04		—	—	-	-	LATA10	LATA9	LATA8	LATA7	_	-	LATA4	LATA3	LATA2	LA1TA1	LA0TA0	0000
ODCA	0E06	_	_	_	_	_	ODCA10	ODCA9	ODCA8	ODCA7	_	_	ODCA4	ODCA3	ODCA2	ODCA1	ODCA0	0000
CNENA	0E08		—	—			CNIEA10	CNIEA9	CNIEA8	CNIEA7			CNIEA4	CNIEA3	CNIEA2	CNIEA1	CNIEA0	0000
CNPUA	0E0A	_	_	_	_	_	CNPUA10	CNPUA9	CNPUA8	CNPUA7	_	_	CNPUA4	CNPUA3	CNPUA2	CNPUA1	CNPUA0	0000
CNPDA	0E0C	_	_	_	_	_	CNPDA10	CNPDA9	CNPDA8	CNPDA7	_	_	CNPDA4	CNPDA3	CNPDA2	CNPDA1	CNPDA0	0000
ANSELA	0E0E	_	_	_	_	_	_	_	_	_	_	_	ANSA4	_	_	ANSA1	ANSA0	0013

Legend: - = unimplemented, read as '0'. Reset values are shown in hexadecimal.

TABLE 4-54: PORTB REGISTER MAP FOR PIC24EPXXXGP/MC204 AND dsPIC33EPXXXGP/MC204/504 DEVICES ONLY

File Name	Addr.	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	All Resets
TRISB	0E10	TRISB15	TRISB14	TRISB13	TRISB12	TRISB11	TRISB10	TRISB9	TRISB8	TRISB7	TRISB6	TRISB5	TRISB4	TRISB3	TRISB2	TRISB1	TRISB0	FFFF
PORTB	0E12	RB15	RB14	RB13	RB12	RB11	RB10	RB9	RB8	RB7	RB6	RB5	RB4	RB3	RB2	RB1	RB0	xxxx
LATB	0E14	LATB15	LATB14	LATB13	LATB12	LATB11	LATB10	LATB9	LATB8	LATB7	LATB6	LATB5	LATB4	LATB3	LATB2	LATB1	LATB0	xxxx
ODCB	0E16	ODCB15	ODCB14	ODCB13	ODCB12	ODCB11	ODCB10	ODCB9	ODCB8	ODCB7	ODCB6	ODCB5	ODCB4	ODCB3	ODCB2	ODCB1	ODCB0	0000
CNENB	0E18	CNIEB15	CNIEB14	CNIEB13	CNIEB12	CNIEB11	CNIEB10	CNIEB9	CNIEB8	CNIEB7	CNIEB6	CNIEB5	CNIEB4	CNIEB3	CNIEB2	CNIEB1	CNIEB0	0000
CNPUB	0E1A	CNPUB15	CNPUB14	CNPUB13	CNPUB12	CNPUB11	CNPUB10	CNPUB9	CNPUB8	CNPUB7	CNPUB6	CNPUB5	CNPUB4	CNPUB3	CNPUB2	CNPUB1	CNPUB0	0000
CNPDB	0E1C	CNPDB15	CNPDB14	CNPDB13	CNPDB12	CNPDB11	CNPDB10	CNPDB9	CNPDB8	CNPDB7	CNPDB6	CNPDB5	CNPDB4	CNPDB3	CNPDB2	CNPDB1	CNPDB0	0000
ANSELB	0E1E	-	—	—	—	—	—	—	ANSB8	-	—	-	_	ANSB3	ANSB2	ANSB1	ANSB0	010F

Legend: x = unknown value on Reset, — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

TABLE 4-55: PORTC REGISTER MAP FOR PIC24EPXXXGP/MC204 AND dsPIC33EPXXXGP/MC204/504 DEVICES ONLY

File Name	Addr.	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	All Resets
TRISC	0E20	—	—	—	—	—	-	TRISC9	TRISC8	TRISC7	TRISC6	TRISC5	TRISC4	TRISC3	TRISC2	TRISC1	TRISC0	03FF
PORTC	0E22	—	_	—	—	—		RC9	RC8	RC7	RC6	RC5	RC4	RC3	RC2	RC1	RC0	xxxx
LATC	0E24	—	—	—	—	—		LATC9	LATC8	LATC7	LATC6	LATC5	LATC4	LATC3	LATC2	LATC1	LATC0	xxxx
ODCC	0E26	_	_	_	_	_	_	ODCC9	ODCC8	ODCC7	ODCC6	ODCC5	ODCC4	ODCC3	ODCC2	ODCC1	ODCC0	0000
CNENC	0E28	—	—	—	—	—	-	CNIEC9	CNIEC8	CNIEC7	CNIEC6	CNIEC5	CNIEC4	CNIEC3	CNIEC2	CNIEC1	CNIEC0	0000
CNPUC	0E2A	_	_	_	_	_	_	CNPUC9	CNPUC8	CNPUC7	CNPUC6	CNPUC5	CNPUC4	CNPUC3	CNPUC2	CNPUC1	CNPUC0	0000
CNPDC	0E2C	_	_	_	_	_	_	CNPDC9	CNPDC8	CNPDC7	CNPDC6	CNPDC5	CNPDC4	CNPDC3	CNPDC2	CNPDC1	CNPDC0	0000
ANSELC	0E2E	_	_	_	_	_	_	_		_		_	_	_	ANSC2	ANSC1	ANSC0	0007

Legend: x = unknown value on Reset, --- = unimplemented, read as '0'. Reset values are shown in hexadecimal.

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dsPIC33EPXXXGP50X, dsPIC33EPXXXMC20X/50X AND PIC24EPXXXGP/MC20X

R/W-0	U-0	R/W-0	R/W-0	R/W-0	R-0	R-0	R-0
VAR	—	US1	US0	EDT	DL2	DL1	DL0
bit 15							bit 8
R/W-0	R/W-0	R/W-1	R/W-0	R/C-0	R-0	R/W-0	R/W-0
SATA	SATB	SATDW	ACCSAT	IPL3 ⁽²⁾	SFA	RND	IF
bit 7							bit 0

REGISTER 7-2: CORCON: CORE CONTROL REGISTER⁽¹⁾

Legend:	C = Clearable bit		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read	1 as '0'
-n = Value at POR	'1'= Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit

bit 15	VAR: Variable Exception Processing Latency Control
	1 = Variable exception processing is enabled
	0 = Fixed exception processing is enabled
bit 3	IPL3: CPU Interrupt Priority Level Status bit 3 ⁽²⁾
	1 = CPU Interrupt Priority Level is greater than 7
	0 = CPU Interrupt Priority Level is 7 or less

Note 1: For complete register details, see Register 3-2.

2: The IPL3 bit is concatenated with the IPL<2:0> bits (SR<7:5>) to form the CPU Interrupt Priority Level.

11.5 I/O Helpful Tips

- In some cases, certain pins, as defined in Table 30-11, under "Injection Current", have internal protection diodes to VDD and Vss. The term, "Injection Current", is also referred to as "Clamp Current". On designated pins, with sufficient external current-limiting precautions by the user, I/O pin input voltages are allowed to be greater or less than the data sheet absolute maximum ratings, with respect to the Vss and VDD supplies. Note that when the user application forward biases either of the high or low side internal input clamp diodes, that the resulting current being injected into the device, that is clamped internally by the VDD and Vss power rails, may affect the ADC accuracy by four to six counts.
- 2. I/O pins that are shared with any analog input pin (i.e., ANx) are always analog pins by default after any Reset. Consequently, configuring a pin as an analog input pin automatically disables the digital input pin buffer and any attempt to read the digital input level by reading PORTx or LATx will always return a '0', regardless of the digital logic level on the pin. To use a pin as a digital I/O pin on a shared ANx pin, the user application needs to configure the Analog Pin Configuration registers in the I/O ports module (i.e., ANSELx) by setting the appropriate bit that corresponds to that I/O port pin to a '0'.
- **Note:** Although it is not possible to use a digital input pin when its analog function is enabled, it is possible to use the digital I/O output function, TRISx = 0x0, while the analog function is also enabled. However, this is not recommended, particularly if the analog input is connected to an external analog voltage source, which would create signal contention between the analog signal and the output pin driver.
- 3. Most I/O pins have multiple functions. Referring to the device pin diagrams in this data sheet, the priorities of the functions allocated to any pins are indicated by reading the pin name from left-to-right. The left most function name takes precedence over any function to its right in the naming convention. For example: AN16/T2CK/T7CK/RC1. This indicates that AN16 is the highest priority in this example and will supersede all other functions to its right in the list. Those other functions to its right, even if enabled, would not work as long as any other function to its left was enabled. This rule applies to all of the functions listed for a given pin.
- 4. Each pin has an internal weak pull-up resistor and pull-down resistor that can be configured using the CNPUx and CNPDx registers, respectively. These resistors eliminate the need for external resistors in certain applications. The internal pull-up is up to ~(VDD - 0.8), not VDD. This value is still above the minimum VIH of CMOS and TTL devices.

5. When driving LEDs directly, the I/O pin can source or sink more current than what is specified in the VOH/IOH and VOL/IOL DC characteristic specification. The respective IOH and IOL current rating only applies to maintaining the corresponding output at or above the VOH, and at or below the VOL levels. However, for LEDs, unlike digital inputs of an externally connected device, they are not governed by the same minimum VIH/VIL levels. An I/O pin output can safely sink or source any current less than that listed in the absolute maximum rating section of this data sheet. For example:

VOH = 2.4V @ IOH = -8 mA and VDD = 3.3VThe maximum output current sourced by any 8 mA I/O pin = 12 mA.

LED source current < 12 mA is technically permitted. Refer to the VOH/IOH graphs in Section 30.0 "Electrical Characteristics" for additional information.

- 6. The Peripheral Pin Select (PPS) pin mapping rules are as follows:
 - a) Only one "output" function can be active on a given pin at any time, regardless if it is a dedicated or remappable function (one pin, one output).
 - b) It is possible to assign a "remappable output" function to multiple pins and externally short or tie them together for increased current drive.
 - c) If any "dedicated output" function is enabled on a pin, it will take precedence over any remappable "output" function.
 - d) If any "dedicated digital" (input or output) function is enabled on a pin, any number of "input" remappable functions can be mapped to the same pin.
 - e) If any "dedicated analog" function(s) are enabled on a given pin, "digital input(s)" of any kind will all be disabled, although a single "digital output", at the user's cautionary discretion, can be enabled and active as long as there is no signal contention with an external analog input signal. For example, it is possible for the ADC to convert the digital output logic level, or to toggle a digital output on a comparator or ADC input provided there is no external analog input, such as for a built-in self-test.
 - f) Any number of "input" remappable functions can be mapped to the same pin(s) at the same time, including to any pin with a single output from either a dedicated or remappable "output".

16.2 PWM Resources

Many useful resources are provided on the main product page of the Microchip web site for the devices listed in this data sheet. This product page, which can be accessed using this link, contains the latest updates and additional information.

Note:	In the event you are not able to access the
	product page using the link above, enter
	this URL in your browser:
	http://www.microchip.com/wwwproducts/
	Devices.aspx?dDocName=en555464

16.2.1 KEY RESOURCES

- "High-Speed PWM" (DS70645) in the "dsPIC33/PIC24 Family Reference Manual"
- Code Samples
- Application Notes
- · Software Libraries
- Webinars
- All Related "dsPIC33/PIC24 Family Reference Manual" Sections
- Development Tools

17.2 QEI Control Registers

|--|

R/W-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0				
QEIEN		QEISIDL	PIMOD2 ⁽¹⁾	PIMOD1 ⁽¹⁾	PIMOD0 ⁽¹⁾	IMV1 ⁽²⁾	IMV0 ⁽²⁾				
bit 15							bit 8				
U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0				
_	INTDIV2 ⁽³⁾	INTDIV1 ⁽³⁾	INTDIV0 ⁽³⁾	CNTPOL	GATEN	CCM1	CCM0				
bit 7							bit 0				
Legend:											
R = Readable bitW = Writable bitU = Unimplemented bit, read as '0'											
-n = Value at I	POR	'1' = Bit is set		'0' = Bit is cle	ared	x = Bit is unkr	Iown				
bit 15 QEIEN: Quadrature Encoder Interface Module Counter Enable bit 1 = Module counters are enabled 0 = Module counters are disabled, but SFRs can be read or written to											
bit 14	Unimplemented: Read as '0'										
bit 13	QEISIDL: QEI Stop in Idle Mode bit										
	1 = Discontinues	ues module opera module opera	eration when c tion in Idle mo	levice enters I de	dle mode						
bit 12-10	PIMOD<2:0>	: Position Coun	iter Initializatio	n Mode Selec	t bits ⁽¹⁾						
	PIMOD<2:0>: Position Counter Initialization Mode Select bits ⁽¹⁾ 111 = Reserved 100 = Modulo Count mode for position counter 101 = Resets the position counter when the position counter equals QEI1GEC register 100 = Second index event after home event initializes position counter with contents of QEI1IC register 011 = First index event after home event initializes position counter with contents of QEI1IC register 010 = Next index input event initializes the position counter with contents of QEI1IC register 010 = Every index input event resets the position counter 000 = Index input event dese not affect position counter										
bit 9	IMV1: Index N	Match Value for	Phase B bit ⁽²)							
	1 = Phase B match occurs when QEB = 1 0 = Phase B match occurs when QEB = 0										
bit 8	IMV0: Index N	Match Value for	Phase A bit ⁽²⁾)							
	1 = Phase A r 0 = Phase A r	match occurs w match occurs w	/hen QEA = 1 /hen QEA = 0								
bit 7	Unimplemen	ted: Read as '	י)								
	0014.4.0		(II) OF								

Note 1: When CCM<1:0> = 10 or 11, all of the QEI counters operate as timers and the PIMOD<2:0> bits are ignored.

2: When CCM<1:0> = 00, and QEA and QEB values match the Index Match Value (IMV), the POSCNTH and POSCNTL registers are reset. QEA/QEB signals used for the index match have swap and polarity values applied, as determined by the SWPAB and QEAPOL/QEBPOL bits.

3: The selected clock rate should be at least twice the expected maximum quadrature count rate.

19.0 INTER-INTEGRATED CIRCUIT[™] (I²C[™])

- Note 1: This data sheet summarizes the features of the dsPIC33EPXXXGP50X, dsPIC33EPXXXGP50X and PIC24EPXXXGP/MC20X families of devices. It is not intended to be a comprehensive reference source. To complement the information in this data sheet, refer to "Inter-Integrated Circuit™ (I²C™)" (DS70330) in the "dsPIC33/ PIC24 Family Reference Manual", which is available from the Microchip web site (www.microchip.com).
 - 2: Some registers and associated bits described in this section may not be available on all devices. Refer to **Section 4.0 "Memory Organization"** in this data sheet for device-specific register and bit information.
 - 3: There are minimum bit rates of approximately FCY/512. As a result, high processor speeds may not support 100 Kbit/second operation. See timing specifications, IM10 and IM11, and the "Baud Rate Generator" in the "dsPIC33/PIC24 Family Reference Manual".

The dsPIC33EPXXXGP50X, dsPIC33EPXXXMC20X/ 50X and PIC24EPXXXGP/MC20X family of devices contains two Inter-Integrated Circuit (I²C) modules: I2C1 and I2C2.

The l^2C module provides complete hardware support for both Slave and Multi-Master modes of the l^2C serial communication standard, with a 16-bit interface.

The I^2C module has a 2-pin interface:

- · The SCLx pin is clock
- The SDAx pin is data

The I²C module offers the following key features:

- I²C interface supporting both Master and Slave modes of operation
- I²C Slave mode supports 7 and 10-bit addressing
- I²C Master mode supports 7 and 10-bit addressing
- I²C port allows bidirectional transfers between master and slaves
- Serial clock synchronization for I²C port can be used as a handshake mechanism to suspend and resume serial transfer (SCLREL control)
- I²C supports multi-master operation, detects bus collision and arbitrates accordingly
- Intelligent Platform Management Interface (IPMI)
 support
- System Management Bus (SMBus) support

U-0	U-0	U-0	U-0	U-0	U-0	R/W-0	R/W-0
—	—	—	—		—	AMSK9	AMSK8
bit 15							bit 8
R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
AMSK7	AMSK6	AMSK5	AMSK4	AMSK3	AMSK2	AMSK1	AMSK0
bit 7							bit 0

REGISTER 19-3: I2CxMSK: I2Cx SLAVE MODE ADDRESS MASK REGISTER

r			
Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit	t, read as '0'
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15-10 Unimplemented: Read as '0'

bit 9-0

AMSK<9:0>: Address Mask Select bits

For 10-Bit Address:

1 = Enables masking for bit Ax of incoming message address; bit match is not required in this position

0 = Disables masking for bit Ax; bit match is required in this position

For 7-Bit Address (I2CxMSK<6:0> only):

1 = Enables masking for bit Ax + 1 of incoming message address; bit match is not required in this position

0 = Disables masking for bit Ax + 1; bit match is required in this position

dsPIC33EPXXXGP50X, dsPIC33EPXXXMC20X/50X AND PIC24EPXXXGP/MC20X

U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
_	_	_	_	_	_	_	_
bit 15							bit 8
R/W-0	R/W-0	R/W-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0
IVRIE	WAKIE	ERRIE	—	FIFOIE	RBOVIE	RBIE	TBIE
bit 7					·		bit 0
Legend:							
R = Readable	bit	W = Writable	bit	U = Unimpler	mented bit, read	as '0'	
-n = Value at F	POR	'1' = Bit is set		'0' = Bit is cle	ared	x = Bit is unkr	nown
bit 15-8	Unimplemen	ted: Read as ')'				
bit 7	IVRIE: Invalid	I Message Inter	rupt Enable b	bit			
	1 = Interrupt r	equest is enab	led				
		request is not e	nabled				
DIT 6	WAKIE: Bus	vvake-up Activi	ty interrupt Er	Table bit			
	$\perp = \text{Interrupt r}$ 0 = Interrupt r	request is enab	nabled				
bit 5	ERRIE: Frror	Interrupt Enab	le bit				
	1 = Interrupt r	request is enab	led				
	0 = Interrupt r	equest is not e	nabled				
bit 4	Unimplemen	ted: Read as ')'				
bit 3	FIFOIE: FIFO	Almost Full Int	errupt Enable	e bit			
	1 = Interrupt r	request is enab	led				
	0 = Interrupt r	request is not e	nabled				
bit 2	RBOVIE: RX	Buffer Overflov	v Interrupt En	able bit			
	1 = Interrupt request is enabled						
hit 1	BBIE: BX But	ffer Interrunt Fr	nable hit				
bit 1	1 = Interrupt r	request is enab	led				
	0 = Interrupt r	request is not e	nabled				
bit 0	TBIE: TX Buff	fer Interrupt En	able bit				
	1 = Interrupt r	request is enab	led				
	0 = Interrupt r	request is not e	nabled				

REGISTER 21-7: CXINTE: ECANX INTERRUPT ENABLE REGISTER

dsPIC33EPXXXGP50X, dsPIC33EPXXXMC20X/50X AND PIC24EPXXXGP/MC20X

REGISTER 21-22: CxRXFUL1: ECANx RECEIVE BUFFER FULL REGISTER 1

R/C-0	R/C-0	R/C-0	R/C-0	R/C-0	R/C-0	R/C-0	R/C-0
RXFUL15	RXFUL14	RXFUL13	RXFUL12	RXFUL11	RXFUL10	RXFUL9	RXFUL8
bit 15							bit 8

| R/C-0 |
|--------|--------|--------|--------|--------|--------|--------|--------|
| RXFUL7 | RXFUL6 | RXFUL5 | RXFUL4 | RXFUL3 | RXFUL2 | RXFUL1 | RXFUL0 |
| bit 7 | | | | | | | bit 0 |

Legend:	C = Writable bit, but only '0' can be written to clear the bit				
R = Readable bit	W = Writable bit U = Unimplemented bit, read as '0'				
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown		

bit 15-0 **RXFUL<15:0>:** Receive Buffer n Full bits

1 = Buffer is full (set by module)

0 = Buffer is empty (cleared by user software)

REGISTER 21-23: CxRXFUL2: ECANx RECEIVE BUFFER FULL REGISTER 2

| R/C-0 |
|---------|---------|---------|---------|---------|---------|---------|---------|
| RXFUL31 | RXFUL30 | RXFUL29 | RXFUL28 | RXFUL27 | RXFUL26 | RXFUL25 | RXFUL24 |
| bit 15 | | | | | | | bit 8 |

| R/C-0 |
|---------|---------|---------|---------|---------|---------|---------|---------|
| RXFUL23 | RXFUL22 | RXFUL21 | RXFUL20 | RXFUL19 | RXFUL18 | RXFUL17 | RXFUL16 |
| bit 7 | | | | | | | bit 0 |

Legend:	C = Writable bit, but only '0' can be written to clear the bit				
R = Readable bit	W = Writable bit	U = Unimplemented bit, read	1 as '0'		
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown		

bit 15-0 **RXFUL<31:16>:** Receive Buffer n Full bits

1 = Buffer is full (set by module)

0 = Buffer is empty (cleared by user software)

R/C-0	R/C-0	R/C-0	R/C-0	R/C-0	R/C-0	R/C-0	R/C-0
RXOVF15	RXOVF14	RXOVF13	RXOVF12	RXOVF11	RXOVF10	RXOVF9	RXOVF8
bit 15							bit 8
R/C-0	R/C-0	R/C-0	R/C-0	R/C-0	R/C-0	R/C-0	R/C-0

REGISTER 21-24: CxRXOVF1: ECANx RECEIVE BUFFER OVERFLOW REGISTER 1

RXOVF7	RXOVF6	RXOVF5	RXOVF4	RXOVF3	RXOVF2	RXOVF1	RXOVF0
bit 7							bit 0
Legend:		C = Writable b	oit, but only '0'	can be writter	ו to clear the bit		

Legend:	C = Writable bit, but only '0' can be written to clear the bit				
R = Readable bit	W = Writable bit	U = Unimplemented bit, read	l as '0'		
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown		

bit 15-0 RXOVF<15:0>: Receive Buffer n Overflow bits

1 = Module attempted to write to a full buffer (set by module)

0 = No overflow condition (cleared by user software)

REGISTER 21-25: CxRXOVF2: ECANx RECEIVE BUFFER OVERFLOW REGISTER 2

| R/C-0 |
|---------|---------|---------|---------|---------|---------|---------|---------|
| RXOVF31 | RXOVF30 | RXOVF29 | RXOVF28 | RXOVF27 | RXOVF26 | RXOVF25 | RXOVF24 |
| bit 15 | | | | | | | bit 8 |

| R/C-0 |
|---------|---------|---------|---------|---------|---------|---------|---------|
| RXOVF23 | RXOVF22 | RXOVF21 | RXOVF20 | RXOVF19 | RXOVF18 | RXOVF17 | RXOVF16 |
| bit 7 | | | | | | | bit 0 |

Legend:	C = Writable bit, but only '0' can be written to clear the bit					
R = Readable bit W = Writable bit		U = Unimplemented bit, read as '0'				
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown			

bit 15-0 RXOVF<31:16>: Receive Buffer n Overflow bits

1 = Module attempted to write to a full buffer (set by module)

0 = No overflow condition (cleared by user software)

21.5 ECAN Message Buffers

ECAN Message Buffers are part of RAM memory. They are not ECAN Special Function Registers. The user application must directly write into the RAM area that is configured for ECAN Message Buffers. The location and size of the buffer area is defined by the user application.

BUFFER 21-1: ECAN™ MESSAGE BUFFER WORD 0

U-0	U-0	U-0	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x
_	_	_	SID10	SID9	SID8	SID7	SID6
bit 15							bit 8
R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x
SID5	SID4	SID3	SID2	SID1	SID0	SRR	IDE
bit 7							bit 0
Legend:							
R = Readable I	bit	W = Writable	bit	U = Unimpler	mented bit, read	d as '0'	
-n = Value at P	OR	'1' = Bit is set		'0' = Bit is cle	ared	x = Bit is unkr	nown
bit 15-13	Unimplemen	ted: Read as '	0'				
bit 12-2	SID<10:0>: S	tandard Identif	ier bits				
bit 1	SRR: Substitu	ute Remote Re	quest bit				
	When IDE = 0	<u>):</u>					
	1 = Message	will request rea	mote transmis	ssion			
	0 = Normal m	lessage					
	When IDE = 1	L <u>:</u>					
	The SRR bit r	nust be set to '	1'.				
bit 0	IDE: Extende	d Identifier bit					
	1 = Message	will transmit Ex	ktended Ident	ifier			
	0 = Message	will transmit St	andard Identi	fier			

BUFFER 21-2: ECAN™ MESSAGE BUFFER WORD 1

U-0	U-0	U-0	U-0	R/W-x	R/W-x	R/W-x	R/W-x	
—	—	—		EID17	EID16	EID15	EID14	
bit 15							bit 8	
R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	
EID13	EID12	EID11	EID10	EID9	EID8	EID7	EID6	
bit 7							bit 0	
Legend:								
R = Readable bit W = Writable bit			bit	U = Unimplemented bit, read as '0'				
-n = Value at F	POR	'1' = Bit is set		'0' = Bit is cle	ared	x = Bit is unknown		

bit 15-12 Unimplemented: Read as '0'

bit 11-0 EID<17:6>: Extended Identifier bits



dsPIC33EPXXXGP50X, dsPIC33EPXXXMC20X/50X AND PIC24EPXXXGP/MC20X

26.0 PROGRAMMABLE CYCLIC REDUNDANCY CHECK (CRC) GENERATOR

- Note 1: This data sheet summarizes the features of the dsPIC33EPXXXGP50X, dsPIC33EPXXXMC20X/50X and PIC24EPXXXGP/MC20X families of devices. It is not intended to be a comprehensive reference source. To complement the information in this data sheet, refer to "Programmable Cyclic Redundancy Check (CRC)" (DS70346) of the "dsPIC33/PIC24 Family Reference Manual", which is available from the Microchip web site (www.microchip.com).
 - Some registers and associated bits described in this section may not be available on all devices. Refer to Section 4.0 "Memory Organization" in this data sheet for device-specific register and bit information.

The programmable CRC generator offers the following features:

- User-programmable (up to 32nd order) polynomial CRC equation
- Interrupt output
- Data FIFO

The programmable CRC generator provides a hardware implemented method of quickly generating checksums for various networking and security applications. It offers the following features:

- User-programmable CRC polynomial equation, up to 32 bits
- Programmable shift direction (little or big-endian)
- · Independent data and polynomial lengths
- Configurable interrupt output
- Data FIFO

A simplified block diagram of the CRC generator is shown in Figure 26-1. A simple version of the CRC shift engine is shown in Figure 26-2.



FIGURE 26-1: CRC BLOCK DIAGRAM





26.1 Overview

The CRC module can be programmed for CRC polynomials of up to the 32nd order, using up to 32 bits. Polynomial length, which reflects the highest exponent in the equation, is selected by the PLEN<4:0> bits (CRCCON2<4:0>).

The CRCXORL and CRCXORH registers control which exponent terms are included in the equation. Setting a particular bit includes that exponent term in the equation; functionally, this includes an XOR operation on the corresponding bit in the CRC engine. Clearing the bit disables the XOR.

For example, consider two CRC polynomials, one a 16-bit equation and the other a 32-bit equation:

$$\begin{array}{c} x16+x12+x5+1\\ \text{and}\\ x32+x26+x23+x22+x16+x12+x11+x10+x8+x7\\ +x5+x4+x2+x+1 \end{array}$$

To program these polynomials into the CRC generator, set the register bits as shown in Table 26-1.

Note that the appropriate positions are set to '1' to indicate that they are used in the equation (for example, X26 and X23). The 0 bit required by the equation is always XORed; thus, X0 is a don't care. For a polynomial of length N, it is assumed that the *N*th bit will always be used, regardless of the bit setting. Therefore, for a polynomial length of 32, there is no 32nd bit in the CRCxOR register.

TABLE 26-1:CRC SETUP EXAMPLES FOR16 AND 32-BIT POLYNOMIAL

CBC Control	Bit Values						
Bits	16-bit Polynomial	32-bit Polynomial					
PLEN<4:0>	01111	11111					
X<31:16>	0000 0000 0000 000x	0000 0100 1100 0001					
X<15:0>	0001 0000 0010 000x	0001 1101 1011 011x					

26.2 Programmable CRC Resources

Many useful resources are provided on the main product page of the Microchip web site for the devices listed in this data sheet. This product page, which can be accessed using this link, contains the latest updates and additional information.

Note:	In the event you are not able to access the
	product page using the link above, enter
	this URL in your browser:
	http://www.microchip.com/wwwproducts/
	Devices.aspx?dDocName=en555464

26.2.1 KEY RESOURCES

- "Programmable Cyclic Redundancy Check (CRC)" (DS70346) in the "dsPIC33/PIC24 Family Reference Manual"
- Code Samples
- Application Notes
- Software Libraries
- · Webinars
- All Related "dsPIC33/PIC24 Family Reference Manual" Sections
- Development Tools

27.0 SPECIAL FEATURES

Note: This data sheet summarizes the features of the dsPIC33EPXXXGP50X. dsPIC33EPXXXMC20X/50X and PIC24EPXXXGP/MC20X families of devices. It is not intended to be a То comprehensive reference source. complement the information in this data sheet, refer to the related section of the "dsPIC33/PIC24 Familv Reference Manual', which is available from the Microchip web site (www.microchip.com).

dsPIC33EPXXXGP50X, dsPIC33EPXXXMC20X/50X and PIC24EPXXXGP/MC20X devices include several features intended to maximize application flexibility and reliability, and minimize cost through elimination of external components. These are:

- Flexible Configuration
- Watchdog Timer (WDT)
- Code Protection and CodeGuard[™] Security
- JTAG Boundary Scan Interface
- In-Circuit Serial Programming[™] (ICSP[™])
- In-Circuit Emulation

27.1 Configuration Bits

In dsPIC33EPXXXGP50X, dsPIC33EPXXXMC20X/ 50X and PIC24EPXXXGP/MC20X devices, the Configuration bytes are implemented as volatile memory. This means that configuration data must be programmed each time the device is powered up. Configuration data is stored in at the top of the on-chip program memory space, known as the Flash Configuration bytes. Their specific locations are shown in Table 27-1. The configuration data is automatically loaded from the Flash Configuration bytes to the proper Configuration Shadow registers during device Resets.

Note:	Configuration data is reloaded on all types
	of device Resets.

When creating applications for these devices, users should always specifically allocate the location of the Flash Configuration bytes for configuration data in their code for the compiler. This is to make certain that program code is not stored in this address when the code is compiled.

The upper 2 bytes of all Flash Configuration Words in program memory should always be '1111 1111 1111 1111 1111 1111'. This makes them appear to be NOP instructions in the remote event that their locations are ever executed by accident. Since Configuration bits are not implemented in the corresponding locations, writing '1's to these locations has no effect on device operation.

Note: Performing a page erase operation on the last page of program memory clears the Flash Configuration bytes, enabling code protection as a result. Therefore, users should avoid performing page erase operations on the last page of program memory.

The Configuration Flash bytes map is shown in Table 27-1.





FIGURE 30-10: HIGH-SPEED PWMx MODULE TIMING CHARACTERISTICS (dsPIC33EPXXXMC20X/50X and PIC24EPXXXMC20X DEVICES ONLY)



TABLE 30-29: HIGH-SPEED PWMx MODULE TIMING REQUIREMENTS (dsPIC33EPXXXMC20X/50X and PIC24EPXXXMC20X DEVICES ONLY)

AC CHARACTERISTICS			Standa (unless Operati	rd Opera otherwis ng tempe	ting Con se stated rature	ditions: 3) -40°C ≤ T -40°C ≤ T	3.0V to 3.6V $A \le +85^{\circ}C$ for Industrial $A \le +125^{\circ}C$ for Extended
Param No.	Symbol	Characteristic ⁽¹⁾	Min.	Тур.	Max.	Units	Conditions
MP10	TFPWM	PWMx Output Fall Time	—			ns	See Parameter DO32
MP11	TRPWM	PWMx Output Rise Time	_	_		ns	See Parameter DO31
MP20	TFD	Fault Input ↓ to PWMx I/O Change	_	_	15	ns	
MP30	Tfh	Fault Input Pulse Width	15	_		ns	

Note 1: These parameters are characterized but not tested in manufacturing.

АС СНА							
Param No.	Symbol	Characteristic	Min.	Тур.	Max.	Units	Conditions
		ADC /	Accuracy	/ (12-Bit	Mode)		
AD20a	Nr	Resolution	12	2 Data Bi	its	bits	
AD21a	INL	Integral Nonlinearity	-2.5		2.5	LSb	-40°C ≤ TA ≤ +85°C (Note 2)
			-5.5		5.5	LSb	+85°C < TA \leq +125°C (Note 2)
AD22a	DNL	Differential Nonlinearity	-1		1	LSb	-40°C \leq TA \leq +85°C (Note 2)
			-1		1	LSb	+85°C < TA \leq +125°C (Note 2)
AD23a	Gerr	Gain Error ⁽³⁾	-10		10	LSb	-40°C \leq TA \leq +85°C (Note 2)
			-10		10	LSb	+85°C < TA \leq +125°C (Note 2)
AD24a	EOFF	Offset Error	-5		5	LSb	$-40^{\circ}C \le TA \le +85^{\circ}C$ (Note 2)
			-5		5	LSb	+85°C < TA \leq +125°C (Note 2)
AD25a	—	Monotonicity	_			—	Guaranteed
		Dynamic	Performa	ance (12	-Bit Mod	e)	
AD30a	THD	Total Harmonic Distortion ⁽³⁾	_	75		dB	
AD31a	SINAD	Signal to Noise and Distortion ⁽³⁾	_	68	-	dB	
AD32a	SFDR	Spurious Free Dynamic Range ⁽³⁾		80	_	dB	
AD33a	Fnyq	Input Signal Bandwidth ⁽³⁾	_	250	—	kHz	
AD34a	ENOB	Effective Number of Bits ⁽³⁾	11.09	11.3	_	bits	

TABLE 30-58: ADC MODULE SPECIFICATIONS (12-BIT MODE)

Note 1: Device is functional at VBORMIN < VDD < VDDMIN, but will have degraded performance. Device functionality is tested, but not characterized. Analog modules (ADC, op amp/comparator and comparator voltage reference) may have degraded performance. Refer to Parameter BO10 in Table 30-13 for the minimum and maximum BOR values.

2: For all accuracy specifications, VINL = AVSS = VREFL = 0V and AVDD = VREFH = 3.6V.

3: Parameters are characterized but not tested in manufacturing.

DC CHARACTERISTICS			Standard Operating Conditions: 3.0V to 3.6V(unless otherwise stated)Operating temperature $-40^{\circ}C \le TA \le +150^{\circ}C$					
Param.	Symbol	Characteristic	Min.	Тур.	Max.	Units	Conditions	
HDO10	Vol	Output Low Voltage 4x Sink Driver Pins ⁽²⁾	_	—	0.4	V	IOL ≤ 5 mA, VDD = 3.3V (Note 1)	
		Output Low Voltage 8x Sink Driver Pins ⁽³⁾	—	_	0.4	V	IOL ≤ 8 mA, VDD = 3.3V (Note 1)	
HDO20	Vон	Output High Voltage 4x Source Driver Pins ⁽²⁾	2.4	—		V	IOH ≥ -10 mA, VDD = 3.3V (Note 1)	
		Output High Voltage 8x Source Driver Pins ⁽³⁾	2.4	—		V	IOH ≥ 15 mA, VDD = 3.3V (Note 1)	
HDO20A	Vон1	1 Output High Voltage 4x Source Driver Pins ⁽²⁾	1.5	—	_	V	IOH ≥ -3.9 mA, VDD = 3.3V (Note 1)	
			2.0	—			IOH ≥ -3.7 mA, VDD = 3.3V (Note 1)	
			3.0	—			IOH ≥ -2 mA, VDD = 3.3V (Note 1)	
		Output High Voltage 8x Source Driver Pins ⁽³⁾	1.5	_		V	IOH ≥ -7.5 mA, VDD = 3.3V (Note 1)	
			2.0	_			IOH ≥ -6.8 mA, VDD = 3.3V (Note 1)	
			3.0	_	_		IOH ≥ -3 mA, VDD = 3.3V (Note 1)	

TABLE 31-8: DC CHARACTERISTICS: I/O PIN OUTPUT SPECIFICATIONS

Note 1: Parameters are characterized, but not tested.

2: Includes all I/O pins that are not 8x Sink Driver pins (see below).

Includes the following pins:
 For devices with less than 64 pins: RA3, RA4, RA9, RB<15:7> and RC3
 For 64-pin devices: RA4, RA9, RB<15:7>, RC3 and RC15

28-Lead Plastic Quad Flat, No Lead Package (MM) - 6x6x0.9mm Body [QFN-S] With 0.40 mm Terminal Length

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



	MILLIMETERS				
Dimension	MIN	NOM	MAX		
Number of Pins	N		28		
Pitch	е		0.65 BSC		
Overall Height	Α	0.80 0.90 1.00			
Standoff	A1	0.00	0.02	0.05	
Terminal Thickness	A3	0.20 REF			
Overall Width	E	6.00 BSC			
Exposed Pad Width	E2	3.65 3.70 4.			
Overall Length	D		6.00 BSC		
Exposed Pad Length	D2	3.65	3.70	4.70	
Terminal Width	b	0.23	0.30	0.35	
Terminal Length	L	0.30	0.40	0.50	
Terminal-to-Exposed Pad	K	0.20	-	-	

Notes:

1. Pin 1 visual index feature may vary, but must be located within the hatched area.

2. Package is saw singulated

3. Dimensioning and tolerancing per ASME Y14.5M

BSC: Basic Dimension. Theoretically exact value shown without tolerances.

 $\label{eq:REF:Reference Dimension, usually without tolerance, for information purposes only.$

Microchip Technology Drawing C04-124C Sheet 2 of 2