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### Applications of "[Embedded - Microcontrollers](#)"

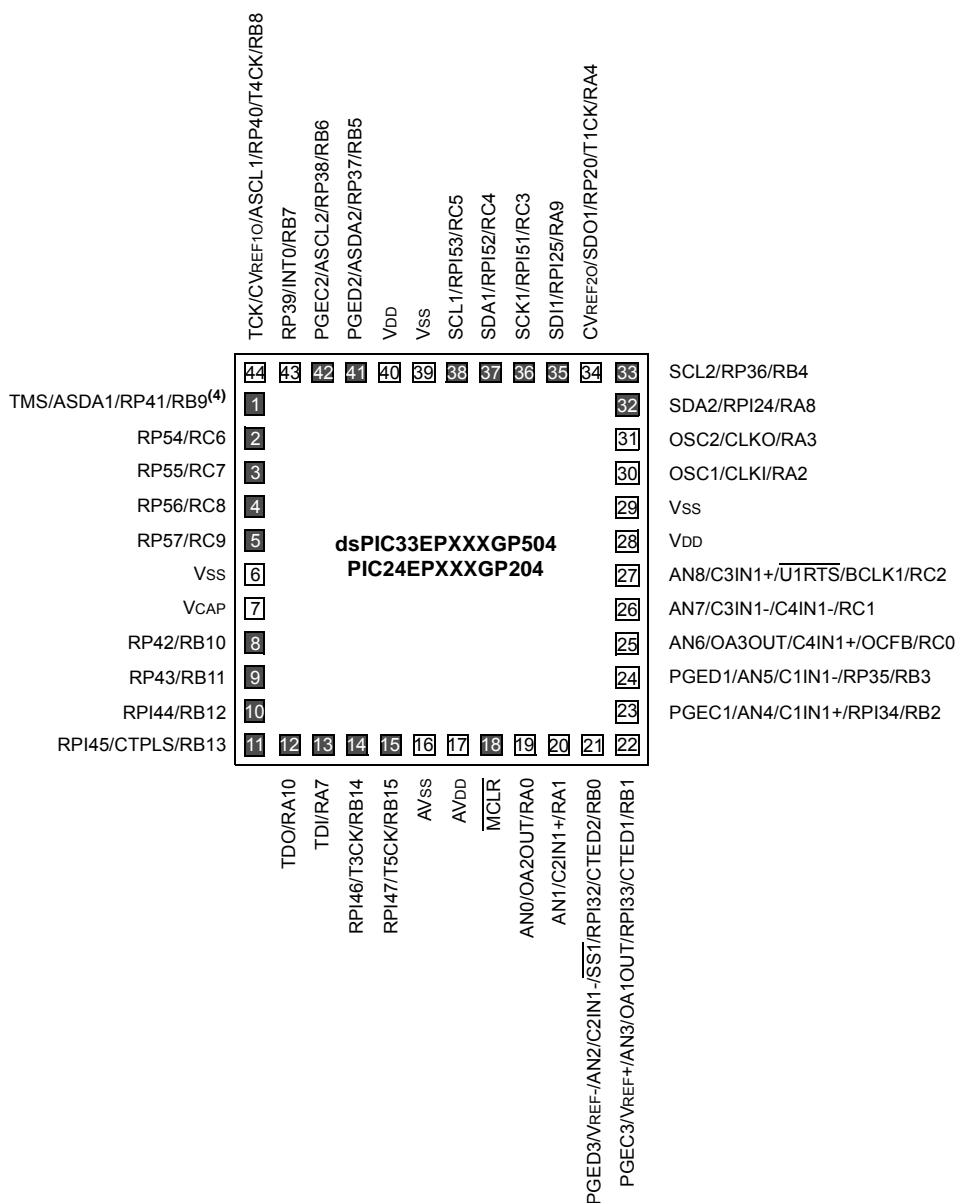
#### Details

Product Status	Active
Core Processor	PIC
Core Size	16-Bit
Speed	70 MIPS
Connectivity	I <sup>2</sup> C, IrDA, LINbus, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, DMA, POR, PWM, WDT
Number of I/O	35
Program Memory Size	512KB (170K x 24)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	24K x 16
Voltage - Supply (Vcc/Vdd)	3V ~ 3.6V
Data Converters	A/D 9x10b/12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	48-UQFN Exposed Pad
Supplier Device Package	48-UQFN (6x6)
Purchase URL	<a href="https://www.e-xfl.com/product-detail/microchip-technology/pic24ep512gp204-i-mv">https://www.e-xfl.com/product-detail/microchip-technology/pic24ep512gp204-i-mv</a>

## Pin Diagrams (Continued)

44-Pin VTLA<sup>(1,2,3)</sup>

■ = Pins are up to 5V tolerant



- Note 1:** The RPN/RPIN pins can be used by any remappable peripheral with some limitation. See **Section 11.4 “Peripheral Pin Select (PPS)”** for available peripherals and for information on limitations.
- Note 2:** Every I/O port pin (RAX-RGX) can be used as a Change Notification pin (CNAX-CNGX). See **Section 11.0 “I/O Ports”** for more information.
- Note 3:** The metal pad at the bottom of the device is not connected to any pins and is recommended to be connected to VSS externally.
- Note 4:** There is an internal pull-up resistor connected to the TMS pin when the JTAG interface is active. See the JTAGEN bit field in Table 27-2.

## 4.2.5 X AND Y DATA SPACES

The dsPIC33EPXXXMC20X/50X and dsPIC33EPXXXGP50X core has two Data Spaces, X and Y. These Data Spaces can be considered either separate (for some DSP instructions) or as one unified linear address range (for MCU instructions). The Data Spaces are accessed using two Address Generation Units (AGUs) and separate data paths. This feature allows certain instructions to concurrently fetch two words from RAM, thereby enabling efficient execution of DSP algorithms, such as Finite Impulse Response (FIR) filtering and Fast Fourier Transform (FFT).

The X Data Space is used by all instructions and supports all addressing modes. X Data Space has separate read and write data buses. The X read data bus is the read data path for all instructions that view Data Space as combined X and Y address space. It is also the X data prefetch path for the dual operand DSP instructions (MAC class).

The Y Data Space is used in concert with the X Data Space by the MAC class of instructions (CLR, ED, EDAC, MAC, MOVSAC, MPY, MPY.N and MSC) to provide two concurrent data read paths.

Both the X and Y Data Spaces support Modulo Addressing mode for all instructions, subject to addressing mode restrictions. Bit-Reversed Addressing mode is only supported for writes to X Data Space. Modulo Addressing and Bit-Reversed Addressing are not present in PIC24EPXXXGP/MC20X devices.

All data memory writes, including in DSP instructions, view Data Space as combined X and Y address space. The boundary between the X and Y Data Spaces is device-dependent and is not user-programmable.

## 4.3 Memory Resources

Many useful resources are provided on the main product page of the Microchip web site for the devices listed in this data sheet. This product page, which can be accessed using this link, contains the latest updates and additional information.

<b>Note:</b>	In the event you are not able to access the product page using the link above, enter this URL in your browser: <a href="http://www.microchip.com/wwwproducts/Devices.aspx?dDocName=en555464">http://www.microchip.com/wwwproducts/Devices.aspx?dDocName=en555464</a>
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### 4.3.1 KEY RESOURCES

- “**Program Memory**” (DS70613) in the “*dsPIC33/PIC24 Family Reference Manual*”
- Code Samples
- Application Notes
- Software Libraries
- Webinars
- All Related “*dsPIC33/PIC24 Family Reference Manual*” Sections
- Development Tools

**TABLE 4-3: INTERRUPT CONTROLLER REGISTER MAP FOR PIC24EPXXXGP20X DEVICES ONLY**

File Name	Addr.	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	All Resets
IFS0	0800	—	DMA1IF	AD1IF	U1TXIF	U1RXIF	SPI1IF	SPI1EIF	T3IF	T2IF	OC2IF	IC2IF	DMA0IF	T1IF	OC1IF	IC1IF	INT0IF	0000
IFS1	0802	U2TXIF	U2RXIF	INT2IF	T5IF	T4IF	OC4IF	OC3IF	DMA2IF	—	—	—	INT1IF	CNIF	CMIF	MI2C1IF	SI2C1IF	0000
IFS2	0804	—	—	—	—	—	—	—	—	—	IC4IF	IC3IF	DMA3IF	—	—	SPI2IF	SPI2EIF	0000
IFS3	0806	—	—	—	—	—	—	—	—	—	—	—	—	—	MI2C2IF	SI2C2IF	—	0000
IFS4	0808	—	—	CTMUIF	—	—	—	—	—	—	—	—	—	CRCIF	U2EIF	U1EIF	—	0000
IFS8	0810	JTAGIF	ICDIF	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
IFS9	0812	—	—	—	—	—	—	—	—	—	PTG3IF	PTG2IF	PTG1IF	PTG0IF	PTGWDTIF	PTGSTIEIF	—	0000
IEC0	0820	—	DMA1IE	AD1IE	U1TXIE	U1RXIE	SPI1IE	SPI1EIE	T3IE	T2IE	OC2IE	IC2IE	DMA0IE	T1IE	OC1IE	IC1IE	INT0IE	0000
IEC1	0822	U2TXIE	U2RXIE	INT2IE	T5IE	T4IE	OC4IE	OC3IE	DMA2IE	—	—	—	INT1IE	CNIE	CMIE	MI2C1IE	SI2C1IE	0000
IEC2	0824	—	—	—	—	—	—	—	—	—	IC4IE	IC3IE	DMA3IE	—	—	SPI2IE	SPI2EIE	0000
IEC3	0826	—	—	—	—	—	—	—	—	—	—	—	—	—	MI2C2IE	SI2C2IE	—	0000
IEC4	0828	—	—	CTMUIE	—	—	—	—	—	—	—	—	—	CRCIE	U2EIE	U1EIE	—	0000
IEC8	0830	JTAGIE	ICDIE	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
IEC9	0832	—	—	—	—	—	—	—	—	—	PTG3IE	PTG2IE	PTG1IE	PTG0IE	PTGWDTIE	PTGSTIEIE	—	0000
IPC0	0840	—	T1IP<2:0>			—	OC1IP<2:0>			—	IC1IP<2:0>			—	INT0IP<2:0>			4444
IPC1	0842	—	T2IP<2:0>			—	OC2IP<2:0>			—	IC2IP<2:0>			—	DMA0IP<2:0>			4444
IPC2	0844	—	U1RXIP<2:0>			—	SPI1IP<2:0>			—	SPI1EIP<2:0>			—	T3IP<2:0>			4444
IPC3	0846	—	—	—	—	—	DMA1IP<2:0>			—	AD1IP<2:0>			—	U1TXIP<2:0>			0444
IPC4	0848	—	CNIP<2:0>			—	CMIP<2:0>			—	MI2C1IP<2:0>			—	SI2C1IP<2:0>			4444
IPC5	084A	—	—	—	—	—	—	—	—	—	—	—	—	—	INT1IP<2:0>			0004
IPC6	084C	—	T4IP<2:0>			—	OC4IP<2:0>			—	OC3IP<2:0>			—	DMA2IP<2:0>			4444
IPC7	084E	—	U2TXIP<2:0>			—	U2RXIP<2:0>			—	INT2IP<2:0>			—	T5IP<2:0>			4444
IPC8	0850	—	—	—	—	—	—	—	—	—	SPI2IP<2:0>			—	SPI2EIP<2:0>			0044
IPC9	0852	—	—	—	—	—	IC4IP<2:0>			—	IC3IP<2:0>			—	DMA3IP<2:0>			0444
IPC12	0858	—	—	—	—	—	MI2C2IP<2:0>			—	SI2C2IP<2:0>			—	—	—	—	0440
IPC16	0860	—	CRCIP<2:0>			—	U2EIP<2:0>			—	U1EIP<2:0>			—	—	—	—	4440
IPC19	0866	—	—	—	—	—	—	—	—	—	CTMUIP<2:0>			—	—	—	—	0040
IPC35	0886	—	JTAGIP<2:0>			—	ICDIP<2:0>			—	—	—	—	—	—	—	—	4400
IPC36	0888	—	PTG0IP<2:0>			—	PTGWDTIP<2:0>			—	PTGSTIEIP<2:0>			—	—	—	—	4440
IPC37	088A	—	—	—	—	—	PTG3IP<2:0>			—	PTG2IP<2:0>			—	PTG1IP<2:0>			0444
INTCON1	08C0	NSTDIS	OVAERR	OVERR	—	—	—	—	—	—	DIV0ERR	DMACERR	MATHERR	ADDRERR	STKERR	OSCFail	—	0000
INTCON2	08C2	GIE	DISI	SWTRAP	—	—	—	—	—	—	—	—	—	—	INT2EP	INT1EP	INT0EP	8000
INTCON3	08C4	—	—	—	—	—	—	—	—	—	—	DAE	DOOVR	—	—	—	—	0000
INTCON4	08C6	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	SGHT	0000
INTTREG	08C8	—	—	—	—	ILR<3:0>				VECNUM<7:0>								0000

**Legend:** — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

**TABLE 4-21: ECAN1 REGISTER MAP WHEN WIN (C1CTRL1<0>) = 0 OR 1 FOR dsPIC33EPXXXMC/GP50X DEVICES ONLY**

File Name	Addr.	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	All Resets
C1CTRL1	0400	—	—	CSIDL	ABAT	CANCKS	REQOP<2:0>			OPMODE<2:0>			—	CANCAP	—	—	WIN	0480
C1CTRL2	0402	—	—	—	—	—	—	—	—	—	—	—	DNCNT<4:0>					0000
C1VEC	0404	—	—	—	FILHIT<4:0>					—	ICODE<6:0>							0040
C1FCTRL	0406	DMABS<2:0>			—	—	—	—	—	—	—	—	FSA<4:0>					0000
C1FIFO	0408	—	—	FBP<5:0>						—	—	FNRB<5:0>						0000
C1INTF	040A	—	—	TXBO	TXBP	RXBP	TXWAR	RXWAR	EWARN	IVRIF	WAKIF	ERRIF	—	FIFOIF	RBOVIF	RBIF	TBIF	0000
C1INTE	040C	—	—	—	—	—	—	—	—	IVRIE	WAKIE	ERRIE	—	FIFOIE	RBOVIE	RBIE	TBIE	0000
C1EC	040E	TERRCNT<7:0>								RERRCNT<7:0>								0000
C1CFG1	0410	—	—	—	—	—	—	—	—	SJW<1:0>		BRP<5:0>						0000
C1CFG2	0412	—	WAKFIL	—	—	—	SEG2PH<2:0>			SEG2PHTS	SAM	SEG1PH<2:0>			PRSEG<2:0>			0000
C1FEN1	0414	FLTEN15	FLTEN14	FLTEN13	FLTEN12	FLTEN11	FLTEN10	FLTEN9	FLTEN8	FLTEN7	FLTEN6	FLTEN5	FLTEN4	FLTEN3	FLTEN2	FLTEN1	FLTEN0	FFFF
C1FMSKSEL1	0418	F7MSK<1:0>		F6MSK<1:0>		F5MSK<1:0>		F4MSK<1:0>		F3MSK<1:0>		F2MSK<1:0>		F1MSK<1:0>		F0MSK<1:0>		0000
C1FMSKSEL2	041A	F15MSK<1:0>		F14MSK<1:0>		F13MSK<1:0>		F12MSK<1:0>		F11MSK<1:0>		F10MSK<1:0>		F9MSK<1:0>		F8MSK<1:0>		0000

**Legend:** — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

**TABLE 4-22: ECAN1 REGISTER MAP WHEN WIN (C1CTRL1<0>) = 0 FOR dsPIC33EPXXXMC/GP50X DEVICES ONLY**

File Name	Addr	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	All Resets
	0400-041E	See definition when WIN = x																
C1RXFUL1	0420	RXFUL15	RXFUL14	RXFUL13	RXFUL12	RXFUL11	RXFUL10	RXFUL9	RXFUL8	RXFUL7	RXFUL6	RXFUL5	RXFUL4	RXFUL3	RXFUL2	RXFUL1	RXFUL0	0000
C1RXFUL2	0422	RXFUL31	RXFUL30	RXFUL29	RXFUL28	RXFUL27	RXFUL26	RXFUL25	RXFUL24	RXFUL23	RXFUL22	RXFUL21	RXFUL20	RXFUL19	RXFUL18	RXFUL17	RXFUL16	0000
C1RXOVF1	0428	RXOVF15	RXOVF14	RXOVF13	RXOVF12	RXOVF11	RXOVF10	RXOVF9	RXOVF8	RXOVF7	RXOVF6	RXOVF5	RXOVF4	RXOVF3	RXOVF2	RXOVF1	RXOVF0	0000
C1RXOVF2	042A	RXOVF31	RXOVF30	RXOVF29	RXOVF28	RXOVF27	RXOVF26	RXOVF25	RXOVF24	RXOVF23	RXOVF22	RXOVF21	RXOVF20	RXOVF19	RXOVF18	RXOVF17	RXOVF16	0000
C1TR01CON	0430	TXEN1	TXABT1	TXLARB1	TXERR1	TXREQ1	RTREN1	TX1PRI<1:0>		TXEN0	TXABAT0	TXLARB0	TXERR0	TXREQ0	RTREN0	TX0PRI<1:0>		0000
C1TR23CON	0432	TXEN3	TXABT3	TXLARB3	TXERR3	TXREQ3	RTREN3	TX3PRI<1:0>		TXEN2	TXABAT2	TXLARB2	TXERR2	TXREQ2	RTREN2	TX2PRI<1:0>		0000
C1TR45CON	0434	TXEN5	TXABT5	TXLARB5	TXERR5	TXREQ5	RTREN5	TX5PRI<1:0>		TXEN4	TXABAT4	TXLARB4	TXERR4	TXREQ4	RTREN4	TX4PRI<1:0>		0000
C1TR67CON	0436	TXEN7	TXABT7	TXLARB7	TXERR7	TXREQ7	RTREN7	TX7PRI<1:0>		TXEN6	TXABAT6	TXLARB6	TXERR6	TXREQ6	RTREN6	TX6PRI<1:0>		xxxx
C1RXD	0440	ECAN1 Receive Data Word																xxxx
C1TXD	0442	ECAN1 Transmit Data Word																xxxx

**Legend:** x = unknown value on Reset, — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

**REGISTER 7-3: INTCON1: INTERRUPT CONTROL REGISTER 1 (CONTINUED)**

bit 4	<b>MATHERR:</b> Math Error Status bit 1 = Math error trap has occurred 0 = Math error trap has not occurred
bit 3	<b>ADDRERR:</b> Address Error Trap Status bit 1 = Address error trap has occurred 0 = Address error trap has not occurred
bit 2	<b>STKERR:</b> Stack Error Trap Status bit 1 = Stack error trap has occurred 0 = Stack error trap has not occurred
bit 1	<b>OSCFAIL:</b> Oscillator Failure Trap Status bit 1 = Oscillator failure trap has occurred 0 = Oscillator failure trap has not occurred
bit 0	<b>Unimplemented:</b> Read as '0'

**Note 1:** These bits are available on dsPIC33EPXXXMC20X/50X and dsPIC33EPXXXGP50X devices only.

**REGISTER 10-6: PMD7: PERIPHERAL MODULE DISABLE CONTROL REGISTER 7**

U-0		U-0		U-0		U-0		U-0		U-0	
—		—		—		—		—		—	
bit 15										bit 8	

U-0		U-0		U-0		R/W-0		R/W-0		U-0		U-0		U-0			
—		—		—		DMA0MD <sup>(1)</sup>		PTGMD		—		—		—			
						DMA1MD <sup>(1)</sup>											
						DMA2MD <sup>(1)</sup>											
						DMA3MD <sup>(1)</sup>											
bit 7																bit 0	

**Legend:**

R = Readable bit

W = Writable bit

U = Unimplemented bit, read as '0'

-n = Value at POR

'1' = Bit is set

'0' = Bit is cleared

x = Bit is unknown

bit 15-5 **Unimplemented:** Read as '0'bit 4 **DMA0MD:** DMA0 Module Disable bit<sup>(1)</sup>

1 = DMA0 module is disabled

0 = DMA0 module is enabled

**DMA1MD:** DMA1 Module Disable bit<sup>(1)</sup>

1 = DMA1 module is disabled

0 = DMA1 module is enabled

**DMA2MD:** DMA2 Module Disable bit<sup>(1)</sup>

1 = DMA2 module is disabled

0 = DMA2 module is enabled

**DMA3MD:** DMA3 Module Disable bit<sup>(1)</sup>

1 = DMA3 module is disabled

0 = DMA3 module is enabled

bit 3 **PTGMD:** PTG Module Disable bit

1 = PTG module is disabled

0 = PTG module is enabled

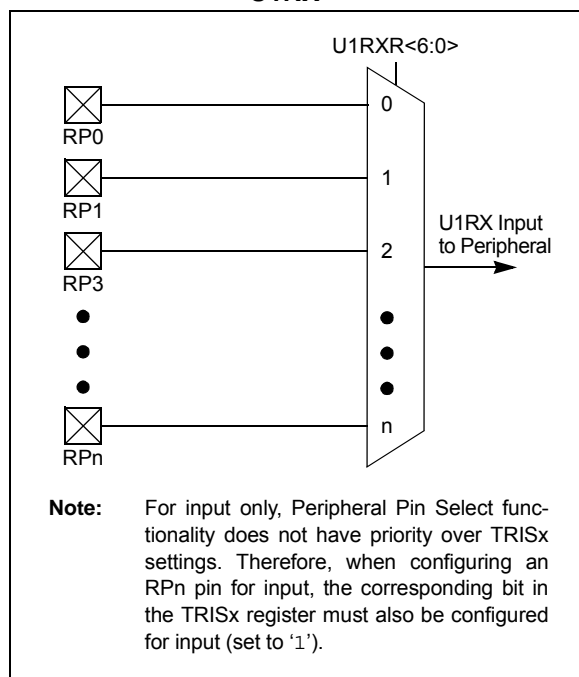
bit 2-0 **Unimplemented:** Read as '0'**Note 1:** This single bit enables and disables all four DMA channels.

#### 11.4.4 INPUT MAPPING

The inputs of the Peripheral Pin Select options are mapped on the basis of the peripheral. That is, a control register associated with a peripheral dictates the pin it will be mapped to. The RPNR<sub>x</sub> registers are used to configure peripheral input mapping (see Register 11-1 through Register 11-17). Each register contains sets of 7-bit fields, with each set associated with one of the remappable peripherals. Programming a given peripheral's bit field with an appropriate 7-bit value maps the RPN pin with the corresponding value to that peripheral. For any given device, the valid range of values for any bit field corresponds to the maximum number of Peripheral Pin Selections supported by the device.

For example, Figure 11-2 illustrates remappable pin selection for the U1RX input.

**FIGURE 11-2: REMAPPABLE INPUT FOR U1RX**



##### 11.4.4.1 Virtual Connections

dsPIC33EPXXXGP50X, dsPIC33EPXXXMC20X/50X and PIC24EPXXXGP/MC20X devices support virtual (internal) connections to the output of the op amp/comparator module (see Figure 25-1 in **Section 25.0 “Op Amp/Comparator Module”**), and the PTG module (see **Section 24.0 “Peripheral Trigger Generator (PTG) Module”**).

In addition, dsPIC33EPXXXMC20X/50X and PIC24EPXXXMC20X devices support virtual connections to the filtered QE1 module inputs: FINDX1, FHOME1, FINDX2 and FHOME2 (see Figure 17-1 in **Section 17.0 “Quadrature Encoder Interface (QE1) Module (dsPIC33EPXXXMC20X/50X and PIC24EPXXXMC20X Devices Only)”**).

Virtual connections provide a simple way of inter-peripheral connection without utilizing a physical pin. For example, by setting the FLT1R<6:0> bits of the RPNR12 register to the value of 'b0000001, the output of the analog comparator, C1OUT, will be connected to the PWM Fault 1 input, which allows the analog comparator to trigger PWM Faults without the use of an actual physical pin on the device.

Virtual connection to the QE1 module allows peripherals to be connected to the QE1 digital filter input. To utilize this filter, the QE1 module must be enabled and its inputs must be connected to a physical RPN pin. Example 11-2 illustrates how the input capture module can be connected to the QE1 digital filter.

**EXAMPLE 11-2: CONNECTING IC1 TO THE HOME1 QE1 DIGITAL FILTER INPUT ON PIN 43 OF THE dsPIC33EPXXXMC206 DEVICE**

```

RPNR15 = 0x2500;    /* Connect the QE1 HOME1 input to RP37 (pin 43) */
RPNR7  = 0x009;    /* Connect the IC1 input to the digital filter on the FHOME1 input */

QE1IOC = 0x4000;    /* Enable the QE1 digital filter */
QE1CON = 0x8000;    /* Enable the QE1 module */
    
```



**REGISTER 11-6: RPINR11: PERIPHERAL PIN SELECT INPUT REGISTER 11**

U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
—	—	—	—	—	—	—	—
bit 15							bit 8

U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	
—	OCFAR<6:0>							
bit 7								bit 0

**Legend:**

R = Readable bit

W = Writable bit

U = Unimplemented bit, read as '0'

-n = Value at POR

'1' = Bit is set

'0' = Bit is cleared

x = Bit is unknown

bit 15-7 **Unimplemented:** Read as '0'

bit 6-0 **OCFAR<6:0>:** Assign Output Compare Fault A (OCFA) to the Corresponding RPn Pin bits (see Table 11-2 for input pin selection numbers)

1111001 = Input tied to RPI121

.

.

.

0000001 = Input tied to CMP1

0000000 = Input tied to Vss

## 16.0 HIGH-SPEED PWM MODULE (dsPIC33EPXXXMC20X/50X AND PIC24EPXXXMC20X DEVICES ONLY)

**Note 1:** This data sheet summarizes the features of the dsPIC33EPXXXGP50X, dsPIC33EPXXXMC20X/50X and PIC24EPXXXGP/MC20X families of devices. It is not intended to be a comprehensive reference source. To complement the information in this data sheet, refer to “**High-Speed PWM**” (DS70645) in the “*dsPIC33/PIC24 Family Reference Manual*”, which is available from the Microchip web site ([www.microchip.com](http://www.microchip.com)).

**2:** Some registers and associated bits described in this section may not be available on all devices. Refer to **Section 4.0 “Memory Organization”** in this data sheet for device-specific register and bit information.

The dsPIC33EPXXXMC20X/50X and PIC24EPXXXMC20X devices support a dedicated Pulse-Width Modulation (PWM) module with up to 6 outputs.

The high-speed PWMx module consists of the following major features:

- Three PWM generators
- Two PWM outputs per PWM generator
- Individual period and duty cycle for each PWM pair
- Duty cycle, dead time, phase shift and frequency resolution of  $T_{CY}/2$  (7.14 ns at  $F_{CY} = 70\text{MHz}$ )
- Independent Fault and current-limit inputs for six PWM outputs
- Redundant output
- Center-Aligned PWM mode
- Output override control
- Chop mode (also known as Gated mode)
- Special Event Trigger
- Prescaler for input clock
- PWMxL and PWMxH output pin swapping
- Independent PWM frequency, duty cycle and phase-shift changes for each PWM generator
- Dead-time compensation
- Enhanced Leading-Edge Blanking (LEB) functionality
- Frequency resolution enhancement
- PWM capture functionality

**Note:** In Edge-Aligned PWM mode, the duty cycle, dead time, phase shift and frequency resolution are 8.32 ns.

The high-speed PWMx module contains up to three PWM generators. Each PWM generator provides two PWM outputs: PWMxH and PWMxL. The master time base generator provides a synchronous signal as a common time base to synchronize the various PWM outputs. The individual PWM outputs are available on the output pins of the device. The input Fault signals and current-limit signals, when enabled, can monitor and protect the system by placing the PWM outputs into a known “safe” state.

Each PWMx can generate a trigger to the ADC module to sample the analog signal at a specific instance during the PWM period. In addition, the high-speed PWMx module also generates a Special Event Trigger to the ADC module based on either of the two master time bases.

The high-speed PWMx module can synchronize itself with an external signal or can act as a synchronizing source to any external device. The SYNC1 input pin that utilizes PPS, can synchronize the high-speed PWMx module with an external signal. The SYNC0 pin is an output pin that provides a synchronous signal to an external device.

Figure 16-1 illustrates an architectural overview of the high-speed PWMx module and its interconnection with the CPU and other peripherals.

### 16.1 PWM Faults

The PWMx module incorporates multiple external Fault inputs to include FLT1 and FLT2 which are remappable using the PPS feature, FLT3 and FLT4 which are available only on the larger 44-pin and 64-pin packages, and FLT32 which has been implemented with Class B safety features, and is available on a fixed pin on all dsPIC33EPXXXMC20X/50X and PIC24EPXXXMC20X devices.

These Faults provide a safe and reliable way to safely shut down the PWM outputs when the Fault input is asserted.

#### 16.1.1 PWM FAULTS AT RESET

During any Reset event, the PWMx module maintains ownership of the Class B Fault, FLT32. At Reset, this Fault is enabled in Latched mode to ensure the fail-safe power-up of the application. The application software must clear the PWM Fault before enabling the high-speed motor control PWMx module. To clear the Fault condition, the FLT32 pin must first be pulled low externally or the internal pull-down resistor in the CNPDx register can be enabled.

**Note:** The Fault mode may be changed using the FLTMOD<1:0> bits (FCLCON<1:0>), regardless of the state of FLT32.

**REGISTER 16-14: TRIGx: PWMx PRIMARY TRIGGER COMPARE VALUE REGISTER**

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
TRGCMP<15:8>							
bit 15				bit 8			

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
TRGCMP<7:0>							
bit 7				bit 0			

**Legend:**

R = Readable bit

W = Writable bit

U = Unimplemented bit, read as '0'

-n = Value at POR

'1' = Bit is set

'0' = Bit is cleared

x = Bit is unknown

bit 15-0 **TRGCMP<15:0>**: Trigger Control Value bits

When the primary PWMx functions in local time base, this register contains the compare values that can trigger the ADC module.

## 19.0 INTER-INTEGRATED CIRCUIT™ (I<sup>2</sup>C™)

**Note 1:** This data sheet summarizes the features of the dsPIC33EPXXXGP50X, dsPIC33EPXXXMC20X/50X and PIC24EPXXXGP/MC20X families of devices. It is not intended to be a comprehensive reference source. To complement the information in this data sheet, refer to “**Inter-Integrated Circuit™ (I<sup>2</sup>C™)**” (DS70330) in the “*dsPIC33/PIC24 Family Reference Manual*”, which is available from the Microchip web site ([www.microchip.com](http://www.microchip.com)).

- 2: Some registers and associated bits described in this section may not be available on all devices. Refer to **Section 4.0 “Memory Organization”** in this data sheet for device-specific register and bit information.
- 3: There are minimum bit rates of approximately  $F_{CY}/512$ . As a result, high processor speeds may not support 100 Kbit/second operation. See timing specifications, IM10 and IM11, and the “**Baud Rate Generator**” in the “*dsPIC33/PIC24 Family Reference Manual*”.

The dsPIC33EPXXXGP50X, dsPIC33EPXXXMC20X/50X and PIC24EPXXXGP/MC20X family of devices contains two Inter-Integrated Circuit (I<sup>2</sup>C) modules: I2C1 and I2C2.

The I<sup>2</sup>C module provides complete hardware support for both Slave and Multi-Master modes of the I<sup>2</sup>C serial communication standard, with a 16-bit interface.

The I<sup>2</sup>C module has a 2-pin interface:

- The SCLx pin is clock
- The SDAx pin is data

The I<sup>2</sup>C module offers the following key features:

- I<sup>2</sup>C interface supporting both Master and Slave modes of operation
- I<sup>2</sup>C Slave mode supports 7 and 10-bit addressing
- I<sup>2</sup>C Master mode supports 7 and 10-bit addressing
- I<sup>2</sup>C port allows bidirectional transfers between master and slaves
- Serial clock synchronization for I<sup>2</sup>C port can be used as a handshake mechanism to suspend and resume serial transfer (SCLREL control)
- I<sup>2</sup>C supports multi-master operation, detects bus collision and arbitrates accordingly
- Intelligent Platform Management Interface (IPMI) support
- System Management Bus (SMBus) support

**REGISTER 21-13: CxBUFPNT2: ECANx FILTER 4-7 BUFFER POINTER REGISTER 2**

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
F7BP<3:0>				F6BP<3:0>			
bit 15				bit 8			
R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
F5BP<3:0>				F4BP<3:0>			
bit 7				bit 0			

**Legend:**

R = Readable bit                      W = Writable bit                      U = Unimplemented bit, read as '0'  
-n = Value at POR                      '1' = Bit is set                      '0' = Bit is cleared                      x = Bit is unknown

- bit 15-12      **F7BP<3:0>**: RX Buffer Mask for Filter 7 bits  
1111 = Filter hits received in RX FIFO buffer  
1110 = Filter hits received in RX Buffer 14  
•  
•  
•  
0001 = Filter hits received in RX Buffer 1  
0000 = Filter hits received in RX Buffer 0
- bit 11-8      **F6BP<3:0>**: RX Buffer Mask for Filter 6 bits (same values as bits<15:12>)
- bit 7-4      **F5BP<3:0>**: RX Buffer Mask for Filter 5 bits (same values as bits<15:12>)
- bit 3-0      **F4BP<3:0>**: RX Buffer Mask for Filter 4 bits (same values as bits<15:12>)

**REGISTER 21-14: CxBUFPNT3: ECANx FILTER 8-11 BUFFER POINTER REGISTER 3**

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
F11BP<3:0>				F10BP<3:0>			
bit 15				bit 8			
R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
F9BP<3:0>				F8BP<3:0>			
bit 7				bit 0			

**Legend:**

R = Readable bit                      W = Writable bit                      U = Unimplemented bit, read as '0'  
-n = Value at POR                      '1' = Bit is set                      '0' = Bit is cleared                      x = Bit is unknown

- bit 15-12      **F11BP<3:0>**: RX Buffer Mask for Filter 11 bits  
1111 = Filter hits received in RX FIFO buffer  
1110 = Filter hits received in RX Buffer 14  
•  
•  
•  
0001 = Filter hits received in RX Buffer 1  
0000 = Filter hits received in RX Buffer 0
- bit 11-8      **F10BP<3:0>**: RX Buffer Mask for Filter 10 bits (same values as bits<15:12>)
- bit 7-4      **F9BP<3:0>**: RX Buffer Mask for Filter 9 bits (same values as bits<15:12>)
- bit 3-0      **F8BP<3:0>**: RX Buffer Mask for Filter 8 bits (same values as bits<15:12>)

## 23.2 ADC Helpful Tips

1. The SMP1x control bits in the AD1CON2 register:
  - a) Determine when the ADC interrupt flag is set and an interrupt is generated, if enabled.
  - b) When the CSCNA bit in the AD1CON2 registers is set to '1', this determines when the ADC analog scan channel list, defined in the AD1CSSL/AD1CSSH registers, starts over from the beginning.
  - c) When the DMA peripheral is not used (ADDMAEN = 0), this determines when the ADC Result Buffer Pointer to ADC1BUF0-ADC1BUFF gets reset back to the beginning at ADC1BUF0.
  - d) When the DMA peripheral is used (ADDMAEN = 1), this determines when the DMA Address Pointer is incremented after a sample/conversion operation. ADC1BUF0 is the only ADC buffer used in this mode. The ADC Result Buffer Pointer to ADC1BUF0-ADC1BUFF gets reset back to the beginning at ADC1BUF0. The DMA address is incremented after completion of every 32nd sample/conversion operation. Conversion results are stored in the ADC1BUF0 register for transfer to RAM using DMA.
2. When the DMA module is disabled (ADDMAEN = 0), the ADC has 16 result buffers. ADC conversion results are stored sequentially in ADC1BUF0-ADC1BUFF, regardless of which analog inputs are being used subject to the SMP1x bits and the condition described in 1c) above. There is no relationship between the ANx input being measured and which ADC buffer (ADC1BUF0-ADC1BUFF) that the conversion results will be placed in.
3. When the DMA module is enabled (ADDMAEN = 1), the ADC module has only 1 ADC result buffer (i.e., ADC1BUF0) per ADC peripheral and the ADC conversion result must be read, either by the CPU or DMA Controller, before the next ADC conversion is complete to avoid overwriting the previous value.
4. The DONE bit (AD1CON1<0>) is only cleared at the start of each conversion and is set at the completion of the conversion, but remains set indefinitely, even through the next sample phase until the next conversion begins. If application code is monitoring the DONE bit in any kind of software loop, the user must consider this behavior because the CPU code execution is faster than the ADC. As a result, in Manual Sample mode, particularly where the user's code is setting the SAMP bit (AD1CON1<1>), the DONE bit should also be cleared by the user application just before setting the SAMP bit.

5. Enabling op amps, comparator inputs and external voltage references can limit the availability of analog inputs (ANx pins). For example, when Op Amp 2 is enabled, the pins for AN0, AN1 and AN2 are used by the op amp's inputs and output. This negates the usefulness of Alternate Input mode since the MUXA selections use AN0-AN2. Carefully study the ADC block diagram to determine the configuration that will best suit your application. Configuration examples are available in the "**Analog-to-Digital Converter (ADC)**" (DS70621) section in the "*dsPIC33/PIC24 Family Reference Manual*".

## 23.3 ADC Resources

Many useful resources are provided on the main product page of the Microchip web site for the devices listed in this data sheet. This product page, which can be accessed using this link, contains the latest updates and additional information.

**Note:** In the event you are not able to access the product page using the link above, enter this URL in your browser:  
<http://www.microchip.com/wwwproducts/Devices.aspx?dDocName=en555464>

### 23.3.1 KEY RESOURCES

- "**Analog-to-Digital Converter (ADC)**" (DS70621) in the "*dsPIC33/PIC24 Family Reference Manual*"
- Code Samples
- Application Notes
- Software Libraries
- Webinars
- All Related "*dsPIC33/PIC24 Family Reference Manual*" Sections
- Development Tools

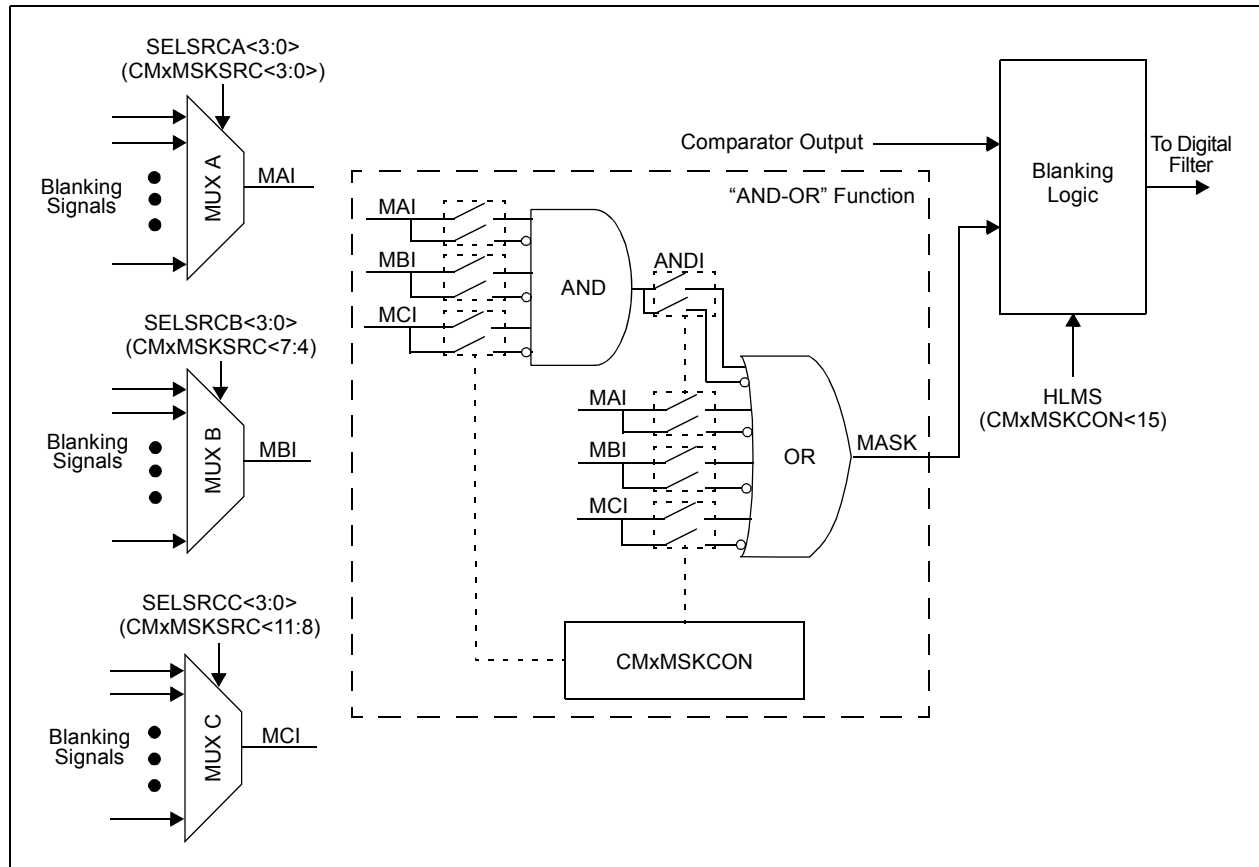
**REGISTER 24-3: PTGBTE: PTG BROADCAST TRIGGER ENABLE REGISTER<sup>(1,2)</sup> (CONTINUED)**

- bit 4      **OC1CS:** Clock Source for OC1 bit  
1 = Generates clock pulse when the broadcast command is executed  
0 = Does not generate clock pulse when the broadcast command is executed
- bit 3      **OC4TSS:** Trigger/Synchronization Source for OC4 bit  
1 = Generates Trigger/Synchronization when the broadcast command is executed  
0 = Does not generate Trigger/Synchronization when the broadcast command is executed
- bit 2      **OC3TSS:** Trigger/Synchronization Source for OC3 bit  
1 = Generates Trigger/Synchronization when the broadcast command is executed  
0 = Does not generate Trigger/Synchronization when the broadcast command is executed
- bit 1      **OC2TSS:** Trigger/Synchronization Source for OC2 bit  
1 = Generates Trigger/Synchronization when the broadcast command is executed  
0 = Does not generate Trigger/Synchronization when the broadcast command is executed
- bit 0      **OC1TSS:** Trigger/Synchronization Source for OC1 bit  
1 = Generates Trigger/Synchronization when the broadcast command is executed  
0 = Does not generate Trigger/Synchronization when the broadcast command is executed

**Note 1:** This register is read-only when the PTG module is executing Step commands (PTGEN = 1 and PTGSTRT = 1).

**2:** This register is only used with the PTGCTRL OPTION = 1111 Step command.

**FIGURE 25-4: USER-PROGRAMMABLE BLANKING FUNCTION BLOCK DIAGRAM**



**FIGURE 25-5: DIGITAL FILTER INTERCONNECT BLOCK DIAGRAM**

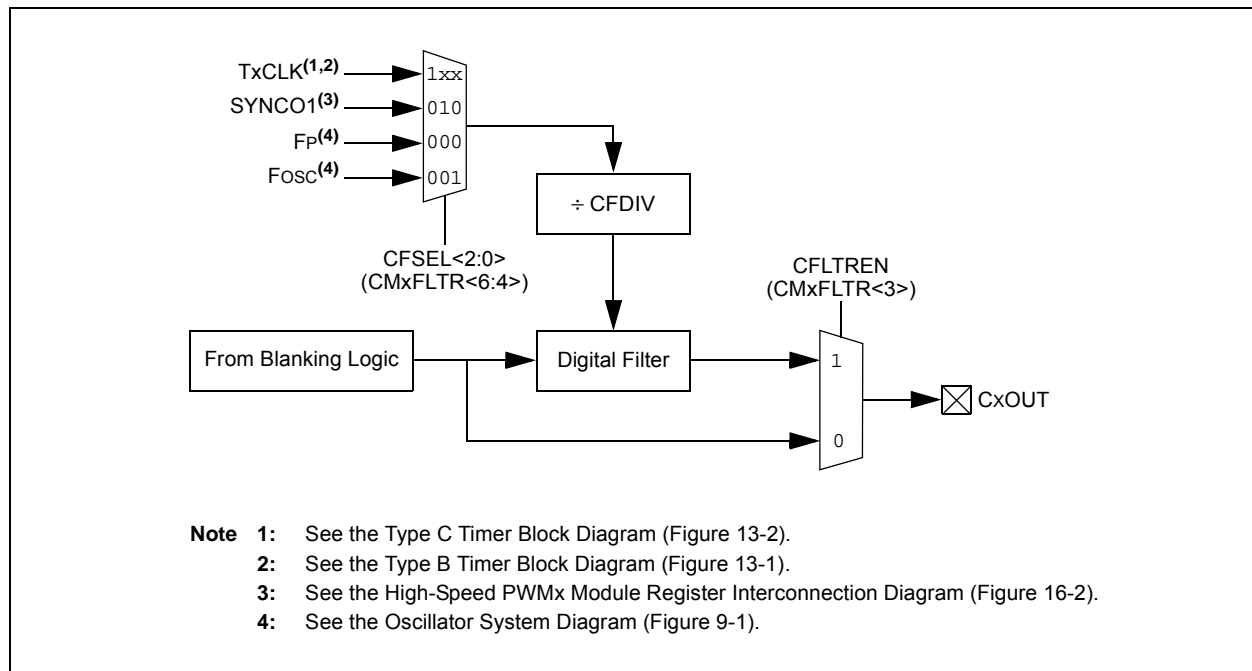


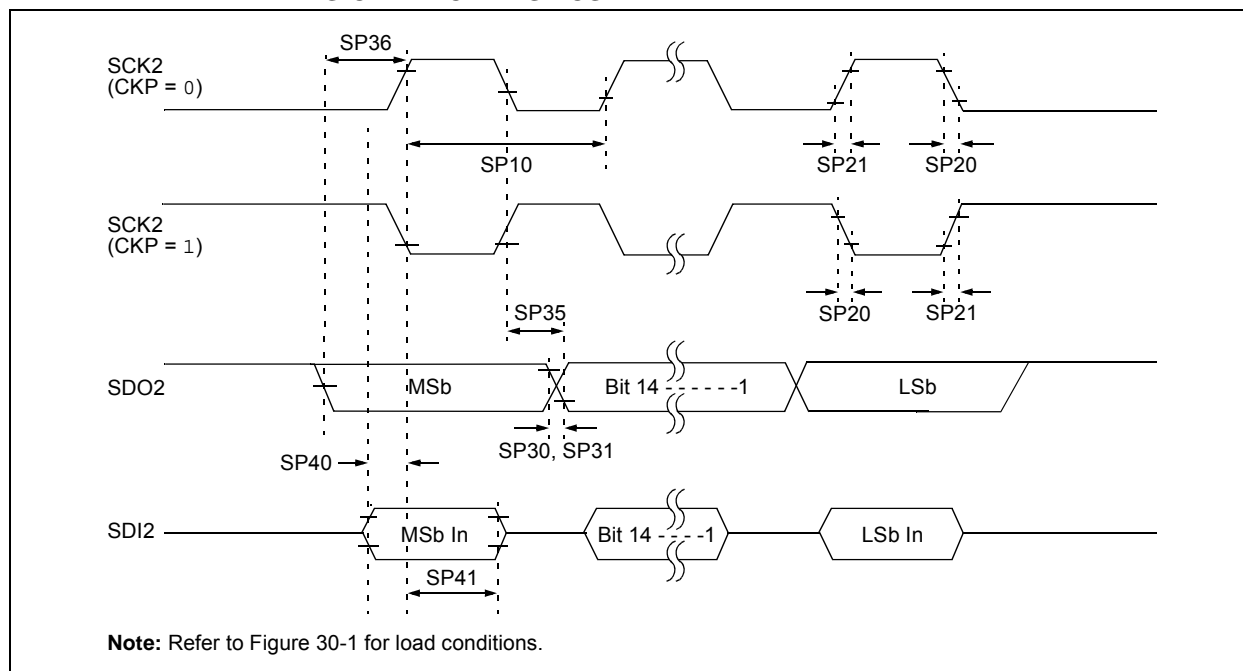


TABLE 30-11: DC CHARACTERISTICS: I/O PIN INPUT SPECIFICATIONS (CONTINUED)

DC CHARACTERISTICS			Standard Operating Conditions: 3.0V to 3.6V (unless otherwise stated) Operating temperature $-40^{\circ}\text{C} \leq T_A \leq +85^{\circ}\text{C}$ for Industrial $-40^{\circ}\text{C} \leq T_A \leq +125^{\circ}\text{C}$ for Extended				
Param No.	Symbol	Characteristic	Min.	Typ.	Max.	Units	Conditions
DI60a	I <sub>ICL</sub>	Input Low Injection Current	0	—	-5 <sup>(4,7)</sup>	mA	All pins except V <sub>DD</sub> , V <sub>SS</sub> , AV <sub>DD</sub> , AV <sub>SS</sub> , MCLR, VCAP and RB7
DI60b	I <sub>ICH</sub>	Input High Injection Current	0	—	+5 <sup>(5,6,7)</sup>	mA	All pins except V <sub>DD</sub> , V <sub>SS</sub> , AV <sub>DD</sub> , AV <sub>SS</sub> , MCLR, VCAP, RB7 and all 5V tolerant pins <sup>(6)</sup>
DI60c	$\Sigma I_{ICT}$	Total Input Injection Current (sum of all I/O and control pins)	-20 <sup>(8)</sup>	—	+20 <sup>(8)</sup>	mA	Absolute instantaneous sum of all $\pm$ input injection currents from all I/O pins ( $ I_{ICL}  +  I_{ICH} $ ) $\leq \Sigma I_{ICT}$

- Note 1:** The leakage current on the MCLR pin is strongly dependent on the applied voltage level. The specified levels represent normal operating conditions. Higher leakage current can be measured at different input voltages.
- 2:** Negative current is defined as current sourced by the pin.
- 3:** See the “Pin Diagrams” section for the 5V tolerant I/O pins.
- 4:** V<sub>IL</sub> source < (V<sub>SS</sub> – 0.3). Characterized but not tested.
- 5:** Non-5V tolerant pins V<sub>IH</sub> source > (V<sub>DD</sub> + 0.3), 5V tolerant pins V<sub>IH</sub> source > 5.5V. Characterized but not tested.
- 6:** Digital 5V tolerant pins cannot tolerate any “positive” input injection current from input sources > 5.5V.
- 7:** Non-zero injection currents can affect the ADC results by approximately 4-6 counts.
- 8:** Any number and/or combination of I/O pins not excluded under I<sub>ICL</sub> or I<sub>ICH</sub> conditions are permitted provided the mathematical “absolute instantaneous” sum of the input injection currents from all pins do not exceed the specified limit. Characterized but not tested.

**FIGURE 30-16: SPI2 MASTER MODE (FULL-DUPLEX, CKE = 1, CKP = x, SMP = 1)**  
**TIMING CHARACTERISTICS**



**TABLE 30-35: SPI2 MASTER MODE (FULL-DUPLEX, CKE = 1, CKP = x, SMP = 1)**  
**TIMING REQUIREMENTS**

AC CHARACTERISTICS			Standard Operating Conditions: 3.0V to 3.6V (unless otherwise stated) Operating temperature -40°C ≤ TA ≤ +85°C for Industrial -40°C ≤ TA ≤ +125°C for Extended				
Param.	Symbol	Characteristic <sup>(1)</sup>	Min.	Typ. <sup>(2)</sup>	Max.	Units	Conditions
SP10	FscP	Maximum SCK2 Frequency	—	—	9	MHz	(Note 3)
SP20	TscF	SCK2 Output Fall Time	—	—	—	ns	See Parameter DO32 (Note 4)
SP21	TscR	SCK2 Output Rise Time	—	—	—	ns	See Parameter DO31 (Note 4)
SP30	TdoF	SDO2 Data Output Fall Time	—	—	—	ns	See Parameter DO32 (Note 4)
SP31	TdoR	SDO2 Data Output Rise Time	—	—	—	ns	See Parameter DO31 (Note 4)
SP35	Tsch2doV, TscL2doV	SDO2 Data Output Valid after SCK2 Edge	—	6	20	ns	
SP36	TdoV2sc, TdoV2scL	SDO2 Data Output Setup to First SCK2 Edge	30	—	—	ns	
SP40	TdiV2sch, TdiV2scL	Setup Time of SDI2 Data Input to SCK2 Edge	30	—	—	ns	
SP41	Tsch2diL, TscL2diL	Hold Time of SDI2 Data Input to SCK2 Edge	30	—	—	ns	

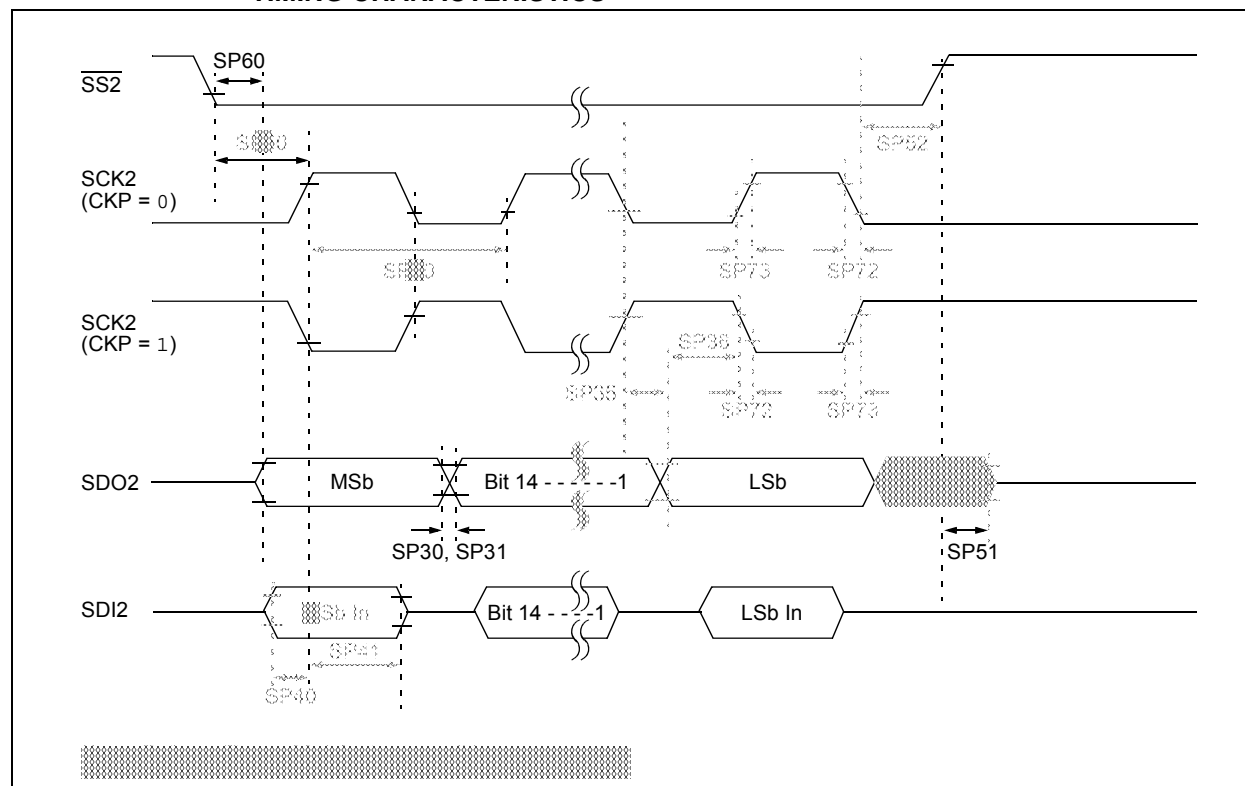
**Note 1:** These parameters are characterized, but are not tested in manufacturing.

**2:** Data in "Typical" column is at 3.3V, +25°C unless otherwise stated.

**3:** The minimum clock period for SCK2 is 111 ns. The clock generated in Master mode must not violate this specification.

**4:** Assumes 50 pF load on all SPI2 pins.

**FIGURE 30-18: SPI2 SLAVE MODE (FULL-DUPLEX, CKE = 1, CKP = 0, SMP = 0)  
TIMING CHARACTERISTICS**



**TABLE 30-37: SPI2 SLAVE MODE (FULL-DUPLEX, CKE = 1, CKP = 0, SMP = 0)  
TIMING REQUIREMENTS**

AC CHARACTERISTICS			Standard Operating Conditions: 3.0V to 3.6V (unless otherwise stated) Operating temperature -40°C ≤ TA ≤ +85°C for Industrial -40°C ≤ TA ≤ +125°C for Extended				
Param.	Symbol	Characteristic <sup>(1)</sup>	Min.	Typ. <sup>(2)</sup>	Max.	Units	Conditions
SP70	FscP	Maximum SCK2 Input Frequency	—	—	Lesser of Fp or 15	MHz	(Note 3)
SP72	TscF	SCK2 Input Fall Time	—	—	—	ns	See Parameter DO32 (Note 4)
SP73	TscR	SCK2 Input Rise Time	—	—	—	ns	See Parameter DO31 (Note 4)
SP30	TdoF	SDO2 Data Output Fall Time	—	—	—	ns	See Parameter DO32 (Note 4)
SP31	TdoR	SDO2 Data Output Rise Time	—	—	—	ns	See Parameter DO31 (Note 4)
SP35	Tsch2doV, TscL2doV	SDO2 Data Output Valid after SCK2 Edge	—	6	20	ns	
SP36	TdoV2scH, TdoV2scL	SDO2 Data Output Setup to First SCK2 Edge	30	—	—	ns	
SP40	TdiV2scH, TdiV2scL	Setup Time of SDI2 Data Input to SCK2 Edge	30	—	—	ns	
SP41	Tsch2diL, TscL2diL	Hold Time of SDI2 Data Input to SCK2 Edge	30	—	—	ns	
SP50	TssL2scH, TssL2scL	$\overline{SS2}$ ↓ to SCK2 ↑ or SCK2 ↓ Input	120	—	—	ns	
SP51	TssH2doZ	$\overline{SS2}$ ↑ to SDO2 Output High-Impedance	10	—	50	ns	(Note 4)
SP52	Tsch2ssH TscL2ssH	$\overline{SS2}$ ↑ after SCK2 Edge	1.5 Tcy + 40	—	—	ns	(Note 4)
SP60	TssL2doV	SDO2 Data Output Valid after $\overline{SS2}$ Edge	—	—	50	ns	

**Note 1:** These parameters are characterized, but are not tested in manufacturing.

**2:** Data in “Typical” column is at 3.3V, +25°C unless otherwise stated.

**3:** The minimum clock period for SCK2 is 66.7 ns. Therefore, the SCK2 clock generated by the master must not violate this specification.

**4:** Assumes 50 pF load on all SPI2 pins.

**NOTES:**